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Tuning the electrical performance and bias stability of a semiconducting SWCNT thin film transistor with an atomic layer deposited AlZrOx composite

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Solution-processed semiconducting single-walled carbon nanotube (s-SWCNT) thin film transistors (TFTs) based on different atomic layer deposited AlZrOx insulators are fabricated and characterized. It is found that increasing the Al concentration in the AlZrOx insulator can reduce leakage current and decrease the surface roughness of the AlZrOx insulator. Compared with the device with a ZrO_2 insulator, the electrical performance, including subthreshold swing, I_{on}/I_{off} and hysteresis, and negative bias stability of s-SWCNT TFTs with the AlZrOx insulator has been significantly improved. The s-SWCNT TFT based on AlZrOx with a ZrO_2/Al_2O_3 cycle ratio of 1/2 reveals a superior electrical performance with an average mobility of 35.2 cm^2 V^{-1} s^{-1}, a high on/off ratio of 3.7×10^5, a low subthreshold swing of 0.09, a small hysteresis of 0.1 V, and a small threshold voltage shift of 1.62 V under a negative bias stress of −3 V for 1800 s. The improvement of electrical performance and stability for the s-SWCNT TFT with the AlZrOx insulator is attributed to the smooth surface and less AlZrOx/s-SWCNT interface traps. Our results suggest that using a AlZrOx film as a gate insulator can be a useful technique to achieve high performance and more reliable solution-processed s-SWCNT TFTs.

Introduction

Single-walled carbon nanotube (SWCNT) thin film transistors (TFTs) have shown potential in the next generation flexible electronic devices due to their high carrier mobility, high chemical stability, transparency and excellent mechanical properties.[1–3] However, conventional SWCNTs contain both metallic and semiconducting SWCNTs, which results in a poor on/off current ratio and high off state current.[4–8] In order to improve the on/off current ratio, solution-processed pre-separated high-purity semiconducting SWCNTs were recently reported for high performance TFTs. Selective removal of metallic CNTs *via* electrical breakdown has been studied to increase the on/off current ratio. However, these methods cause serious destruction of the remaining nanotubes in the networks.[9–11] In order to achieve low-cost fabrication, solution processed semiconducting SWCNTs have been used for application in transistors. Many methods, such as gradient ultra-centrifugation,[12,13] gel chromatography,[14,15] and selective extraction by conjugated polymers,[16,17] have demonstrated the effective isolation of semiconducting SWCNTs. Despite the separation of metallic and semiconducting SWCNTs, the choice

of gate dielectric is still a key issue in electrical improvement of semiconducting SWCNT TFTs because the electrical properties of SWCNT-TFTs are strongly dependent on the surface conditions, dielectric constant and leakage current of the dielectric layer. In previous works, thermally grown SiO_2 gate insulator is frequently studied for semiconducting SWCNT TFT. However, the process temperature and low dielectric constant of thermally grown SiO_2 insulator is difficult to require the demand of high performance and flexible SWCNT TFT.[18] High k materials, such as ZrO_2,[19] HfO_2,[20] have been prepared for high performance SWCNT TFT. Although ZrO_2 shows a high permittivity of 20–25, it suffers from its high leakage current due to a narrow band gap and existing oxygen vacancies. To address this disadvantage, cation doping is considered as a feasible method to improve band gap and suppress oxygen vacancies of ZrO_2. Recently, yttrium–scandium oxide high-k dielectric is deposited by a solution process for TFT application.[21] Sputtered amorphous strontium titanate film can be used as gate insulator of low–voltage TFTs.[22] Furthermore, Al_2O_3 is a promising gate dielectric material because of its amorphous structure, low-leakage current, acceptable dielectric constant (6.5–9), and wide band gap (5.6–7.8 eV).[23] Combining both advantages of ZrO_2 and Al_2O_3, it is expected to develop a novel dielectric material AlZrOx to meet the requirement of high performance semiconducting SWCNT TFTs. Compared to other deposition methods, atomic layer deposition (ALD) is capable of producing high quality conformal film with control of the thickness and composition of the films at the atomic level.[24] Ultimately, AlZrOx

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gate dielectric with high dielectric constant and low leakage current can be optimized by tuning the Al content.

In the work, $AlZrO_x$ high-k gate insulators with different Al contents are firstly prepared and semiconducting SWCNT TFTs with different $AlZrO_x$ insulators were fabricated. The influence of Al content on the electrical performance, structure, and surface topography of $AlZrO_x$ insulators are investigated. The electrical performance and temperature stress stability of SWCNT TFTs with different $AlZrO_x$ insulators are analyzed. The work aims to supply a facile strategy to enhance performance and bias stability of semiconducting SWCNT thin film transistor with atomic layer deposited $AlZrO_x$ composite.

Experimental

The bottom gate top-contact-type TFTs were fabricated on the highly-doped Si substrate with ZrO_2 and $AlZrO_x$ thin films grown by atom layer deposition as gate insulators. The structure of device is shown in Fig. 1(a). During deposition process, precursors for Zr, Al and O were Tetrakis dimethyl amino zirconium (TDMAZr), $Al(CH_3)_3$ (TMA), and H_2O, respectively. TDMAZr and TMA precursors are purchased from Jiangsu Fu Na Electronic Technology Co., Ltd (China) and Air Liquid Holding Co. Ltd (France). The deposition temperature is about 250 °C. Typical pulsing sequences during ALD process are 1/5/3/5 s (TDMAZr/Ar purge/H_2O/Ar purge) and 1/4/2/5 s (TMA/Ar purge/H_2O/Ar purge) for the growth of ZrO_2 and Al_2O_3 film, respectively. The Al doping concentration in the $AlZrO_x$ film was controlled by adjusting the cycle ratio of the Al_2O_3 and ZrO_2 processes. The cycle ratio of ZrO_2 and Al_2O_3 are 2/1, 1/1, and 1/2 for $AlZrO_{x-1}$, $AlZrO_{x-2}$, and $AlZrO_{x-3}$, respectively. The thickness of all $AlZrO_x$ films was controlled by the total deposition cycles and fixed at 170 nm. For the Al_2O_3 and ZrO_2 film, the overall reactions between the precursors and the surface can be shown:[25,26]

$$2Al(CH_3)_3 + 3H_2O \rightarrow Al_2O_3 + 3CH_4 \qquad (1)$$

$$Zr(N(CH_3)_2)_4 + 2H_2O \rightarrow ZrO_2 + 4H(N(CH_3)_2) \qquad (2)$$

The Ni (10 nm)/Au (90 nm) source and drain electrodes were patterned onto the $Si/AlZrO_x$ wafer by a photolithography process with the channel width (W) of 20 μm and channel length (L) of 10 μm. Next, the well-sonicated 99.9% semi-SWCNTs (Nanointegris, Arc discharge nanotube, average diameter range of 1.4 nm and average length of 1 μm) precursor solution was drop-casted onto the channel region as the active material of p-channel transistors with the solution concentration of 0.1 mg mL^{-1} and the volume of 20 μL at room temperature. The semiconducting SWCNTs were enriched by polymer extraction, so the channel region was cleaned by toluene to remove the polymer. The surface morphology of the semiconducting SWCNTs is shown in Fig. 1(b).

The thickness of thin film was measured by the alpha step (Alpha-Step IQ). The electrical characteristics of semi-SWCNTs TFTs were measured using Agilent E3647A Dual output DC power supply and Keithley 6485 Picoammeter. The capacitance characteristics were measured by Agilent E4980A LRC meter. The surface morphology of thin films was investigated using atomic force microscopy (SII NanoTechnology SPI 4000) with tapping mode. The roughness parameters are as measured over 1.5×1.5 μm^2, and evaluated using the software supplied with the instrument. The structure of $AlZrO_x$ thin films was measured by grazing incidence X-ray diffraction (GIXRD) scans using Cu Kα radiation. The X-ray source was composed of a sealed X-ray tube, a multilayer monochromator able to select a parallel beam of Cu Kα radiation and a system of crossed slits defining a beam of appropriate size. GIXRD spectra were collected on a position sensitive detector (Inel CPS120). The angle of incidence $\omega = 0.5°$ was chosen as not widely exceeding the critical angle for total external reflection of $AlZrO_x$. The chemical bonding states of films were carried out with the X-ray photoelectron spectroscopy (XPS) (Thermo-ESCALAB250XL)) in ultrahigh vacuum (UHV).

Results and discussion

Fig. 2(a) shows the GIXRD patterns of $AlZrO_x$ films with different Al contents. In the previous work,[27] it is verified that ZrO_2 film shows a crystalline structure with a sharp diffraction peak of 35.2°. When Al content is doped into ZrO_2 film, diffraction peak is not observed in the XRD patterns. It suggests that $AlZrO_x$ film shows the amorphous nature. The crystallization-to-amorphous transition is achieved by adding a suitable dopant, because the original bond structure order is distorted.[28] In addition, the amorphous $AlZrO_x$ film is suitable to prepare large-size and uniform thin films. The insulating properties of $AlZrO_x$ films with different Al content are characterized by measuring the leakage current versus bias voltage, as shown in Fig. 2(b). The leakage current density of ZrO_2 thin film is 2.2×10^{-8} mA cm^{-2} at the electrical field strength of 2 MV cm^{-1}. The increased leakage current density is attributed to crystalline grain boundaries of ZrO_2, which can acts as current leakage paths and defect/break-down centers.[29] For comparison, the leakage current density of $AlZrO_x$ film is decreased with increasing Al content. The leakage current density of $AlZrO_{x-3}$ thin film is 3.5×10^{-9} mA cm^{-2} at the electrical field strength of 2 MV cm^{-1}. The value
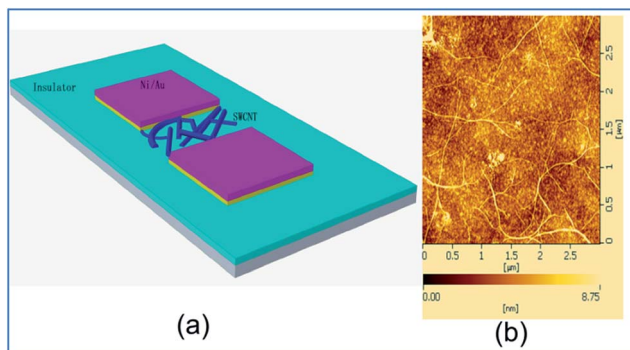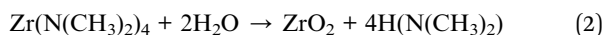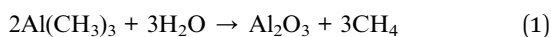

Fig. 1 (a) Schematic structure of Semiconducting SWCNT thin film transistors. (b) The surface morphology of the semiconducting SWCNTs by AFM.
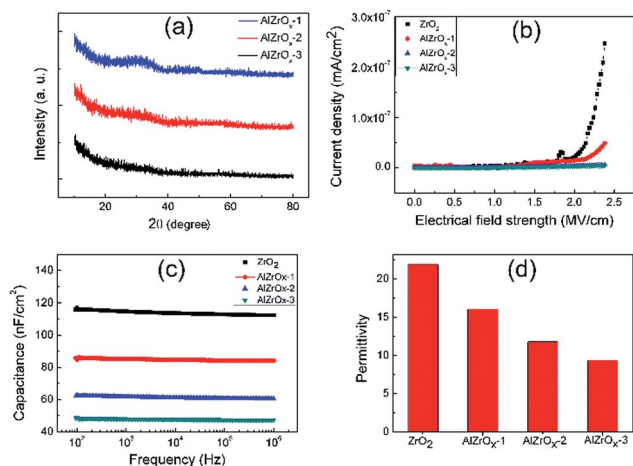
Fig. 2 (a) The GIXRD patterns of AlZrO$_x$ films with different Al contents. (b) The leakage current *versus* bias voltage of AlZrO$_x$ films. (c) The areal capacitance of AlZrO$_x$ film as a function of the frequency. (d) The dielectric permittivity of AlZrO$_x$ and ZrO$_2$ film.

is better than that of other high-k insulators by sputtering and solution process.[30,31] To characterize the capacitance properties of AlZrO$_x$ thin films, a capacitor with the structure of Al/AlZrO$_x$/ p$^+$-Si is prepared. Fig. 2(c) shows the areal capacitance of AlZrO$_x$ film as a function of the frequency. The capacitance of ZrO$_2$, AlZrO$_{x-1}$, AlZrO$_{x-2}$, and AlZrO$_{x-3}$ at a frequency of 1 kHz is 114.0, 84.1, 61.5, and 48.2 nF cm^{-2}, respectively. AlZrO$_x$ films show a smaller frequency dispersion of the capacitance than ZrO$_2$ film, indicating that AlZrO$_x$ films exhibit a low defect density and oxygen vacancies. The similar results were reported by the previous work.[32,33] T. J. Park *et al.* have also verified that Al doping can reduce the electrical defects in atomic layer deposited HfO$_2$ films.[34] The dielectric permittivity (ε_r) can be calculated by the following equation: $C = \varepsilon_0 \varepsilon_r S/d$, where S is the area, d is the thickness of film. The dielectric permittivity of ZrO$_2$, AlZrO$_{x-1}$, AlZrO$_{x-2}$ and AlZrO$_{x-3}$ thin film are 21.9, 16.1, 11.8 and 9.7, respectively. The details are shown in Fig. 2(d). The dielectric permittivity of AlZrO$_x$ film decreases with increasing Al content. It can be explained by considering the dielectric constants of Al$_2$O$_3$ and ZrO$_2$.

Fig. 3 shows XPS spectra of Zr 3d and Al 2p. All the XPS peaks are calibrated with C 1s peak centered at 284.8 eV. As shown in Fig. 2(a), the peak positions of Zr 3d$_{5/2}$ and Zr 3d$_{3/2}$ for ZrO$_2$ film are at 181.9 eV and 184.3 eV, respectively. The binding energy of
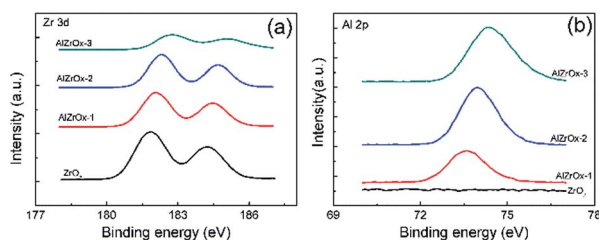
Al 2p of AlZrO$_{x-1}$, AlZrO$_{x-2}$, and AlZrO$_{x-3}$ is 73.6, 74.0, and 74.3 eV, respectively. It is easily seen that the binding energy of Al 2p of all AlZrO$_x$ films are lower than that of Al$_2$O$_3$ (74.8 eV).[35,36] Both Zr 3d and Al 2p peaks for AlZrO$_x$ thin films shift to higher binding energy with increasing Al concentration. It is found that the leading contribution is the charge transfer contribution. The charges transfer can be estimated with DFT-LDA calculations. The similar result is previously reported.[37] In addition, it suggests that the AlZrO$_x$ films mainly consist of Zr–O–Al bonds and present a homogenous structure with negligible phase-separated ZrO$_2$ and Al$_2$O$_3$. The similar result is reported by other groups.[18] The real concentrations of Al are 20.99%, 25.74%, and 30.0% for AlZrO$_{x-1}$, AlZrO$_{x-2}$, and AlZrO$_{x-3}$, respectively.

Fig. 4 shows the AFM images of AlZrO$_x$ insulators with different Al content. The root mean square (rms) of ZrO$_2$, AlZrO$_{x-1}$, AlZrO$_{x-2}$ and AlZrO$_{x-3}$ film is 1.2, 0.86, 0.66 and 0.46 nm, respectively. It suggests that Al doping can reduce rms of AlZrO$_x$ film and improve the surface roughness of AlZrO$_x$. In previous XRD analysis, Al doping can suppress the formation of grain boundaries. It is reported that smooth insulator surface could induce much less interface defects and obtain a better insulator–channel interface, which leads to higher mobility of TFTs.[38] Thus, smooth AlZrO$_x$ insulator is expected to fabricate high performance semiconducting SWCNT TFTs.

Fig. 5 shows the transfer characteristics and hysteresis of semiconducting SWCNT TFTs with different AlZrO$_x$ insulators. The transfer characteristic of SWCNT TFTs is measured between gate voltage of 3 V and −3 V with a fixed drain bias voltage of −3 V. The low operating voltage suggests that it is suitable to fabricate electronic devices with low power consumption. The turn-on voltage (V_{on}) shows a negative voltage direction shift with the increase in the Al concentration. It is ascribed to the decrease in capacitance with the increase in the Al concentration of AlZrO$_x$ film. The field mobility (μ) and threshold voltage (V_T) can be extracted from the following equation[39]
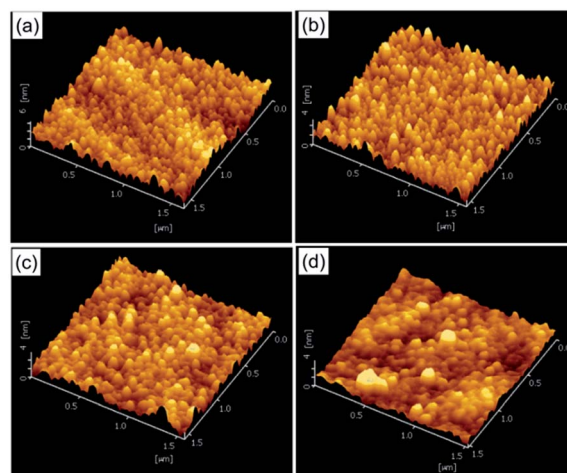

Fig. 3 XPS spectra of the samples with various Al contents: (a) Zr 3d. (b) Al 2p.

Fig. 4 The AFM images of AlZrO$_x$ insulators with different Al content. (a) ZrO$_2$, (b) AlZrO$_{x-1}$, (c) AlZrO$_{x-2}$, (d) AlZrO$_{x-3}$.
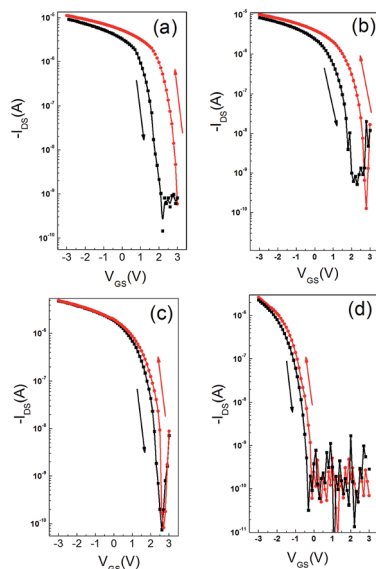
Fig. 5 The transfer characteristics and hysteresis of semiconducting SWCNT TFTs with different gate insulators. (a) ZrO_2, (b) $AlZrO_{x-1}$, (c) $AlZrO_{x-2}$, (d) $AlZrO_{x-3}$.

$$I_{DS} = (V_{GS} - V_T)^2 \times W\mu C_i/2L, \; V_{DS} > V_{GS} - V_T \quad (3)$$

where I_{DS} is the drain-source current, W is the width of channel, L is the length of channel, V_{GS} is the gate voltage, and C_i is the intrinsic capacitance. For SWCNT transistors, the intrinsic capacitance can be calculated using eqn (4) by considering the effect of electrostatic coupling between semi-SWCNTs.[40]

$$C_i = \left\{ \frac{1}{2\pi\varepsilon_0\varepsilon_i} \times \ln\left[\frac{\Lambda_0}{R} \times \frac{\sinh\left(\frac{2\pi t_i}{\Lambda_0}\right)}{\pi} \right] + \frac{1}{C_Q} \right\}^{-1} \times \Lambda_0^{-1} \quad (4)$$

where ε_0 is the vacuum permittivity, ε_i is dielectric constant of dielectric layer, t_i is the thickness of dielectric layer, $C_Q = 4 \times 10^{-10}$ F m^{-1} is the quantum capacitance of semi-SWCNTs, $R = 1$ nm is the average radius of semi-SWCNTs and $\Lambda_0^{-1} = 2.25$ tubes per μm is the linear density of semi-SWCNTs. In our case, the calculated intrinsic capacitance is estimated to be approximately 24.5%, 27.0%, 31.2%, and 29.9% of the gate capacitance based on the parallel plate model, respectively. Consequently, the average intrinsic μ of ZrO_2, $AlZrO_{x-1}$, $AlZrO_{x-2}$, and $AlZrO_{x-3}$ based TFTs are calculated to be 28.7, 30.6, 33.3, and 35.2 cm^2 V^{-1} s^{-1}, respectively. The average intrinsic μ of the devices are tested from the total of 25 devices. The results shows a very strong control on the electrical performance of s-SWCNT TFT by controlling the Al concentration in $AlZrO_x$ insulator. The average mobility improvement of SWCNT TFTs with $AlZrO_{x-3}$ insulator is attributed to smooth surface and low interface trap states, leading to the reduced probability of carrier scattering. The threshold voltage of the device is reduced from 3.2 to −0.5 V with increasing Al content. The result is attributed to the increased capacitance with increasing Al content. More details are shown in Table 1.

The hysteresis of the device is observed in the I_{DS} versus V_{GS} characteristics as shown in Fig. 5. The hysteresis of $AlZrO_{x-3}$

Table 1 The average electrical performance of SWCNT TFTs with different gate insulators

Device	μ (cm^2 V^{-1} s^{-1})	V_T (V)	SS (V dec^{-1})	I_{on}/I_{off}	Hysteresis (V)
ZrO_2	28.7	3.2	0.15	1.2×10^4	1.43
$AlZrO_{x-1}$	30.6	2.3	0.12	2.5×10^4	1.01
$AlZrO_{x-2}$	33.3	1.8	0.10	8×10^4	0.2
$AlZrO_{x-3}$	35.2	−0.5	0.09	3.7×10^5	0.1

based TFT shows a small hysteresis of 0.1 V, which is obviously smaller than that (1.43 V) of ZrO_2 based TFT. Generally, hysteresis in the SWCNT transistor is attributed to trap states in the dielectric or SWCNT/dielectric interface.[41] It is reported that hydroxyl groups (–OH) present on the surface of dielectric layer is considered to be interface defects and significant contributors to hysteresis.[42] Upon applying a gate bias of 3 V, the negative charges formed on the surface of gate insulator can be trapped by –OH group. It facilitates the conduction during the forward sweep in gate voltage. Thus, the threshold voltage of the transistor will shift toward the positive direction. Conversely, a negative gate bias discharges –OH groups into their neutral states, thereby reducing the conductivity for hole transport during the reverse sweep. It suggests that Al doping can effectively reduce the trap states in the ZrO_2 and SWCNT/insulator interface. The results also verified the above XRD and XPS analysis. The effect trap density of states (N_{trap}) of semiconducting SWCNT TFTs can be estimated by the following equation[41,43]

$$SS = dV_{GS}/d(\text{Log } I_{DS}) \quad (5)$$

$$SS = \frac{kT \; \ln 10}{e} \left[1 + \frac{e^2}{C_i} N_{trap} \right] \quad (6)$$

where SS is the subthreshold swing, k is the Boltzmann constant, T is temperature, and C_i is the intrinsic capacitance. The effective trap density for ZrO_2, $AlZrO_{x-1}$, $AlZrO_{x-2}$, and $AlZrO_{x-3}$ based TFTs are estimated to be 4.33×10^{11}, 2.82×10^{11}, 1.92×10^{11}, and 1.34×10^{11} cm^{-2} eV^{-1}, respectively. $AlZrO_{x-3}$ based TFTs shows a smaller trap density, which is attributed to smooth surface and less trap in $AlZrO_{x-3}$ film. The effective trap density is obviously smaller than that of SWCNT-TFTs with SiO_2 and SiN_x gate dielectric.[44]

The negative gate bias stability of semiconducting SWCNT TFTs with different $AlZrO_x$ insulators is evaluated. Fig. 6 shows the transfer characteristics ($V_{DS} = −3$ V) before and after bias stress at a V_{GS} of −3 V for 1800 s in ambient air. For all devices, the transfer characteristics shift slightly toward the negative direction with increasing the stress time. The V_T shift (ΔV_T) of the device with $AlZrO_x$ insulator is smaller than that of the device with ZrO_2 insulator under similar stress condition. ΔV_T of ZrO_2, $AlZrO_{x-1}$, $AlZrO_{x-2}$, and $AlZrO_{x-3}$ based TFTs for 1800 s stress time is 5.01, 3.24, 2.5, and 1.62 V, respectively. It suggests that the negative bias stability is improved with increasing the Al content in $AlZrO_x$ insulator. The negative gate bias instabilities of semiconducting SWCNT TFTs are generally considered to be due to the hole trapping at the interface between the
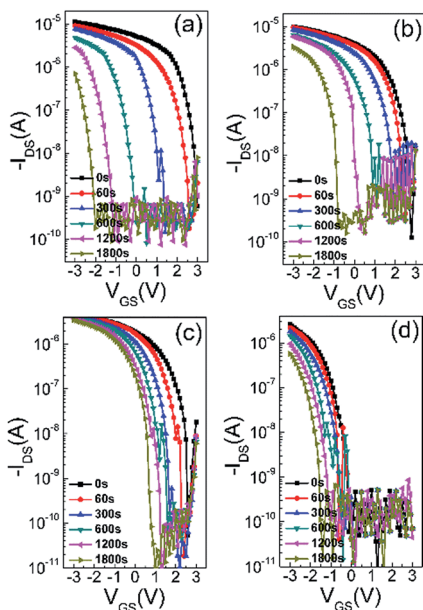
Fig. 6 The negative gate bias stability of semiconducting SWCNT TFTs with different gate insulators. (a) ZrO_2, (b) $AlZrO_{x-1}$, (c) $AlZrO_{x-2}$, (d) $AlZrO_{x-3}$.

semiconducting SWCNT channel layer and $ZrAlO_x$ gate insulator or $ZrAlO_x$ bulk gate insulator. The accumulated hole slowly fills up these trap states under negative gate bias stress. After removal of the stress voltage, the trapped charge can be slowly released again. In addition, the origin of the threshold voltage shift with stress time can be expressed by the stretched exponential model:[45]

$$|\Delta V_T| = \Delta V_{T0}\{1 - \exp[-(t/\tau)^\beta]\} \quad (7)$$

where ΔV_{T0} is the saturated threshold voltage at infinite time, β and τ are the exponent of the trapping rate and the relaxation time of the trapped charges, respectively. The obtained τ values are 6.59×10^2, 8.24×10^2, 1.24×10^3, and 2.63×10^3 s for semiconducting SWCNT TFT with ZrO_2, $AlZrO_{x-1}$, $AlZrO_{x-2}$, and $AlZrO_{x-3}$, respectively. It demonstrates that the degradation of $AlZrO_x$ based TFT is slower than that of ZrO_2-based TFT under a long-time operation. The long trapping time leads to capturing holes frequently at the gate dielectric or at the interface between the gate insulator and channel. Thus, it results in a small threshold voltage shift at the same stress conditions. Detailed comparison of the previous works has been shown in Table 2. It is easily seen that our SWCNT transistors have a high mobility and good stability.

The impact of temperature stress on the electrical performance of semiconducting SWCNT TFTs is also characterized. Fig. 7 shows the transfer curves of semiconducting SWCNT TFTs with temperature varying from 293 to 353 K. For all of the devices, the on-state current and the mobility are enhanced with increasing temperature. It is reported that temperature dependent measurements of SWCNT TFTs is consistent with thermally activated transport.[52] Thus, the thermally activated drain current can be described by the following relation: $I_{DS} \propto \exp(-E_a/kT)$,

Table 2 Comparison of electrical performance for SWCNT TFTs

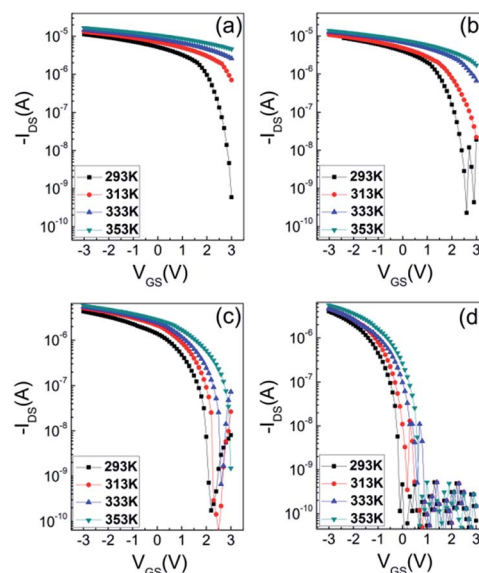| Ref.	μ (cm^2 V^{-1} s^{-1})	V_T (V)	I_{on}/I_{off}	ΔV_T (V) (PBS)
SiO$_2$/CNT[46]	15.03	−0.45	∼10^5	—
SiO$_2$/CNT[47]	∼38	0–1	∼10^5	—
SiO$_2$/CNT[48]	18	0	∼10^6	—
Ion-gel/CNT[49]	>100	−1.0–1.5	138	—
BTO/CNT[50]	0.21	−1.8	∼10^3	—
PV3D3/CNT[51]	9.76	<4V	3 × 10^4	—
Our work	35.2	−0.5	3.7 × 10^5	1.62

Fig. 7 The transfer curves of semiconducting SWCNT TFTs with temperature varying from 293 to 353 K. (a) ZrO_2, (b) $AlZrO_{x-1}$, (c) $AlZrO_{x-2}$, (d) $AlZrO_{x-3}$.

where T and E_a are temperature and activation energy, respectively. At high temperature, polarons are thermally activated to hop between localized states in a faster manner, resulting in high mobility. In addition, the threshold voltage shift of the device under same temperature stress decreases with increasing Al content in the $AlZrO_x$ insulator. The device with $AlZrO_{x-3}$ shows a small threshold voltage shift of 1.18 V under the temperature stress of 353 K. It is reported that the threshold voltage shift is correlated with the total density of states, consisting of the density of states of the bulk channel and interface trap density.[53] Thus, a smaller threshold voltage shift can be attributed to the fact that adding Al into ZrO_2 film can improve the surface roughness and reduce interface trap states. The result is consistent with the previous conclusion.

Conclusions

In summary, $AlZrO_x$ films with different Al contents have been successfully prepared by atomic layer deposition. Increasing Al concentration in the $AlZrO_x$ insulator can reduce leakage current and decrease the surface roughness of $AlZrO_x$ insulator.

$AlZrO_{x-3}$ thin film shows a low leakage current density of 3.5×10^{-9} mA cm^{-2} at the electrical field strength of 2 MV cm^{-1} and a small rms of 0.46 nm. The SWCNT TFT based on $AlZrO_x$ with $AlZrO_{x-3}$ gate insulator exhibits a superior electrical performance with an average mobility of 35.2 cm^2 V^{-1} s^{-1}, a high on/off ratio of 3.7×10^5, a low subthreshold swing of 0.09, and a little hysteresis of 0.1 V, and a small threshold voltage shift of 1.62 V under negative bias stress of -3 V for 1800 s. The improvement of electrical performance and stability for SWCNT TFT with $AlZrO_x$ insulator is attributed to the smooth surface and less $AlZrO_x$/SWCNT interface trap. It suggests that $AlZrO_x$ film combining the advantage of ZrO_2 and Al_2O_3 is a promising candidate as gate insulator for achieving high performance and more reliable solution-processed semiconducting SWCNT TFTs.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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