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Fully solution-induced high performance indium oxide thin film transistors with ZrO_x high-k gate dielectrics†

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Solution based deposition has been recently considered as a viable option for low-cost flexible electronics. In this context, research efforts have been increasingly focused on the development of suitable solution-processed materials for oxide based transistors. In this work, we report a fully solution synthesis route, using 2-methoxyethanol as solvent, for the preparation of In_2O_3 thin films and ZrO_x gate dielectrics, as well as the fabrication of In_2O_3-based TFTs. To verify the possible applications of ZrO_x thin films as the gate dielectric in complementary metal oxide semiconductor (CMOS) electronics, fully solution-induced In_2O_3 TFTs based on ZrO_2 dielectrics have been integrated and investigated. The devices, with an optimized annealing temperature of 300 °C, have demonstrated high electrical performance and operational stability at a low voltage of 2 V, including a high μ_{sat} of 4.42 $cm^2\ V^{-1}\ s^{-1}$, low threshold voltage of 0.31 V, threshold voltage shift of 0.15 V under positive bias stress for 7200 s, and large I_{on}/I_{off} of 7.5×10^7, respectively. The as-fabricated In_2O_3/ZrO_x TFTs enable fully solution-derived oxide TFTs for potential application in portable and low-power consumption electronics.

1. Introduction

Metal oxide semiconductors have been attracting considerable attention as excellent channel materials for thin-film transistors (TFTs) in backplane electronics for active-matrix organic light-emitting diodes (AMOLEDs) and other emerging electronic applications such as commentary-metal-oxide-semiconductor (CMOS) and logic gate devices on low cost substrates due to their high mobility, together with high driven currents, the possibility of coupling optical transparency to visible light and mechanical flexibility with excellent electrical performance.[1,2] Indeed, the performance of oxide-based TFTs, especially the carrier mobility, exceeds that of amorphous Si-based TFTs, and their stability rivals or exceeds that of typical organic semiconductors.[3,4] As a result, metal-oxide-based TFTs have been regarded as the most potential candidates for next generation TFTs in flat panel display driven circuits. Unfortunately, these high-mobility oxide TFTs are conventionally manufactured using costly vacuum-based processing methodologies, such as pulsed laser deposition, atomic layer deposition, and sputtering.[1,3] In spite of their advantages from vacuum-based methods, the high fabrication cost and complex preparation process become major obstacles for realizing large-area electronic devices with high performance.

In an effort to address this problem, recently, there has been remarkable development of high-performance TFTs based on solution-processable oxide semiconductors, such as spin-coating,[5] inkjet printing,[6] spray pyrolysis,[7] and dip-coating,[8] which offers the advantages of simplicity, versatility, and scale-up capability. In addition, solution-derived TFTs have demonstrated impressive performance,[9–12] which in some cases are comparable to or even surpass the ones obtained by physical techniques.[13] However, for traditional oxide-based TFTs fabricated by solution-processed method, a high temperature annealing process is imperative to obtain optimized semiconductor properties.[14] In order to fabricate solution-processed oxide TFTs on flexible polymeric substrates, it is desirable to reduce the process temperature and enable greater process flexibility due to the lower thermal budget. To achieve high performance solution-processed oxide TFTs at low temperatures, appropriate metal precursors, solvents, and gate dielectrics should be taken into account.

As a potential candidate of channel material for the transparent electronics, indium oxide (In_2O_3) has been paid more attention due to its high electron mobility and high optical transparency in the visible region.[15–17] In_2O_3 exhibits excellent electrical properties, including metallic, semiconducting, and insulating characteristics depending on the stoichiometry and defects in materials.[5] Combining the advantages of "solution

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route" and In_2O_3 materials, it can be noted that solution-processed In_2O_3 has been regarded as the promising candidate to fabricate high performance oxide TFTs devices at low temperature.

Although whilst progress on solution-processed oxide TFTs has been rapidly advancing, most of these TFTs generally based on conventional SiO_2 as dielectric requires high operation voltages to put out usable drain current.[18,19] To decrease operation voltage and power consumption for the realization of mobile and portable applications, recent work has been focused on the investigation of large areal capacitance gate dielectrics, including ultrathin nano-dielectrics,[20] electrolyte gate dielectrics,[21] and high-k oxide dielectrics.[22] Among these candidates, oxide-based high-k dielectrics have been regarded as the promising alternatives due to their high dielectric constant and stable interface chemistry with oxide semiconductors.[23,24] By far, oxide transistors based on high-k dielectrics have been confirmed to be successful and demonstrates optimized performance compared to conventional SiO_2 dielectrics.[7,25–28] Among these, ZrO_2 has become one of the most remarkable gate dielectrics due to its relatively high dielectric constants, good thermal stability, and suitable band alignment.[16,29] Shan *et al.* have demonstrated In_2O_3 TFTs based on ZrO_x dielectric exhibits a saturation mobility of 3.08 $cm^2 V^{-1} s^{-1}$ and an on/off current ratio of 10^8.[16] Pradhan *et al.* fabricated CdS TFTs with ZrO_2 as the gate dielectric grown by chemical bath, which exhibits a low operation voltage of 3.8 V and a field effect mobility of 4 $cm^2 V^{-1} s^{-1}$.[30] Despite their attractive properties, however, TFTs based on high-k gate dielectric are usually realized using stringent and potentially costly manufacturing techniques.[7] The development of solution-derived dielectrics is still a step behind, inhibiting the realization of fully solution-processed TFTs with high performance. Although there exist some investigations on the fully solution-processed TFTs, the fabrication of solution-processed TFTs suffers from strict experimental condition, such as high annealing temperature, long annealing time, and complex process, which limits the further development of In_2O_3 TFTs *via* the solution route in high performance electronics. Therefore, the experimental process and the device performance of fully solution-derived TFTs should be optimized.

It has been shown that the carrier mobility and transport properties of TFTs, derived from solution-processed methods, are strongly dependent on the preparation condition, including annealing conditions and the precursor solution concentration.[15,25,31] However, the annealing temperature modulated electrical properties of the fully solution-processed oxide TFTs is not investigated systematically before. In current work, we demonstrate a fully solution-processed method, a simple and large-area-compatible deposition technique, which can be used for the processing of high-quality ZrO_2 dielectric and In_2O_3 channel layer onto Si substrates. An in-depth investigation was performed to reveal the effect of annealing temperature on the structural and dielectric properties of ZrO_x dielectric. In order to confirm the possibility of the In_2O_3 thin films as channel layer, their applications in TFTs based on ZrO_x dielectric by device engineering were also demonstrated. In particular, it has been demonstrated In_2O_3/ZrO_x TFT exhibited a high performance under a ultralow operating voltage of 2 V, with a high I_{on}/I_{off} of around 10^7, and a high μ_{sat} of 4.42 $cm^2 V^{-1} s^{-1}$.

2. Experimental

2.1 Preparations of precursor solutions

The In_2O_3 (0.1 M) and ZrO_x (0.1 M) precursor solution was synthesized through respectively dissolving indium nitrate hydrate ($InN_3O_9 \cdot xH_2O$) and zirconium oxychloride octahydrate ($ZrOCl_2 \cdot 8H_2O$) in 2-methoxyethanol ($C_3H_8O_2$) solution. The precursor solutions were stirred at room temperature for 6 h by a magnetic stirrer. After that, to get a more pure sol solution, the solutions were filtered through a 0.22 μm injection filter before spin coating.

2.2 Film deposition and devices fabrication

Heavily doped p-type Si wafers with resistivity of 0.02 Ω cm were cleaned by a modified RCA method, and etched by hydrofluoric acid and dried by N_2. Then, all-processed wafers were placed in a plasma cleaner to enhance the hydrophilicity of the substrate surface. The ZrO_x solution was filtered through a 0.22 μm injection filter and then spun on the hydrophilic Si substrates at 800 rpm for 6 s and 5000 rpm for 25 s, and then ZrO_x thin films were placed on the roaster and bake at 150 °C for 10 minutes to remove the residual solvent and cooled to room temperature. In order to obtain the desired thickness, the procedure was repeated twice times. At the end, all the ZrO_x thin films were annealed in air with temperatures ranging from 300 °C to 600 °C for 1 h, and their thicknesses were 18.28, 18.02, 17.56, and 17.08 nm, respectively.

The In_2O_3 precursor solution was respectively spun on heavily doped p-type Si substrates with thermally grown SiO_2 gate dielectric (200 nm) and 400 °C-annealed ZrO_x thin films at 800 rpm for 6 s and 5000 rpm for 25 s, and then the laminated samples were annealed at 250–325 °C in air for 1 h. Finally, Al source and drain electrodes were deposited by thermal evaporation through a shadow mask. The channel length and width for all devices were 100 and 1000 μm, respectively. The detailed schematic diagram of the solution-process for In_2O_3 and ZrO_x thin films and In_2O_3-based TFTs fabrication are demonstrated in Fig. 1. In order to measure the dielectric properties of the ZrO_x thin films, MOS capacitor based on structures of Al/ZrO_x/p^+-Si/Al were fabricated and investigated using an impedance analyzer (TH2636B).

2.3 Characterization

The microstructure of ZrO_x gate dielectric thin films correlated to annealing temperature were studied by X-Ray diffractometer (XRD). The thickness of In_2O_3 (about 9 nm) and ZrO_x thin films was obtained by spectroscopy ellipsometry (SE) (SC630, SANCO Co, Shanghai). The ultraviolet visible spectroscopy (UV-Vis, Shimadzu, UV-2550) were carried out to investigate the annealing temperature dependent band gap and transmittance spectra of the ZrO_x thin films. The surface morphologies of the ZrO_x thin films were investigated by atomic force microscopy (AFM). X-Ray photoelectron spectroscopy (XPS, ESCALAB 250Xi

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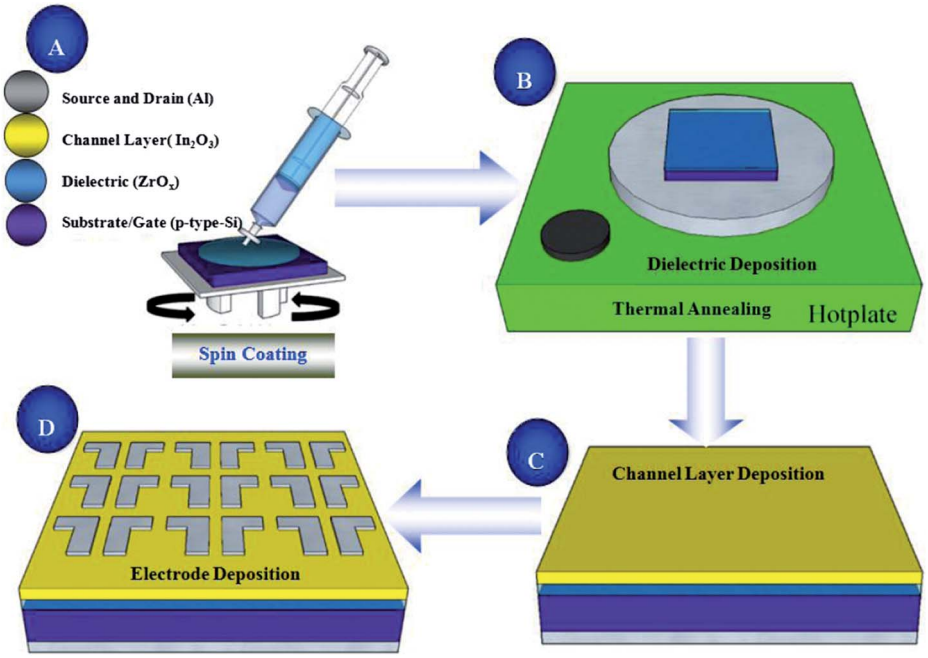

Fig. 1 Schematic diagram of solution-derived In_2O_3 and ZrO_x thin films and In_2O_3 TFTs device fabrication.

Thermo Scientific) was used to analyze the chemical compositions of the ZrO_x thin films. The electrical properties of the ZrO_x thin films, In_2O_3/SiO_2 TFTs and In_2O_3/ZrO_x TFTs were measured by using an Agilent B1500A semiconductor device analyzer in a dark shelter.

3. Results and discussion

3.1 Microstructure and surface morphology of ZrO_x thin films

Fig. 2 shows the XRD patterns for the solution-derived ZrO_x thin films as a function of annealing temperature. Based on Fig. 2, it can be noted that ZrO_x thin films keep amorphous when the annealing temperature is lower than 400 °C. However, when the annealing temperature has increased to 500 °C, the amorphous state disappears and polycrystalline films with diffraction patterns matching that of ZrO_x have been detected, indicating that the formation of ZrO_x phase is thermally activated and crystallization takes place at 500 °C, which is in good agreement with the observation from Park *et al.*[32] Four main peaks centered at 30.4°, 35.1°, 50.6° and 60.1° corresponding to the (011), (110), (020), and (121) planes of ZrO_x, are attributed to the tetragonal phase of ZrO_2.[32] Further increase of annealing temperature enhances the crystallinity of the film, which is represented by the decreased full width at half maximum (FWHM) of the ZrO_x peaks. The high annealing temperature supplies high kinetic energy and increases the surface mobility of deposited particles.[31] As we know, as a potential candidate of dielectric layer for TFTs, the amorphous nature of the dielectrics has demonstrates apparent advantage over the crystalline phase due to its low leakage current and high thermal stability. The grain boundaries act as preferential paths for impurity diffusion and leakage current, leading to show high off-state current in TFT devices.[33] In addition, dielectric with amorphous structure normally exhibits smooth surface morphology, which is beneficial to obtain dielectric/channel heterointerface with high quality.[28] For TFTs, the smooth and sharp interface between channel and dielectric layer is highly desired because carrier transport is generally limited in a narrow region of the interface. Thus, it can be inferred that the annealing temperature for solution-processed ZrO_x dielectric should be controlled accurately for the gate dielectric applications.

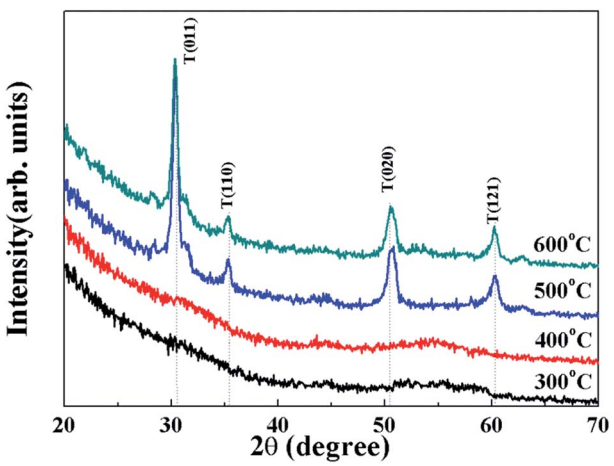

Fig. 2 XRD patterns of ZrO_x thin films as a function of annealing temperature.

Surface morphology of solution-processed ZrO_x dielectric thin films annealed at different temperatures were measured by atomic force microscope (AFM), as shown in Fig. 3. The films

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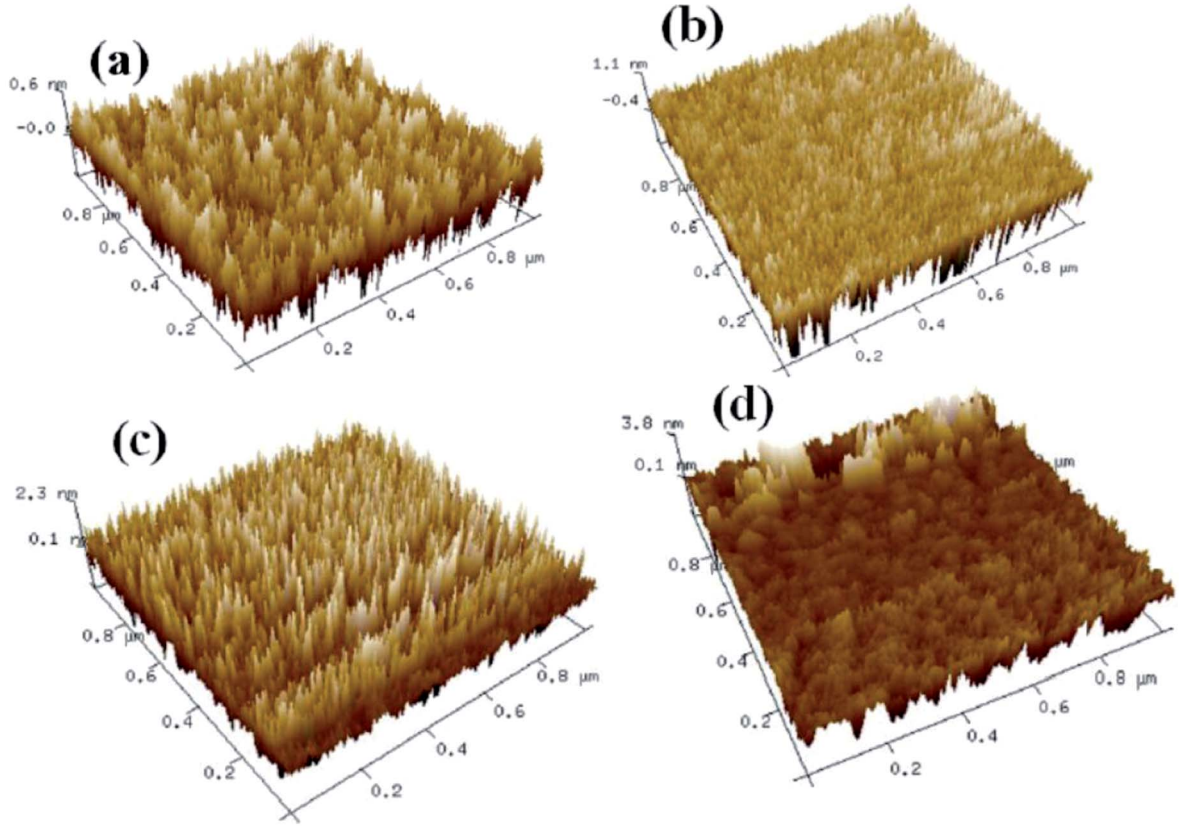

Fig. 3 AFM images of the ZrO_x thin films annealed at (a) 300 °C, (b) 400 °C, (c) 500 °C, (d) 600 °C.

roughness was determined from the AFM height profile of a 1 × 1 μm^2 area scan. The root mean square (RMS) roughness of ZrO_x thin films annealed at 300, 400, 500, and 600 °C are 0.17, 0.37, 0.60, and 0.91 nm, respectively. Based on Fig. 3, RMS values of smaller than 1 nm have been observed for solution-processed ZrO_x dielectrics. The smooth surface of the dielectric layer plays an important role in improving the TFT performance and stability. Indeed, the smooth surface is connected to the reduction of the interface charge traps, carrier scattering centers and so, to the production of an excellent interface between the channel layer and the dielectric layer. This will certainly lead to high performance TFTs with higher field-effect mobility and smaller sub-threshold slope (SS) value. Additionally, dielectric with small RMS is also in favor of growing the high-quality channel layer, which is beneficial to obtain high-stability TFTs.[34] The slight increase in RMS value for the 600 °C-annealed sample may be attributed to the agglomeration induced by high annealing temperature.

3.2 Optical properties characterization of ZrO_x thin films

To investigate the optical properties of the solution-derived ZrO_x dielectric thin films as a function of annealing temperature, the optical transmittances spectra of the ZrO_x thin films on quartz substrates were measured with the wavelength ranging from 200 to 900 nm, as demonstrated in Fig. 4. All of the films are highly transparent with an average optical transmittance of over 80% in the visible range. An optical image of the corresponding ZrO_x thin films annealed at different temperature is shown as the inset of Fig. 4. No apparent color difference between the bare glass and the samples has been observed, demonstrating the good optical transparency. The high transmittances of the ZrO_x thin films indicate the potential

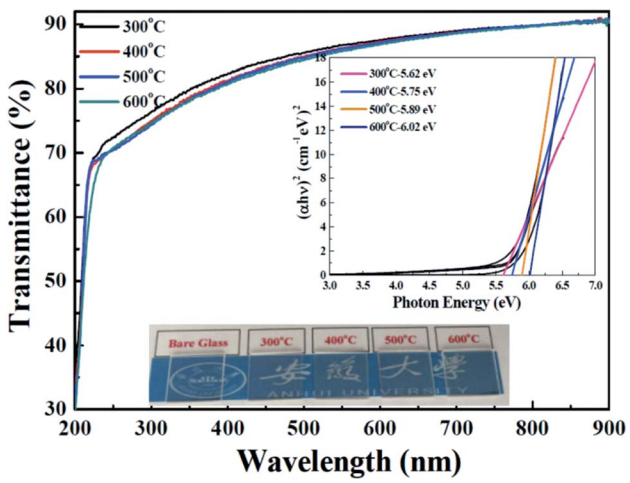

Fig. 4 Optical transmittances of ZrO_x thin films annealed at different temperatures. The insets above and below display the band gap energy values of these ZrO_x films and photographs of bare glass and as-processed ZrO_x thin films annealed at various temperatures, respectively.

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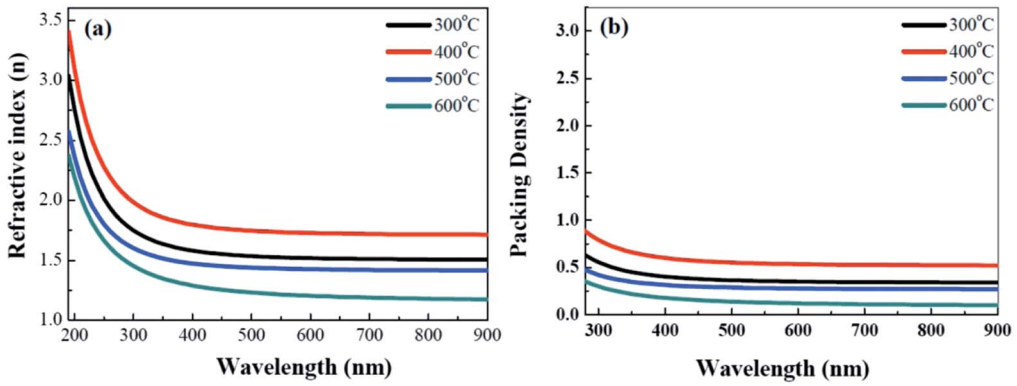

Fig. 5 Annealing temperature dependent refractive index (a) and fitting packing density (b) for solution-derived ZrO_2 thin films.

applications in transparent electronics. With the increase in annealing temperature, a slight reduction in transmittance has been observed, which can be attributed to the increase in surface roughness of ZrO_x thin films or the elimination of oxygen defect at high temperatures.[35] The optical band gap of the ZrO_x thin films was calculated by using a standard Tauc plotmethod,[36] as shown in the inset of Fig. 4. For ZrO_x dielectric annealed at low temperature, the presence of defects in thin films would produce localized states in the forbidden gap, which will lead to the reduced band gap energy.[26] At high annealing temperature, the annihilation of oxygen vacancies/defects results in the reduced density of localized states and the increased band gap energy. As an candidate of high-k gate dielectric for TFTs, it should process higher packing density and compactness, which can be determined by the optical constant of refractive index. Fig. 5a displays the evolution of refractive index of solution-derived ZrO_2 gate dielectrics as a function of annealing temperature. It can be seen that the refractive index increases with the annealing temperature ranging from 300 to 400 °C, indicating the increase in packing density. However, annealing the samples from 500 to 600 °C, reduction in refractive index has been detected, which can be attributed to the increased RMS value for ZrO_2 samples. As we know, the refractive index (n) is related to its packing density (p) and its porosity. Based on the following Yoldas formula,

$$p = (n_p^2 - 1)/(n_{bulk}^2 - 1)$$

where n_p is the refractive index, n_{bulk} is the refractive index in bulk form. Fig. 5b gives the fitted packing density for all the samples as a function of annealing temperature, which fits well the evolution of refractive index. It can be concluded that 400 °C-annealed sample demonstrates increased thin film quality and higher compactness, which indicates its potential application in TFTs.

3.3 X-Ray photoelectron spectroscopy measurements for ZrO_x thin films

The surface impurities, chemical bonding states and compositions of ZrO_x thin films were analyzed by X-ray Photoelectron Spectroscopy (XPS). C 1s peak at 284.6 eV was taken as a reference for charge correction. The charge neutralizations of X-ray bombarded samples are performed by flood guns and spectral deconvolution was performed by Shirley background subtraction using a Voigt function convoluting Gaussian and Lorentzian functions. Fig. 6a shows the O 1s core-level XPS spectra for ZrO_x thin films as a function of annealing temperature. The deconvoluted O 1s spectra show three peaks centered at 529.8, 531.2, and 532.4 eV, respectively. The peak centers at 529.8 and 531.2 eV can be assigned to the oxygen in oxide lattices (Zr–O) and the oxygen vacancy in lattices (V_o), respectively. The feature at 532.4 eV can originate from the hydroxyl species or absorbed H_2O on the surface.[17] The semiquantitative analyses of oxygen compositions are summarized in Fig. 6b. The atomic percentages are calculated based on the area integration of each O 1s peak. Based on Fig. 6b, it can be seen that annealing the samples from 300 to 600 °C, the fraction of O^{2-} in ZrO_x increases and oxygen vacancy or hydroxyl species decreases, indicating that high temperature annealing removes the bonded oxygen including the oxygen vacancy and hydroxyl species, and improves the metal–oxygen lattice. For a good candidate as dielectric layer, the bonded oxygen in the film should be kept at a relatively low level, which can be explained by the fact that the bonded oxygen generally creates defect states in the forbidden band of dielectric film, contributing the uncontrollable leakage current and the reduced breakdown voltage.[37]

Fig. 6c displays the XPS Zr 3d core-level spectra of ZrO_x dielectric thin films annealed at various temperatures. It can be seen that there is a doublet corresponding to Zr $3d_{5/2}$ and Zr $3d_{3/2}$ features at 181.8 and 184.1 eV for 300 °C-annealed sample, respectively. With the increase in annealing temperature, the Zr 3d peaks shift to lower binding energies. The same trend has been observed previously in solution-processed ZrO_x and ScO_x thin films,[26,38] which can be due to the full oxidation of ZrO_x and the enhanced alloy reaction. To obtain the interface chemistry bonding states and interfacial composition of Si/ZrO_x gate stack, XPS depth profile has been performed. After etching the Si/ZrO_x gate stack by Ar^+, Si 2p has been paid more investigation. Fig. 6d shows the Si 2p core-level XPS spectra as a function of annealing temperature. All Si 2p core-level spectra are fitted with three peaks. For all-processed samples, the fitted substrate doublet peaks (Si–Si) have a separation of 0.57 eV, which is composed of the Si $2p_{3/2}$

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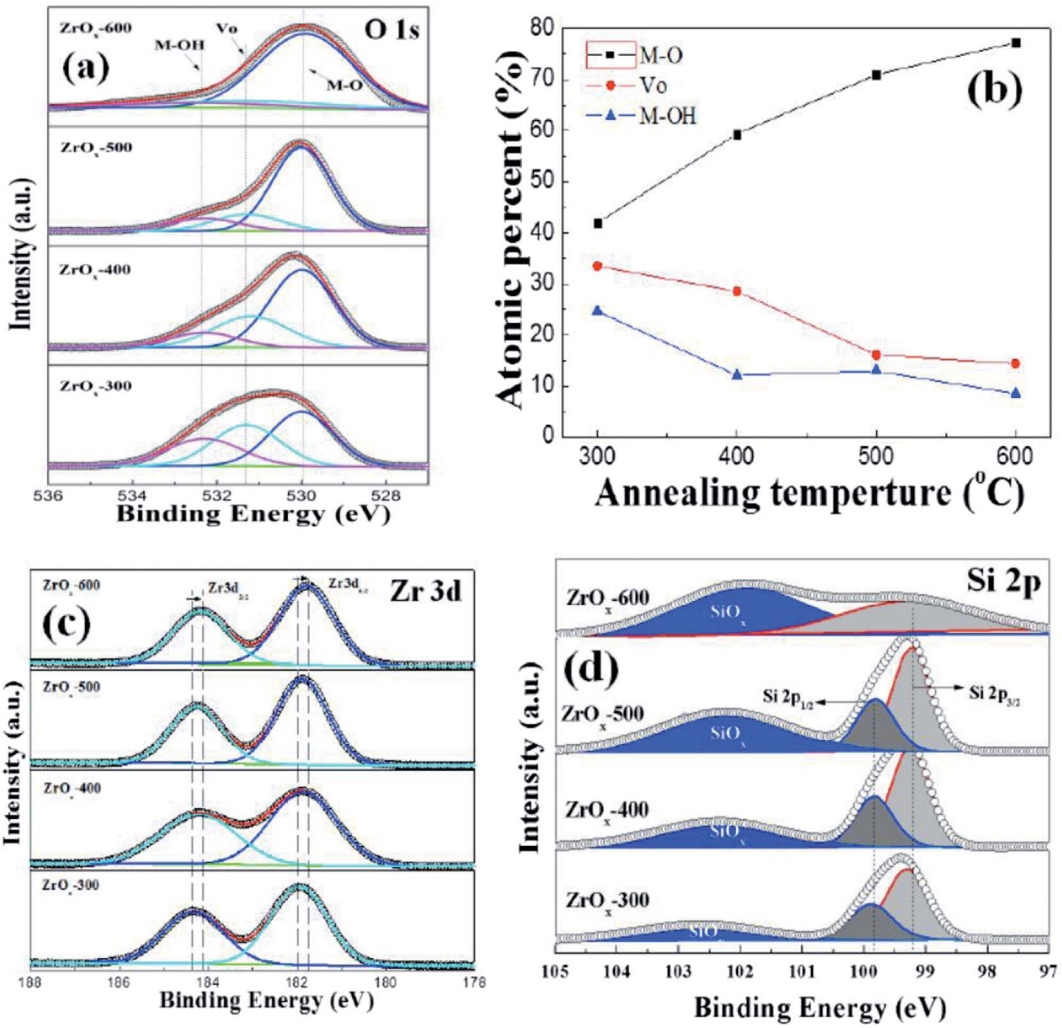

Fig. 6 XPS spectra of O 1s (a) and Zr 3d peaks (c) for ZrO_x thin films as a function of annealing temperature. (b) Semiquantitative analyses of the oxygen component for the corresponding ZrO_x thin films. (d) Si 2p XPS core-level spectra of Si/ZrO_x gate stacks annealed at different temperatures.

for 99.27 eV and Si $2p_{1/2}$ for 99.84 eV. The third peaks centered at 102–103 eV are attributed to the interfacial SiO_x layer. It can be noted that with increasing the annealing temperature, there is a continuous increase in the intensity ratio of the high binding energy content, which is attributed to the formation of more SiO_x interfacial layer by diffusion of oxygen from annealing ambient or oxide film.

3.4 Dielectric and electrical properties of ZrO_x thin films

In order to investigate the dielectric behavior and electrical properties of solution-grown ZrO_x dielectric thin films as a function of annealing temperature, MOS capacitor based on ZrO_x/Si gate stack were fabricated. Fig. 7a demonstrates the frequency dependent areal capacitance. Reduction in area capacitance at high frequency has been detected, which can be attributed to the limited polarization response time.[17] The areal capacitance of ZrO_x thin films annealed at 300, 400, 500, and 600 °C are measured to 388, 313, 268, and 254 nF cm^{-2} at 10^3 Hz, respectively. As a result, the relative dielectric constants for all the samples are calculated to be 7.05, 5.69, 5.09, and 4.65, respectively. With the increase in annealing temperature, it can be seen that the areal capacitance demonstrate an apparent decreased trend, which can be attributed to the formation of low-k interface layer,[39] which is confirmed by previous XPS measurements. In addition, ZrO_x thin films annealed at higher temperatures exhibit weaker frequency dispersion of capacitance, indicating a low defect density such as hydroxyl group and/or oxygen vacancies in thin films. This will be beneficial to control the leakage current because the conduction paths in dielectrics are mainly caused by hydroxyl and grain boundaries.[15]

The current–density and electric field characteristics of the same ZrO_x capacitors are shown in Fig. 7b to evaluate the leakage behavior of the ZrO_x thin films. As can be seen, the MOS capacitor devices based on 400 °C-annealed ZrO_x dielectrics exhibit a low leakage density of 1.5×10^{-9} A cm^{-2} at 2 mV cm^{-1}.[40] The decreased leakage current at 400 °C annealing temperature comes from the gradually decomposition of residuals and reduction in the defect density.[41] The leakage current density levels for devices annealed at 500 °C and 600 °C

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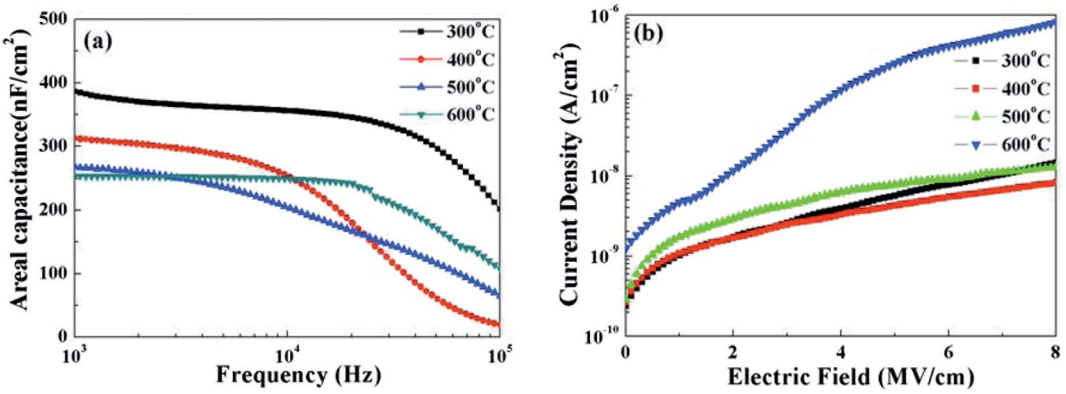

Fig. 7 (a) Areal capacitance and (b) leakage current density of the ZrO_x dielectric thin films annealed at various temperatures.

have been increased much, originating from the increased surface smooth and the crystallization-induced grain boundaries. As a result, it can be concluded that the sufficient low leakage current for 400 °C-annealed solution-processed ZrO_x dielectric attributed to the smooth surface and amorphous structure guarantees its potential application in low-voltage transistor.

3.5 Electrical properties of In_2O_3 TFTs on SiO_2/Si substrate

Based on the aforementioned discussion, it can be inferred that 400 °C-annealed solution-processed ZrO_x dielectric can be applied as potential dielectric thin film in TFTs. Before investigating the feasibility of solution-processed ZrO_x as gate dielectric in TFTs, the possibility of solution-derived In_2O_3 TFTs with bottom-gate and top-contact architecture has been evaluated. Thermally-grown SiO_2 with thickness of 200 nm is adopted as the dielectric layer due to its low trap defects and high reliability. The schematic diagram of the In_2O_3 TFTs is displayed in Fig. 8a. The solution-processed In_2O_3 channel layers were annealed at 250–325 °C. The output curves of each In_2O_3/SiO_2 TFT are shown in Fig. S1 (ESI†) and the typical output characteristics of the as-fabricated In_2O_3 TFTs annealed at different temperatures, at a gate voltage of (V_{GS}) of 20 V, are depicted in Fig. 8b. It has been found that all the as-fabricated TFTs exhibit typical n-type channel conduction behavior with clear pinch-off voltage and current saturation.

The representative transfer characteristics of In_2O_3 TFTs as functions of annealing temperatures, at a drain voltage of (V_{DS}) of 20 V, are displayed in Fig. 8c. With increasing the annealing temperature from 250 to 325 °C, the In_2O_3 TFTs exhibit the increased saturation current and negative shifted threshold voltage (V_{TH}). At the same time, the device operation mode changes from enhancement to depletion mode. The low saturation current at 250 °C may mainly attributed to the formation of defect states and the degree of the oxidation in the channel layer.[38] With the formation of high-temperature-induced In–O bonds in In_2O_3 channel layer and the decreased lattice defects, such as hydroxides and residual impurities,[42,43] the improved electrical performance has been achieved at higher annealing temperatures.

To further investigate the electrical properties of the as-fabricated In_2O_3 TFTs, the saturation mobility (μ_{sat}) and the threshold voltage (V_{TH}) are calculated from the slope of $I_{DS,sat}^{1/2}$ *vs.* V_{GS} according to the following equation,[16]

$$\mu_{sat} = \frac{2L}{WC_i}\left(\frac{\partial\sqrt{I_{DS}}}{\partial V_{GS}}\right)^2$$

where W is the channel width, L is the channel length, V_G is the source-gate voltage, I_D is the saturation current, and C_i is the areal capacitance of the dielectric layer. The extracted TFTs performance parameters as a function of annealing temperature are summarized in Table 1. It is found that μ_{sat} values increase from 0.06 to 0.63 $cm^2\ V^{-1}\ s^{-1}$ with the increase in annealing temperature. According to the observations from Shan *et al.*,[16] solution-derived In_2O_3 channel layer annealed at low temperature contains a large amount of organic groups and degrades the electrical performance of TFTs. Therefore, high annealing temperature leads to the decomposition of organic groups and the formation of metal–oxygen bonds, which attributes to the gradual enhancement of μ_{sat} in TFTs.

The V_{TH} of the In_2O_3 TFTs based on SiO_2 dielectric thin film annealed at 250, 275, 300, and 325 °C is 11.25, 5.56, 4.15, and −22.92 V, respectively. The negative shift of V_{TH} may be mainly due to the decrease amount of interfacial defects acting as carrier trap between In_2O_3 channel and SiO_2 gate dielectric layer. With increasing the annealing temperature, the oxygen vacancy and free carrier concentration decrease. As a result, I_{on}/I_{off} initially increases because of the reduced I_{off}. However, further increase of the annealing temperature for In_2O_3 channel layer to 325 °C leads to the degradation of the device performance, which may be due to the increased trap states near the In_2O_3/SiO_2 interface. The subthreshold swing (SS) value, an important performance parameter, which is defined as the V_{DS} required to increase the I_{DS} by one decade, are calculated to be 1.09, 0.96, 0.41, and 20 V dec^{-1} in 250, 275, 300, and 325 °C-annealed In_2O_3 TFTs. A small SS is expected to achieve a high operation speed and low power consumption. Normally, the SS value is dependent on the traps located in channel/dielectric interface.[44] Based on SS value, the density of interface states (D_{it}) can be inferred using the following equation,[16]

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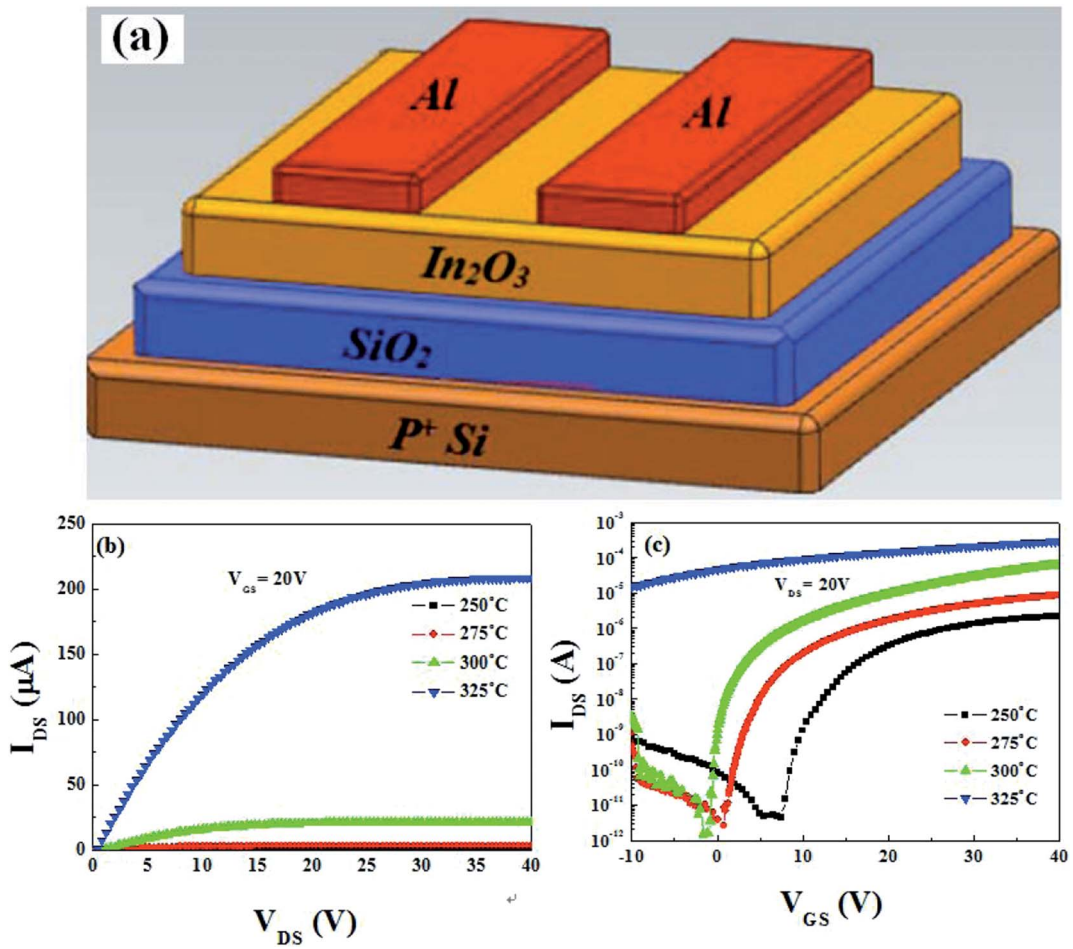

Fig. 8 (a) Schematic illustration of the bottom-gate and top-contact In_2O_3/SiO_2 TFTs. (b) and (c) Output and transfer characteristics of the In_2O_3/SiO_2TFTs.

$$D_{it} = \left[\frac{SS\log(e)}{kT/q} - 1\right]\frac{C_i}{q}$$

where k, T, and q are Boltzman's constant, absolute temperature, and charge quality, respectively. The D_{it} values of In_2O_3 TFTs annealed at 250, 275, 300, and 325 °C are calculated to be 1.35×10^{12}, 1.18×10^{12}, 4.60×10^{11}, and 2.62×10^{13} cm^{-2}, respectively. A large D_{it} has been observed in the 250 °C-annealed TFTs, which is attributed to the incomplete decomposition of residual organic groups and the existence of the defects states near In_2O_3/SiO_2 interface. Smallest D_{it} has been obtained for 300 °C-annealed sample, indicating the controllable growth of the interface layer and reduced trap states. However, for 325 °C-annealed TFTs, the sharp increased D_{it} has been observed. Okamura *et al.* have reported that the degraded surface morphology will lead to a rough interface and more interfacial trap states.[45] As a result, it can be inferred that the 325 °C-annealing increases the surface smooth and accelerates the uncontrollable growth of the interface layer. Therefore, the increased defect states will undoubtedly trap mobile carriers and degrade the performance parameter of TFTs.

From overall consideration of the electrical performance of the In_2O_3 TFTs, it can be concluded that the solution-derived In_2O_3 TFTs annealed at 300 °C exhibits the optimized electrical performance including a high μ_{sat} of 0.6 cm^2 V^{-1} s^{-1}, a high I_{on}/I_{off} value of 10^7, and a small SS value of 0.41 V dec^{-1}, respectively. However, due to the low dielectric constant of SiO_2 employed as candidate of gate dielectric in TFTs, all the as-fabricated TFTs devices operate at high voltages and hence increase the power consumption. To decrease the operation voltage and reduce the power consumption of solution-derived

Table 1 Electrical parameters of In_2O_3/SiO_2 annealed at various conditions

Sample	μ_{sat} [cm^2 V^{-1} s^{-1}]	I_{on}/I_{off}	V_{TH} [V]	SS [V dec^{-1}]	D_{it} [cm^{-2}]
In_2O_3-250/SiO_2	0.07	4.78×10^5	11.25	1.09	1.35×10^{12}
In_2O_3-275/SiO_2	0.13	3.30×10^6	5.56	0.96	1.18×10^{12}
In_2O_3-300/SiO_2	0.63	4.09×10^7	4.15	0.41	4.60×10^{11}
In_2O_3-325/SiO_2	Conductive	2.12×10	−22.92	20.00	2.62×10^{13}

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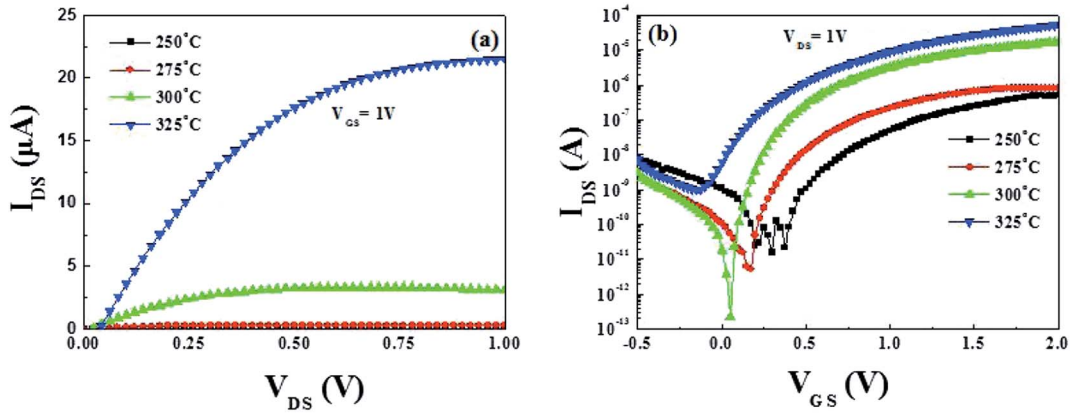

Fig. 9 Output and transfer characteristics of the In_2O_3/ZrO_x TFTs.

In_2O_3 TFTs, replacing SiO_2 with high-k gate dielectric should be explored.

3.6 Electrical properties of solution-processed In_2O_3/ZrO_x TFTs

Encouraged by the successful TFTs performance based on SiO_2 dielectric, the TFTs performance needs to be optimized further. To explore the possibility of the improvement of device performance, bottom-gated fully solution-derived TFTs combined with In_2O_3 channel and ZrO_x dielectric layer were fabricated. Based on previous investigation, 400 °C-annealed ZrO_x has been selected to act as the dielectric layer due to its relatively low leakage current and good dielectric properties. For the solution-derived In_2O_3 channel layer, 250–325 °C annealing temperature is still selected to pursue the optimized TFTs device performance.

The output curves of each TFT are shown in Fig. S2 (ESI†) and the summarized output curves of In_2O_3 TFTs at a V_{GS} of 1 V are demonstrated in Fig. 9a. It is noted that an ultra-low operating voltage of 2 V has been observed in ZrO_x-based TFTs. Based on our best knowledge, it is the lowest reported operating voltage for fully solution-derived In_2O_3 TFTs. As a result, the as-fabricated TFTs expend lower consumption compared to those TFTs based on conventional SiO_2 dielectrics, which is desirable for low-consumption electronics. Fig. 9b shows the corresponding transfer characteristics of In_2O_3 TFTs. Table 2 summaries all the electrical parameters of fully solution-derived In_2O_3 TFTs based on 400 °C-annealed ZrO_x dielectrics. It can be clearly seen that In_2O_3 TFTs annealed at 300 °C represents improved electrical performances, such as a high μ_{sat} of 4.42 $cm^2\ V^{-1}\ s^{-1}$, a low V_{TH} of 0.31 V, an large I_{on}/I_{off} of 7.5×10^7, a turn-on voltage of 0 V, and a small SS of 78.1 mV dec^{-1}. In addition, D_{it} is calculated to 5.2×10^{11} cm^{-2} for 300 °C-processed In_2O_3 TFTs. The as-calculated D_{it} is much lower than that of the reported TFTs based on solution-derived ZrO_x (8.7×10^{11} cm^{-2}),[16] sputtered AlO_x (1.1×10^{13} cm^{-2}),[46] spin-coated MgO (1.1×10^{13} cm^{-2}),[17] and water-induced ScO_x (1.1×10^{13} cm^{-2}).[26] Such a small D_{it} is not only beneficial to carrier transport in the interface region, but also to the operation stability. The small SS values for 300 °C-annealed TFTs may be attributed to the large areal capacitance of the ZrO_x dielectric layer and the electronic-clean interface between In_2O_3 and ZrO_x.[15,25] Based on the optimized electrical performance parameters, it can be noted that the μ_{sat} of In_2O_3 TFTs based on ZrO_x dielectric has been significantly enhanced by a factor of 7 compared to that of based on SiO_2 dielectric. The sharp increase in μ_{sat} comes from the electronic-free interface and high capacitance density of ZrO_x dielectric layer. According to the multiple-trap-and-release (MTR) model, Lee *et al.* have supposed that a higher electron mobility may originate from an increased gate capacitance, which stems from the larger dielectric constant of the gate dielectric relative to SiO_2.[47] The increase in gate capacitance causes electrons to rapidly fill the lower localized states between the energy gap, allowing additional induced electrons to occupy the upper localized states. As a result, electrons can easily jump into the nearby localized states along the percolating-conduction path, leading to the enhanced electron mobility.[24] Based on above analyses, it can be concluded that the optimized device performance for 300 °C-annealed In_2O_3 TFTs based on ZrO_x dielectric may be due to the smooth surface, the high capacitance of the ZrO_x dielectric, and/or the enhanced interface quality of In_2O_3/ZrO_x.

Table 2 Electrical parameters of In_2O_3/ZrO_x annealed at various conditions

Sample	μ_{sat} [$cm^2\ V^{-1}\ s^{-1}$]	I_{on}/I_{off}	V_{TH} [V]	SS [V dec^{-1}]	D_{it} [cm^{-2}]
In_2O_3-250/ZrO_x	0.18	2.27×10^4	0.56	0.11	2.13×10^{12}
In_2O_3-275/ZrO_x	0.32	1.61×10^5	0.34	0.082	7.25×10^{11}
In_2O_3-300/ZrO_x	4.42	7.50×10^7	0.31	0.078	5.21×10^{11}
In_2O_3-325/ZrO_x	11.32	5.50×10^4	−0.15	0.13	1.89×10^{12}

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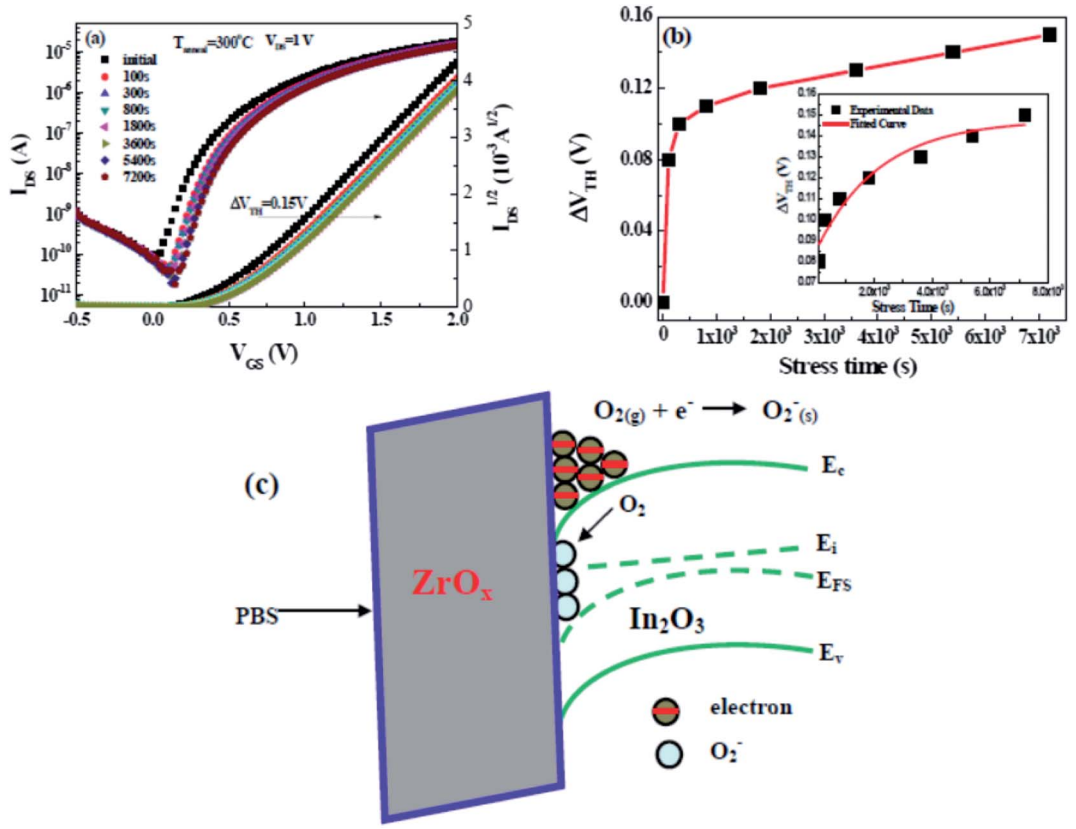

Fig. 10 (a) Transfer curves of 300 °C-annealed In_2O_3/ZrO_x TFT under PBS with a VG value of 2 V for 7200 s. (b) The V_{TH} shift as a function of stress time. The inset shows the time dependence of ΔV_{TH} in the In_2O_3 TFT with an ZrO_x gate dielectric under the bias-stress of 1 V. (c) The energy band diagram of the 300 °C-annealed In_2O_3/ZrO_x TFT under PBS.

In spite of the high saturation current and the large μ_{sat} for In_2O_3 TFTs annealed at 325 °C, it operates in the depletion mode with a negative of −0.15 V, which can be due to the high carrier concentration resulting from Fermi level approaching the conduction band minimum (CBM).[2] The high carrier concentration, as well as the increased interface defect states make it difficult to deplete In_2O_3 channel layer, leading to a negative V_{TH}, a high off current, and a low I_{on}/I_{off}. What's more, the corresponding D_{it} for 325 °C-annealed TFTs is calculated to be 1.89×10^{12} cm^{-2}, approaching nearly one magnitude larger than that of 300 °C-annealed TFTs. The small I_{on}/I_{off} value for 325 °C-annealed TFTs is mainly caused by the large off-state current (I_{off}), which will lead to the inevitable static power consumption and degrade device performance.[48] It is known that static power consumption is comparable to dynamic power in modern silicon chips or even become dominating in the future.[49] Therefore, the I_{off} has been regarded as a critical parameter to evaluate the power consumption of a device in modern integrated circuits.

Although solution-derived TFTs based on high-k gate dielectric have been previously achieved, there have been little reports on the investigation of their electrical stability under long-term bias stressing. To investigate the bias stability of the In_2O_3/ZrO_x TFT positive bias stress (PBS) tests were performed by applying a constant gate bias of 1 V while maintaining source and drain electrodes grounded. Fig. 10a displays the transfer curves with stress time intervals for 300 °C-annealed In_2O_3/ZrO_x TFT. The resulting V_{TH} *versus* stress time has been demonstrated in Fig. 10b. It can be seen that the 300 °C-annealed In_2O_3/ZrO_x TFT exhibits higher operation stability with a small threshold voltage shift (ΔV_{TH}) of 0.15 V up to 7200 s. The negligible change in the SS value reveals that there is no additional defect creation at the channel/dielectric interface during bias stressing.[29] The small ΔV_{TH} shift value reveals that there are a small number of defects at the In_2O_3/ZrO_x interface, which is consistent with previous D_{it} data. Based on the investigation from Jeong *et al.*, it can be noted that the interaction between the channel layer and oxygen from the ambient atmosphere determines the instability.[50] Testing PBS in the atmosphere, excess electrons will accumulate in the channel layer. The O_2 adsorption in the channel layer can deplete the electron carriers, leading to a positively shift of ΔV_{TH}.[29] The chemical reaction and the proposed band diagram are displayed in Fig. 10c.

The investigation of the time dependence of ΔV_{TH} can be used to confirm the dominant charge trapping mechanism causing the bias stress-induced ΔV_{TH} in TFTs.[51] From the inset plot shown in Fig. 10b, it can be noted that the time dependence of ΔV_{TH} in the In_2O_3 TFTs device follows a stretched exponential equation. This model is predictive of the voltage threshold shift for long stress durations of up to 2 h. This dependence is

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indicative of charge trapping phenomenon. The stretched exponential model of ΔV_{TH} is defined as[51]

$$\Delta V_{TH} = \Delta V_{TH_0}\left[1 - e^{-\left(\frac{t}{\tau}\right)^{\beta}}\right]$$

where ΔV_{TH_0} is the ΔV_{TH} right before the relaxation begins, τ is the characteristic detrapping time of carriers, and β is the stretched exponential exponent. The stretched exponential model well describes the measured ΔV_{TH}, which confirms our assumption that the charge trapping is the dominant mechanism of ΔV_{TH} in the ZrO_x/In_2O_3 interface. Similar results have been detected in InGaZnO-based TFTs.[51,52]

The achievement of the high-performance fully solution-derived In_2O_3 TFTs based on ZrO_x gate dielectric indicates the potential application of ZrO_x as an excellent high-k dielectric candidate, which represents a significant step towards the development of low-cost, low-power consumption, and large-area oxide flexible electronics. Although the progress made by integrating In_2O_3 channel layer with high-k gate dielectric, the processing temperature (400 °C) is somewhat beyond the limitation of flexible substrate. In addition, In_2O_3 and ZrO_x in current work has been obtained by conventional solution-based route, the use of toxic organic precursors has hindered its development. An eco-friendly, innovative and green synthetic route should be reconsidered. Currently, water-inducement route[15,23] and solution combustion synthesis process[53–55] have been adopted to success in reducing the processing temperature. Such process in under way.

4. Conclusions

In summary, we have demonstrated the solution-processed In_2O_3 thin films and explored its application possibility as channel layer in TFTs. The annealing temperature dependence on the electrical properties of In_2O_3 TFTs based on SiO_2 gate dielectric has been investigated. The optimized In_2O_3/SiO_2 TFTs annealed at 300 °C exhibit excellent electrical performance, including a μ_{sat} of 0.6 $cm^2\ V^{-1}\ s^{-1}$, a high I_{on}/I_{off} value of 10^7, V_{TH} of 4.15 V, and a small SS value of 0.41 V dec^{-1}, respectively. To verify the possible application of the ZrO_x thin films as dielectrics in low-temperature-processed CMOS logics, fully solution-derived In_2O_3/ZrO_x TFTs have been successfully fabricated to display a ultralow operating voltage of 2 V with optimized performance, including a high μ_{sat} of 4.42 $cm^2\ V^{-1}\ s^{-1}$, a low V_{TH} of 0.31 V, an large I_{on}/I_{off} of 7.5×10^7, a small SS of 78.1 mV dec^{-1}, an threshold voltage shift of 0.15 V under positive bias stress for 7200 s, respectively. As a result, it can be inferred that fully solution-based In_2O_3/ZrO_x TFTs have potential application as a promising alternative for low-cost, low-power consumption, and large-area oxide flexible electronics.

Conflicts of interest

The authors declare no competing financial interest.

Acknowledgements

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