



Cite this: *RSC Adv.*, 2019, 9, 9678

# Field-plate engineering for high breakdown voltage $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer field-effect transistors†

Jinho Bae,<sup>a</sup> Hyoung Woo Kim,<sup>b</sup> In Ho Kang<sup>b</sup> and Jihyun Kim<sup>\*a</sup>

The narrow voltage swing of a nanoelectronic device limits its implementations in electronic circuits. Nanolayer  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> has a superior breakdown field of approximately 8 MV cm<sup>-1</sup>, making it an ideal candidate for a next-generation power device nanomaterial. In this study, a field modulating plate was introduced into a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nano-field-effect transistor (nanoFET) to engineer the distribution of electric fields, wherein the off-state three-terminal breakdown voltage was reported to be 314 V.  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flakes were separated from a single-crystal bulk substrate using a mechanical exfoliation method. The layout of the field modulating plate was optimized through a device simulation to effectively distribute the peak electric fields. The field-plated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs exhibited n-type behaviors with a high output current saturation, exhibiting excellent switching characteristics with a threshold voltage of -3.8 V, a subthreshold swing of 101.3 mV dec<sup>-1</sup>, and an on/off ratio greater than 10<sup>7</sup>. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs with a high breakdown voltage of over 300 V could pave a way for downsizing power electronic devices, enabling the economization of power systems.

Received 15th February 2019  
 Accepted 16th March 2019

DOI: 10.1039/c9ra01163c

[rsc.li/rsc-advances](http://rsc.li/rsc-advances)

## Introduction

$\beta$ -Ga<sub>2</sub>O<sub>3</sub> is an attractive material for high-efficiency power devices owing to its ultra-wide energy bandgap (4.85 eV at room temperature), large breakdown field (approximately 8 MV cm<sup>-1</sup>), and excellent chemical and thermal stability.<sup>1,2</sup> Its Baliga's figure of merit is estimated to be 3214.1 times greater than that of Si, which surpasses that of conventional wide-bandgap materials such as GaN (846.0) and 4H-SiC (317.1), suggesting its great potential as a near-future power device material.<sup>3,4</sup> The commercial availability of a large single-crystal  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate at its early R&D stage makes it more competitive compared to III-nitride semiconductors, which have suffered from the absence of a commercial freestanding substrate. Many techniques of growing an epitaxial  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> layer have been previously reported, including metal organic chemical vapor deposition and molecular beam epitaxy (MBE), and pulsed laser deposition.<sup>5-9</sup> Thin film  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> power devices such as metal-oxide semiconductor field-effect transistors, Schottky diodes, and metal-semiconductor field-effect transistors (MESFETs) have demonstrated their potential as near-future, next-generation high-voltage electronic devices.<sup>10-15</sup> Yang *et al.* fabricated edge-defined film-fed grown (EFG) Si-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> thin-film vertical Schottky diodes with

a reverse breakdown voltage of ~2300 V.<sup>16</sup> Wong *et al.* demonstrated MBE-grown Si-implanted thin-film  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFET with a breakdown voltage of 755 V.<sup>17</sup>

Although  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is not a van der Waals material, it can be easily separated into a single-crystalline nanolayer *via* mechanical exfoliation owing to its large anisotropy in the monoclinic lattice constants ( $a$  [100] = 12.225 Å,  $b$  [010] = 3.039 Å, and  $c$  [001] = 5.801 Å). Mechanically exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer flakes feature a strain-free and flat surface with a high crystallinity maintained. Hwang *et al.* reported a quasi-two-dimensional (quasi-2D)  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> layer obtained through the mechanical exfoliation of a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> crystal, grown by the Czochralski method.<sup>18</sup> Kim *et al.* demonstrated quasi-2D  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFETs with a stable operation at a high temperature of 250 °C, where the Ga<sub>2</sub>O<sub>3</sub> was grown by the EFG method.<sup>19</sup> Zhou *et al.* fabricated FET devices with an on/off current ratio of 10<sup>10</sup> using Sn-doped  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flakes.<sup>20</sup> The exfoliated quasi-2D  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayers can be easily integrated with other 2D materials such as graphene, hexagonal boron nitride (h-BN), or transition metal dichalcogenides. The formation of a heterostructure by combining diverse nanolayers is intrinsically strain-free, *i.e.*, the high crystal quality of each layer is maintained. The integration of n-Ga<sub>2</sub>O<sub>3</sub> with a p-type 2D material, which is absent in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, can enable a versatile device configuration that facilitates p-n heterojunctions and bandgap engineering.<sup>21-23</sup> Kim *et al.* fabricated a 2D material-integrated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MOSFET by stacking h-BN on top of an exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer and analyzed the single- and dual-gate operations.<sup>24</sup> A  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> quasi-2D MESFET with a stepped-gate structure was demonstrated by using 2D h-BN as a dielectric layer.<sup>25</sup>

<sup>a</sup>Department of Chemical and Biological Engineering, Korea University, Anamdong-5-Ga, Seoul 02841, South Korea. E-mail: [hyunhyun7@korea.ac.kr](mailto:hyunhyun7@korea.ac.kr)

<sup>b</sup>Korea Electrotechnology Research Institute (KERI), Seongsan-gu, Changwon-si, Gyeongsangnam-do 51543, South Korea

† Electronic supplementary information (ESI) available: DC output characteristics of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs with and without the field-modulating plate and the materials parameters for the device simulations. See DOI: 10.1039/c9ra01163c



The premature electrical breakdown induced by the concentrated electric fields limits the device operation under a high bias voltage and threatens the device reliability. Various techniques, such as a field-modulating plate, a stepped gate, and a recess gate structure, have been introduced to ease the peak electric field and enhance the breakdown voltage for high-power electronics.<sup>26–30</sup> Among these, the field-modulating plate technique has been widely used owing to its efficacy and ease of fabrication. Studies have been conducted to increase the off-state electrical breakdown voltage using a gate or source field-plate, or multiple field-plates.<sup>31–33</sup> However, such methods are rarely studied in nanodevices despite their potential in power nanoelectronics. The integration of a field-modulating plate with a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer can miniaturize the power circuit system and simplify the layout. In this study, we optimized the structure of a field-modulating plate on a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET through electric field simulations. Based on them, we fabricated high breakdown voltage quasi-2D  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs. The structural and electrical properties of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs with a field-modulating plate were systematically investigated.

## Experimental details

A single crystalline  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> substrate (Tamura Corp.) with an effective carrier density of approximately  $3.5 \times 10^{17} \text{ cm}^{-3}$ , grown by the EFG method, was mechanically exfoliated into quasi-2D nanolayers using a commercial adhesive tape. The exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer flakes were transferred onto a thermally grown SiO<sub>2</sub> (300 nm)/Si (500  $\mu\text{m}$ ) substrate *via* a standard dry transfer method. Both the source and drain electrodes were defined using an electron beam lithography (EBL) technique, followed by Ti/Au (50 nm/100 nm) metal deposition using an electron-beam evaporator. The optimal design of a field-modulating plate, in order to distribute the localized peak electric field of a  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET device, was simulated using the device simulation software SILVACO Atlas. Rapid thermal annealing (Mila-5050, Ulvac Technologies, Inc.) under a low-vacuum condition (<10 mTorr) was performed at 500 °C for 1 min to improve the ohmic contact. The

top-gate electrode of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs was deposited with Ni/Au (50 nm/100 nm), which was defined by the EBL and electron beam evaporation procedures. A SiO<sub>2</sub> dielectric layer with a thickness of 200 nm was deposited using plasma-enhanced chemical vapor deposition (PECVD, VL-LA-PECVD, Unaxis), followed by the patterning of the field-modulating plate (Ti/Au (50 nm/100 nm)). The overall device fabrication process is shown in Fig. 1.

The surface morphology and thickness of the fabricated field-plated FET devices were characterized using atomic force microscopy (AFM; Innova, Bruker). Micro-Raman spectroscopy was used to analyze the structural properties of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flakes under a back-scattering geometry using a 532 nm wavelength line of a diode-pumped solid-state laser (Omicron). The cross-sectional device structure and crystal orientation of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> were investigated using scanning transmission electron microscopy (JEM-2100F, JEOL) after the specimen was prepared using the focused ion beam (FIB) technique (Quanta 3D FEG, FEI). The surface of the specimen was protected from FIB damage by a carbon layer. The electrical properties of the field-plated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFETs were monitored using an Agilent 4155C semiconductor parameter analyzer and 41501B single measurement unit expander connected to a probe station. The three-terminal off-state breakdown voltages of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> MESFETs were measured using a Keithley 6485 picoammeter connected with a Keithley 248 high-voltage supply. The fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs were immersed in a Fluorinert solution (FC-40, 3M) to prevent an unintended dielectric breakdown during the measurement of the three-terminal off-state breakdown voltage.

## Results and discussion

Prior to the device fabrication, the optimal field-modulating structure that can effectively distribute the concentrated electric fields was investigated in order to prevent a premature breakdown and maximize the off-state breakdown voltage of the fabricated nanoFET devices. A schematic of the simulated device structure and  $L_{FP}$  are presented in Fig. 2a. The simulations of electric field distribution were performed while varying

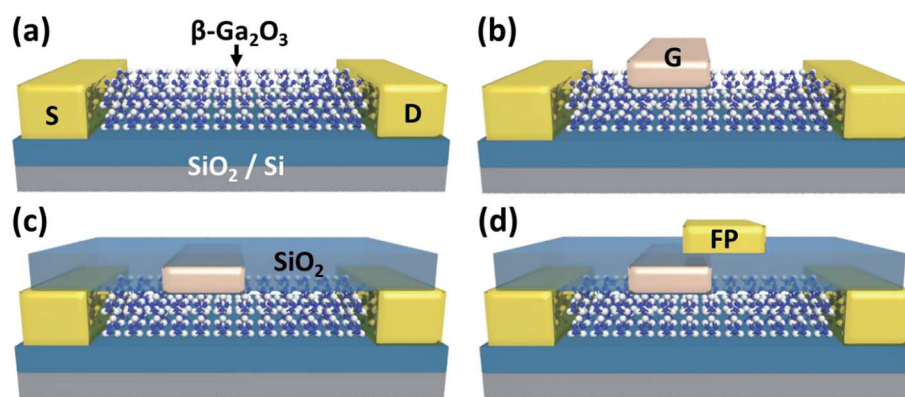


Fig. 1 Fabrication process of a top-gated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET with a field-modulating plate. (a) Patterning of the source and drain ohmic contacts to the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flake. (b) Deposition of the Ni/Au top gate electrode. (c) Deposition of the PECVD-SiO<sub>2</sub> dielectric layer. (d) Patterning of the field-modulating plate (Ti/Au).



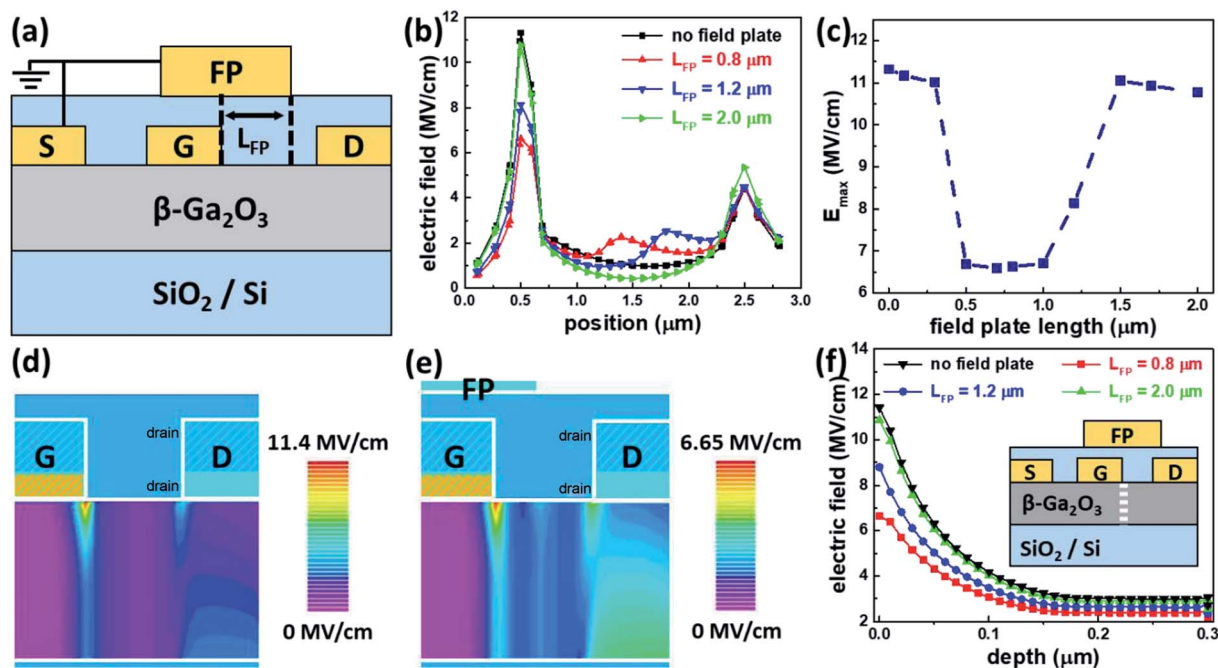


Fig. 2 (a) Schematic of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET with the field-modulating plate. (b) Simulation results of the electric field distribution between the gate and drain electrodes. (c) Maximum electric fields with varying field-plate lengths ( $L_{FP}$ ). Simulation results of the electric field distribution in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel (d) without and (e) with the field-modulating plate of  $L_{FP} \cong 0.8 \mu\text{m}$ . (f) Depth profile of the electric fields calculated along the dotted line in the inset figure at varying  $L_{FP}$ .

the length of the field-modulating plate from the edge of the gate electrode to the source-grounded field-plate electrode ( $L_{FP}$ ). Using the numerical device analysis, the electric field distributions, which varied with the  $L_{FP}$  under the conditions of  $V_{DS} = +400 \text{ V}$  and  $V_{GS} = -50 \text{ V}$ , are shown in Fig. 2b. The electric fields at the middle of the gate and drain electrodes were less than  $3 \text{ MV cm}^{-1}$ , which is much lower than the breakdown field of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> ( $\sim 8 \text{ MV cm}^{-1}$ ). However, the electric fields were much higher at the drain edge of the gate ( $x = 0.5 \mu\text{m}$ ) and the edge of the drain electrode ( $x = 2.5 \mu\text{m}$ ). Generally, the peak electric field was observed at the drain-side edge of the gate electrode due to the bias condition of the FET. Once defective sites are created under the intense electric fields, they will grow and damage the device. These high-intensity, highly localized electric fields can eventually destroy it.<sup>34,35</sup> Fig. 2b indicates the redistribution of the concentrated electric fields due to the presence of the field-modulating plate. In particular, at the drain-side edge of the gate electrode ( $x = 0.5 \mu\text{m}$ ), the electric field was greatly alleviated by introducing the source-grounded field-plate structure, which is consistent with the previous reports of AlGaAs/GaAs, AlGaN/GaN, and SiC devices. In AlGaAs/GaAs HEMTs, the peak electric field was lowered by employing the field-modulating plate.<sup>36</sup> Fig. 2c shows the maximum electric field values varying with  $L_{FP}$  and proposes that the layout optimized for the dispersion of the concentrated electric fields is  $L_{FP} \cong 0.8 \mu\text{m}$ , which decreases the peak electric field from  $11.4 \text{ MV cm}^{-1}$  to  $6.6 \text{ MV cm}^{-1}$ . The peak electric field ( $6.6 \text{ MV cm}^{-1}$ ) redistributed by the source-grounded field-modulating plate was lower than the intrinsic breakdown field ( $\sim 8 \text{ MV cm}^{-1}$ ) of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>, which can prevent a premature

electrical breakdown during device operation and help to improve the device reliability. Fig. 2d and e compare the electric field distribution in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel layer without and with a field-modulating plate, respectively. Fig. 2f shows the depth profile of the electric field in the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel that varies with  $L_{FP}$ . The electric field at the hot gate edge which is located in the drain-side gate edge was greatly mitigated by the introduction of field-modulating plate, enhancing the off-state breakdown voltage of the FET device.

Exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer MESFETs with a source-grounded field-plate were fabricated based on the optimized length of the field-modulating plate electrode ( $L_{FP} = 0.8 \mu\text{m}$ ). The optical microscopic image (Fig. 3a) and AFM image (Fig. 3b) confirm that the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs were fabricated using the same layout as that suggested by the above electric field simulation. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flakes used in this study had a thickness ranging from 200 to 350 nm with a root-mean-square roughness of approximately 1.3 nm (Fig. 3b), which is consistent with the result of the cross-sectional high-resolution TEM image (Fig. 3c). PECVD SiO<sub>2</sub> conformally covered the Ni/Au top gate electrode. On top of the PECVD SiO<sub>2</sub> layer, the Ti/Au field-plate electrodes were seamlessly defined with the optimized  $L_{FP}$  ( $0.8 \mu\text{m}$ ). A clear boundary was maintained between each layer without interdiffusion after the device fabrication process, as in Fig. 3c, which indicates the robustness of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer. The Raman spectrum of the fabricated nanoFETs is shown in Fig. 4a. No change in the Raman mode was observed after the device fabrication process, which also indicates the chemical and mechanical stability of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanolayer.<sup>37</sup> The high crystallinity of the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flake is also





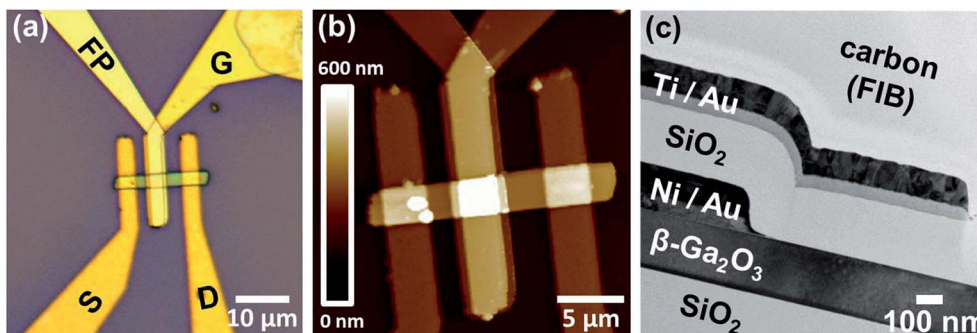


Fig. 3 (a) Optical microscope image, (b) AFM image, and (c) cross-sectional high-resolution TEM image of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET with the field-modulating plate. Note that a carbon layer was deposited to protect the specimen from FIB damage.

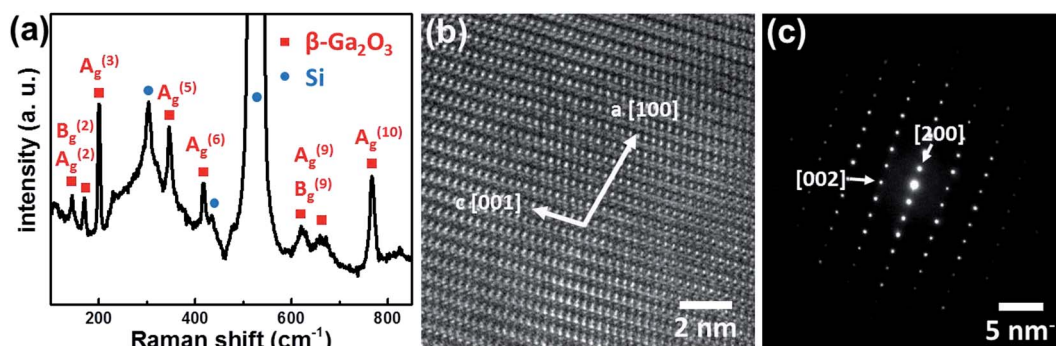


Fig. 4 (a) Raman spectrum of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET with the field-modulating plate. (b) Cross-sectional high-resolution TEM image and (c) SAED pattern of the mechanically exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flake.

confirmed by the TEM image (Fig. 4b) and the selected area electron diffraction (SAED) pattern (Fig. 4c). The  $d$ -spacing in the SAED pattern was 0.609 nm, which matches the (200) lattice plane. This indicates that the mechanically exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flake was separated along the (100) direction due to the large anisotropy of the monoclinic  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> unit cell, even though  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> is not a van der Waals material.

Eight  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs, each with a source-grounded field-plate, were fabricated. The electrical properties of the representative device are shown in Fig. 5. For comparison, the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET without the field plate was characterized, where

the current density of the field-plated FETs was lower than that of the non-field-plated FETs because the voltage on the field plate competed with that on the gate electrode (Fig. S1†). They exhibited excellent DC output characteristics at varying  $V_{GS}$  (Fig. 5a). The fabricated device showed n-type characteristics and was completely pinched off at a  $V_{GS}$  of approximately  $-5$  V. They showed a linear increase in the  $I_{DS}$  under low-voltage operation below the knee voltage, and output currents were saturated above the knee voltage. Considering that conventional 2D material-based electronic devices suffer from the absence of output current saturation, the saturated output

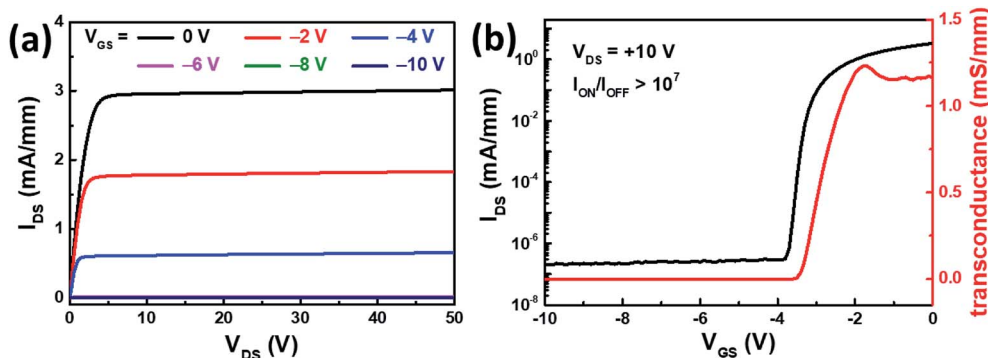


Fig. 5 (a) DC output and (b) transfer/transconductance characteristics of the representative  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET with the field-modulating plate at varying  $V_{GS}$ .



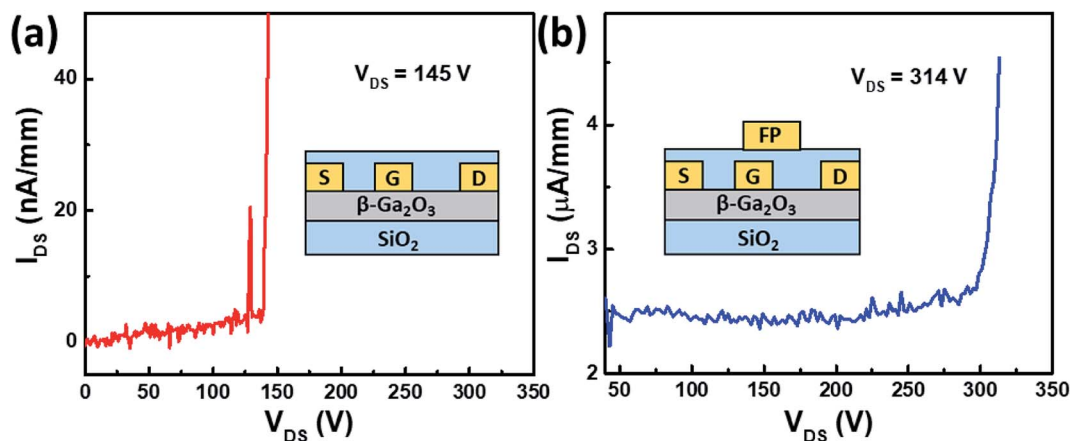


Fig. 6 Off-state three-terminal hard-breakdown results of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET (a) without and (b) with the source-connected field-modulating plate. The insets show the schematics of each device.

current in  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs show a potential for a nano-electronic power amplifier. They also exhibited reproducible electrical characteristics without a significant change under the repeated driving conditions of  $V_{DS} = +50$  V. By contrast, 2D-material based electronic devices using graphene, black phosphorus, and transition metal dichalcogenides cannot withstand the high bias conditions used in our measurements of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> devices. Fig. 5b shows the transfer and transconductance characteristics of the fabricated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> device. The field-effect mobility ( $\mu_{FE}$ ) was estimated to be  $3.1 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which was calculated by the following equation:

$$\mu_{FE} = \frac{g_{\max} L}{q(N_d - N_a)dW}$$

where  $g_{\max}$  is the maximum transconductance,  $L$  is the length,  $W$  is the width,  $d$  is the thickness of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel, respectively,  $q$  is the elementary charge, and  $(N_d - N_a)$  is the effective carrier concentration of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> channel. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs showed a threshold voltage ( $V_{th}$ ) of  $-3.8$  V and a subthreshold swing (SS) value of  $101.3 \text{ mV dec}^{-1}$ , where the PECVD SiO<sub>2</sub> served as both the surface passivation layer for the exfoliated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> and the dielectric layer for the field-modulating plate. Considering that the previous SS of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub>-based device was  $\sim 140 \text{ mV dec}^{-1}$ , the lower SS combined with a high on/off ratio ( $>10^7$ ) can promise to minimize the power switching loss.

The three-terminal off-state hard-breakdown voltages of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFETs with and without a field-modulating plate are compared in Fig. 6a and b. The three-terminal off-state breakdown voltages were measured under the pinched-off condition. The devices under the test were immersed in Fluorinert solution to prevent unintentional dielectric breakdown due to ambient molecules, which is a standard test condition in power electronics. A high electric field can initiate carrier multiplication through impact ionization, where the accelerated carriers collide with the lattice and release their kinetic energy. The cascade creations of electron-hole pairs will result in high off-state currents, which will catastrophically damage the device. The impact ionization coefficients of  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> were estimated to be

approximately  $6.1 \times 10^4 \text{ cm}^{-1}$  and  $9.5 \times 10^3 \text{ cm}^{-1}$  at the peak electric fields of  $11.4 \text{ MV cm}^{-1}$  (without field-modulating plate) and  $6.6 \text{ MV cm}^{-1}$  (with field-modulating plate), which are much lower than those of 4H-SiC ( $1.7 \times 10^6$ ) and GaN ( $1.8 \times 10^4$ ) at electric fields of  $6.6 \text{ MV cm}^{-1}$ .<sup>38</sup> The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> shows a lower impact ionization coefficient under the same electric field due to its high bond strength of the binding energy of Ga-O ( $\sim 531$  eV (O1s)), much larger than that of Ga-N ( $\sim 397$  eV (N1s)) and Si-C ( $\sim 283$  eV (C1s)). The breakdown field is generally proportional to  $(\text{energy bandgap})^{2-2.5}$ .<sup>2</sup> This can reduce the off-state leakage currents and ensure a high hard-breakdown voltage. The hard-breakdown voltage of the field-plated  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET was 314 V (Fig. 5b), while the hard-breakdown voltage of the  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET without the field-modulating plate (Fig. 5a) was observed at  $V_{DS} = 145$  V. The two-fold increase of the hard-breakdown voltage is attributed to the existence of the field-modulating plate, which is consistent with the simulation results. The high off-state breakdown voltage of 314 V is much higher than those of conventional 2D devices (MoS<sub>2</sub>, 120 V) and wide-bandgap GaN nanowire device (140 V), opening a new route for next-generation high-power nanoelectronics with wide voltage swing.

## Conclusion

A  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> nanoFET with an off-state hard-breakdown voltage of 314 V was fabricated by introducing a source-grounded field-modulating plate. The numerical device simulation was employed to analyze the effects of the field-modulating plate and determine the optimal structure to effectively distribute the electric fields concentrated on the hot gate edge. The  $\beta$ -Ga<sub>2</sub>O<sub>3</sub> flakes, which were mechanically exfoliated from a single-crystal bulk substrate, was used as a n-channel layer with their crystallinity maintained. The fabricated nanoFET device showed excellent device characteristics including low SS and high on/off ratio with a high off-state hard-breakdown voltage (314 V). Engineering of the peak electric fields in a nanodevice by using a field-modulating plate improved the device stability under a high-voltage operation, paving the way for high-efficiency integrated power nanoelectronic systems.



## Conflicts of interest

There are no conflicts to declare.

## Acknowledgements

The research at Korea University was supported by the New & Renewable Energy Core Technology Program of Korea Institute of Energy Technology Evaluation and Planning (KETEP), which was granted financial resources from the Ministry of Trade, Industry & Energy, Korea (No. 20172010104830) and the Technology Development Program to Solve Climate Changes of the National Research Foundation (NRF) funded by the Ministry of Science and ICT (NRF-2017M1A2A2087351).

## References

- M. A. Mastro, A. Kuramata, J. Calkins, J. Kim, F. Ren and S. Pearton, *ECS J. Solid State Sci. Technol.*, 2017, **6**, P356.
- S. Pearton, F. Ren, M. Tadjer and J. Kim, *Appl. Phys. Rev.*, 2018, **124**, 220901.
- B. J. Baliga, *IEEE Electron Device Lett.*, 1989, **10**, 455.
- S. Pearton, J. Yang, P. H. Cary IV, F. Ren, J. Kim, M. J. Tadjer and M. A. Mastro, *Appl. Phys. Rev.*, 2018, **5**, 011301.
- A. Kuramata, K. Koshi, S. Watanabe, Y. Yamaoka, T. Masui and S. Yamakoshi, *Jpn. J. Appl. Phys.*, 2016, **55**, 1202A1202.
- Y. Lv, J. Ma, W. Mi, C. Luan, Z. Zhu and H. Xiao, *Vacuum*, 2012, **86**, 1850.
- S. Rafique, L. Han, M. J. Tadjer, J. A. Freitas Jr, N. A. Mahadik and H. Zhao, *Appl. Phys. Lett.*, 2016, **108**, 182105.
- K. Sasaki, A. Kuramata, T. Masui, E. G. Villora, K. Shimamura and S. Yamakoshi, *Appl. Phys. Express*, 2012, **5**, 035502.
- F. Zhang, K. Saito, T. Tanaka, M. Nishio and Q. Guo, *J. Cryst. Growth*, 2014, **387**, 96.
- M. Higashiwaki, K. Sasaki, A. Kuramata, T. Masui and S. Yamakoshi, *Appl. Phys. Lett.*, 2012, **100**, 013504.
- M. Higashiwaki, K. Sasaki, T. Kamimura, M. Hoi Wong, D. Krishnamurthy, A. Kuramata, T. Masui and S. Yamakoshi, *Appl. Phys. Lett.*, 2013, **103**, 123511.
- M. J. Tadjer, N. A. Mahadik, V. D. Wheeler, E. R. Glaser, L. Ruppalt, A. D. Koehler, K. D. Hobart, C. R. Eddy Jr and F. J. Kub, *ECS J. Solid State Sci. Technol.*, 2016, **5**, P468.
- S. Ahn, F. Ren, L. Yuan, S. Pearton and A. Kuramata, *ECS J. Solid State Sci. Technol.*, 2017, **6**, P68.
- Z. Hu, K. Nomoto, W. Li, L. J. Zhang, J.-H. Shin, N. Tanen, T. Nakamura, D. Jena and H. G. Xing, *Device Research Conference*, 2017.
- J. Yang, S. Ahn, F. Ren, R. Khanna, K. Bevlín, D. Geerapuram, S. Pearton and A. Kuramata, *Appl. Phys. Lett.*, 2017, **110**, 142101.
- J. Yang, F. Ren, M. Tadjer, S. Pearton and A. Kuramata, *ECS J. Solid State Sci. Technol.*, 2018, **7**, Q92.
- M. H. Wong, K. Sasaki, A. Kuramata, S. Yamakoshi and M. Higashiwaki, *IEEE Electron Device Lett.*, 2016, **37**, 212.
- W. S. Hwang, A. Verma, H. Peelaers, V. Protasenko, S. Rouvimov, H. Xing, A. Seabaugh, W. Haensch, C. V. de Walle and Z. Galazka, *Appl. Phys. Lett.*, 2014, **104**, 203111.
- J. Kim, S. Oh, M. A. Mastro and J. Kim, *Phys. Chem. Chem. Phys.*, 2016, **18**, 15760.
- H. Zhou, M. Si, S. Alghamdi, G. Qiu, L. Yang and P. Ye, *IEEE Electron Device Lett.*, 2017, **38**, 103.
- J. Kim, M. A. Mastro, M. J. Tadjer and J. Kim, *ACS Appl. Mater. Interfaces*, 2018, **10**, 29724.
- G. Shin, H. Y. Kim and J. Kim, *Korean J. Chem. Eng.*, 2018, **35**, 574.
- S. Nakagomi, T. Sakai, K. Kikuchi and Y. Kokubun, *Phys. Status Solidi A*, 2018, 1700796.
- J. Kim, M. A. Mastro, M. J. Tadjer and J. Kim, *ACS Appl. Mater. Interfaces*, 2017, **9**, 21322.
- J. Bae, H. W. Kim, I. H. Kang, G. Yang and J. Kim, *Appl. Phys. Lett.*, 2018, **112**, 122102.
- Y. Ando, Y. Okamoto, H. Miyamoto, T. Nakayama, T. Inoue and M. Kuzuhara, *IEEE Electron Device Lett.*, 2003, **24**, 289.
- Y. Okamoto, Y. Ando, K. Hataya, T. Nakayama, H. Miyamoto, T. Inoue, M. Senda, K. Hirata, M. Kosaki and N. Shibata, *IEEE Trans. Microwave Theory Tech.*, 2004, **52**, 2536.
- H. Xing, Y. Dora, A. Chini, S. Heikman, S. Keller and U. K. Mishra, *IEEE Electron Device Lett.*, 2004, **25**, 161.
- C. Gaquiere, B. Bonte, D. Theron, Y. Crosnier, P. Arsene-Henri and T. Pacou, *IEEE Trans. Electron Devices*, 1995, **42**, 209.
- T. Suemitsu, H. Yokoyama, T. Ishii, T. Enoki, G. Meneghesso and E. Zanoni, *IEEE Trans. Electron Devices*, 2002, **49**, 1694.
- R. Chu, A. Corrión, M. Chen, R. Li, D. Wong, D. Zehnder, B. Hughes and K. Boutros, *IEEE Electron Device Lett.*, 2011, **32**, 632.
- W. Saito, Y. Takada, M. Kuraguchi, K. Tsuda, I. Omura, T. Ogura and H. Ohashi, *IEEE Trans. Electron Devices*, 2003, **50**, 2528.
- J. Li, S. Cai, G. Pan, Y. Chen, C. Wen and K. Wang, *Electron. Lett.*, 2001, **37**, 196.
- W. R. Frensley, *IEEE Trans. Electron Devices*, 1981, **28**, 962.
- B. J. Baliga, *Semicond. Sci. Technol.*, 2013, **28**, 074011.
- A. D. Rawal, S. Sharma, S. Kapoor, R. Liashram, R. K. Chaubey, S. Vinayak and R. K. Sharma, *Def. Sci. J.*, 2018, **68**, 290.
- C. Kranert, C. Sturm, R. Schmidt-Grund and M. Grundmann, *Sci. Rep.*, 2016, **6**, 35964.
- K. Ghosh and U. Singiseti, *J. Appl. Phys.*, 2018, **124**, 085707.

