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Approaching subthreshold-swing limit for thin-film transistors by using a giant-dielectric-constant gate dielectric†

Zhuo Chen, Linfeng Lan * and Junbiao Peng

Low-temperature giant-dielectric-constant thin films ($In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$) fabricated with simple radio frequency (RF) sputtering on glass substrates are employed as the gate dielectrics for thin-film transistors (TFTs) for the first time. The 380 nm-thick $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film exhibited a quasi-static capacitance of as high as 36 156 nF cm^{-2} with a quasi-static permittivity of 15 525 (and 7607 nF cm^{-2} at 1 kHz). Indium zinc oxide (IZO) TFTs with $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate dielectrics exhibited high output current at low operation voltage and little hysteresis in the transfer curves between forward and reverse sweeps. The subthreshold swing (SS) of the IZO TFTs is 0.068 V dec^{-1}, very close to the lowest limit of the SS of the field-effect transistors (0.06 V dec^{-1}). The results also proves that the lowest limit of the SS (0.06 V dec^{-1}) cannot be broken no matter how high the gate dielectric capacitance is (except for negative capacitors). The TFTs demonstrate the potential for the applications in low-power circuits or flat-panel displays.

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1. Introduction

The gate dielectric is important for a thin-film transistor (TFT), because the performance of the TFT device is affected by the interface/bulk traps, interface coupling, dielectric constant, leakage current, and breakdown field of the gate dielectric. For applications in active-matrix (AM) displays, especially for the AM organic light-emitting diode (OLED) displays, TFTs should be of high output current at relatively low operation voltage to meet the driving current of the OLEDs and reduce the power consumption. In AMOLEDs, the total power consumption (P_{total}) of each pixel mainly depends on the OLED power consumption (P_{OLED}) and the TFT power consumption (P_{TFT}):

$$P_{total} \approx \eta_{video} \times (P_{OLED} + P_{TFT}) \propto (V_{OLED} + V_{TFT}) \quad (1)$$

where η_{video} is the percentage of on state of the pixels during the video operation, V_{OLED} is the voltage drop of the OLED, and V_{TFT} is the voltage drop of the TFT. It has been reported that P_{TFT} can be greater than 50% of P_{total} when the mobility is lower than 5 $cm^2\ V^{-1}\ s^{-1}$.[1] Therefore, reducing the operation voltage of TFTs is an effective way for reducing the power consumption for AMOLEDs.

As known, the operation voltage of TFTs is determined by subthreshold swing (SS), which is defined as the change in gate voltage (V_G) required for one order change in the drain current (I_D). TFTs with lower SS usually have lower operation voltage. To lower the operation voltage and SS, fabricating TFTs with high-capacitance gate dielectric is the topic intriguing researchers in the industry and academia. Generally, there are two ways to increase the capacitance of the gate dielectrics—reducing the thickness or increasing the dielectric constant (k) of the gate dielectrics. For practical application to active-matrix displays, the thickness of the gate dielectrics of TFTs should be greater than 200 nm to avoid electrical breakdown in the whole panel. In this case, further reducing the dielectric thickness to less than 200 nm would risk increasing of defects in the displays. Therefore, employing high dielectric constant dielectrics to increase the capacitance is preferred. Various high-k dielectric materials have been applied to TFTs, such as HfO_2, Al_2O_3 and *etc.*[2,3] However, the dielectric constants of most of the high-k materials are less than 40. So these materials have a limited effect of reducing the operating voltage of the transistors.

At the same time, some research teams employed ferroelectrics as the gate dielectrics,[4,5] such as $BaTiO_3$ (BTO, $k_{bulk} \sim 10^3$; $k_{film} \sim 500$), $Pb(Zr,Ti)O_3$ (PZT, $k_{bulk} \sim 10^3$; $k_{film} \sim 800$) and *etc.*[6–9] However, the dielectric constant of the spontaneous-polarization ferroelectrics relies seriously on the temperature and the electric field applied to the ferroelectrics, causing uncertain response when writing data signal to the TFTs.

Recently, a new type of transistors, named electric-double-layer (EDL) transistors, have been investigated as a candidate for low-voltage application by using polymer electrolytes or

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† Electronic supplementary information (ESI) available: (1) Histograms of the (a) mobility and (b) threshold voltage of the IZO-TFT with the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate dielectric. (2) The enlarge transfer curves of Fig. 10b. (3) The variations of time-dependent transfer curves of the IZO-TFT with the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ insulator under negative gate bias stress. See DOI: 10.1039/c9ra03574e.

ionic liquids as gate dielectrics.[10–12] In such transistors, a high gate capacitance can be obtained by mobile ions that are able to move to form EDL, whose capacitance can be higher than 1 μF cm^{-2} at low frequency. However, the speed of the ions is usually too slow for active-matrix displays, whose frame rate is ~50–500.

In 2000, Subramanian *et al.* found the "giant dielectric behaviour" ($k_{bulk} > 10^4$) in $CaCu_3Ti_4O_{12}$ ceramics,[13] which triggers a large number of studies on giant dielectric materials, *e.g.*, $A_{2/3}Cu_3Ti_4O_{12}$ (A = Bi, La, Y), (Li, Ti) co-doped NiO, (In, Nb) co-doped TiO_2 (k_{bulk} ~10^4; k_{film} ~4000), *etc.*[14–18] However, attaining "giant dielectric" phase requires well-controlled deposition processes, specify substrates, and high annealing temperature (>1000 °C), which is beyond the upper limit of glass substrates for TFTs.

In this paper, we demonstrate low-temperature (400 °C) giant-dielectric-constant thin films ($In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$) fabricated with simply radio frequency (RF) sputtering method for the gate dielectrics of the indium–zinc-oxide (IZO) TFTs on glass substrates. The 380 nm-thick $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film exhibited a capacitance of as high as 7607 nF cm^{-2} with a permittivity of 3266 at 1 kHz. IZO-TFTs with $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate dielectrics exhibited high output current at low operation voltage and little hysteresis in the transfer curves between forward and reverse sweeps.

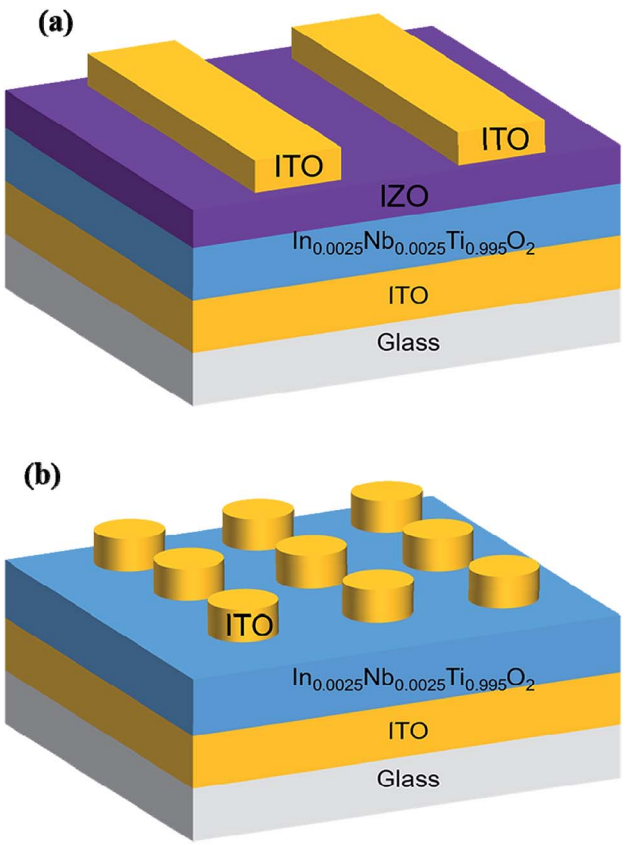

Fig. 1 Schematic structures of (a) the TFT with $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate insulator and (b) the capacitors with ITO/$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/ITO stacks.

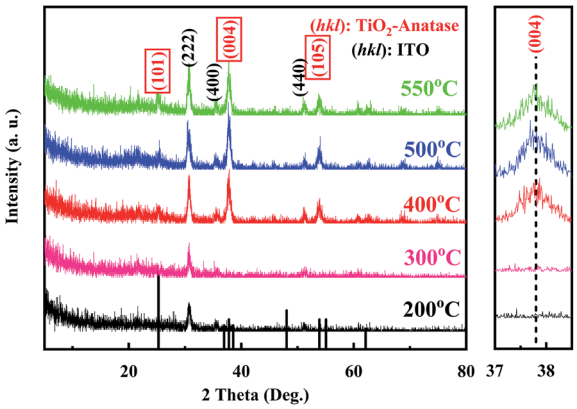

Fig. 2 XRD patterns of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ films on ITO/glass substrates annealing at 200 °C, 300 °C, 400 °C, 500 °C and 550 °C.

The micro structures and the mechanisms of the giant dielectric behaviour at low annealing temperature were discussed.

2. Experimental

2.1. Device preparation

The device structure of the IZO TFTs is shown in Fig. 1a. A layer of 150 nm-thick indium–tin-oxide (ITO, In : Sn = 9 : 1) gate electrode was fabricated on a glass substrate by direct current sputtering. Then, a layer of 380 nm-thick $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film acting as the gate dielectric layer was deposited by RF magnetron sputtering with the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ ceramics target under argon pressure of 0.5 Pa, and annealed in air at 400 °C for 30 minutes. The IZO (In : Zn = 2 : 1) semiconductor layer was deposited onto the gate dielectric layer by RF magnetron sputtering and annealed in air at 300 °C for 30 minutes. For the source and drain electrodes, a layer of 110 nm-thick ITO was deposited through a shadow mask, defining a channel width/length of 800/200 μm. Finally, the

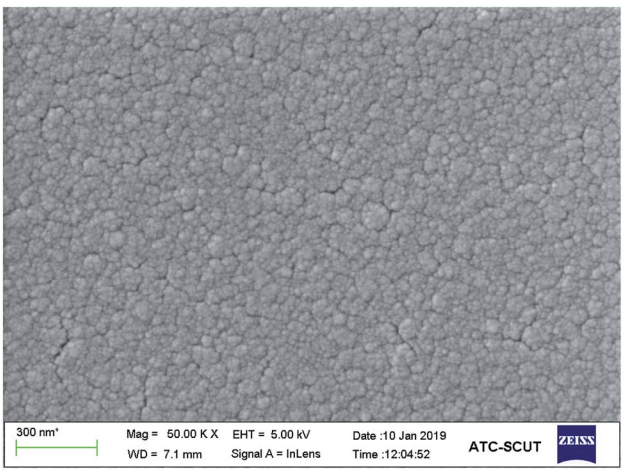

Fig. 3 SEM image of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film on ITO/glass substrates annealed at 400 °C for 30 minutes.

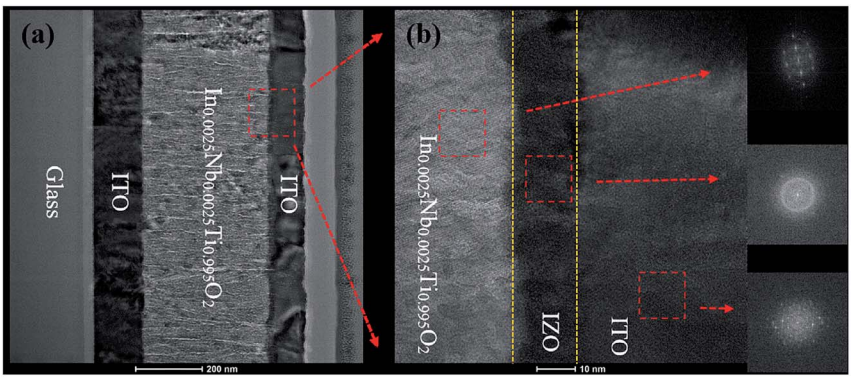

Fig. 4 (a) Cross-sectional STEM image of the Glass/ITO/$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/IZO/ITO sample annealed at 400 °C for 30 minutes; (b) the HR-TEM image of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/IZO/ITO region; the insets of (b) is the FFTs of the region of $In_{0.0025}Nb_{0.0025}Ti_{0.995}O$, IZO and ITO.

TFTs were annealed in air at 300 °C for 30 minutes. In addition, the metal–insulator–metal (MIM) capacitors were fabricated (see Fig. 1b).

2.2. Characterization

The $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film structure and morphology were characterized by X-ray diffraction (XRD, Bruker D8 ADVANCE) and scanning electron microscopy (SEM, Zeiss Merlin), respectively. The chemical valence of each element of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film was characterized by X-ray photoelectron spectroscopy (XPS, Thermo Fisher Scientific Inc, ESCALAB 250Xi), and the spectra were calibrated with the C 1s peak (at 284.8 eV). Transmission electron microscopy (TEM, FEI Titan Themis 200) specimens of the TFT device was prepared by focused ion beam (FIB, HELIOS NANOLAB 450S). The electrical performance of the TFTs and the MIM capacitors were measured by semiconductor parameter analyzer (Keysight B1500A).

3. Results and discussion

Fig. 2 shows XRD patterns of $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ films on the ITO/glass substrates at different annealing

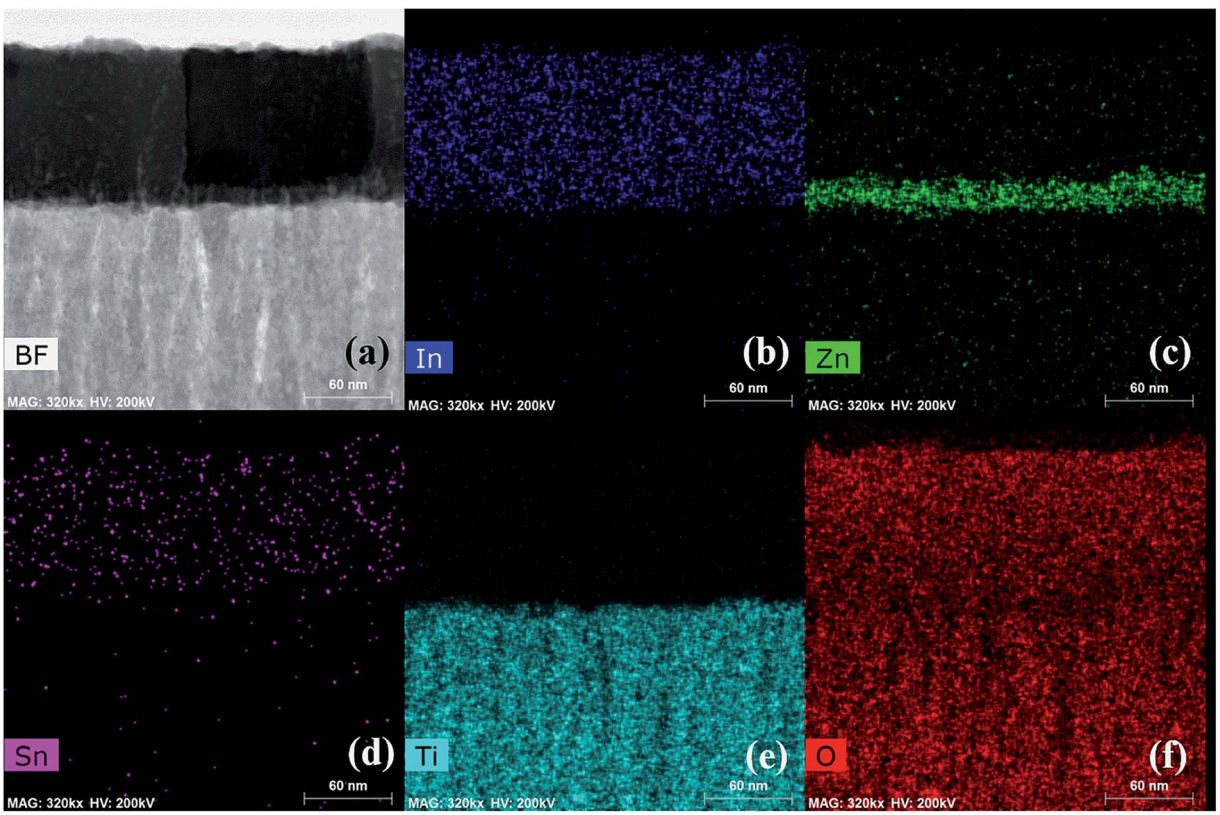

Fig. 5 (a) HAADF STEM images with elemental distribution detected by EDS for (b) In, (c) Zn, (d) Sn, (e) Ti, (f) O.

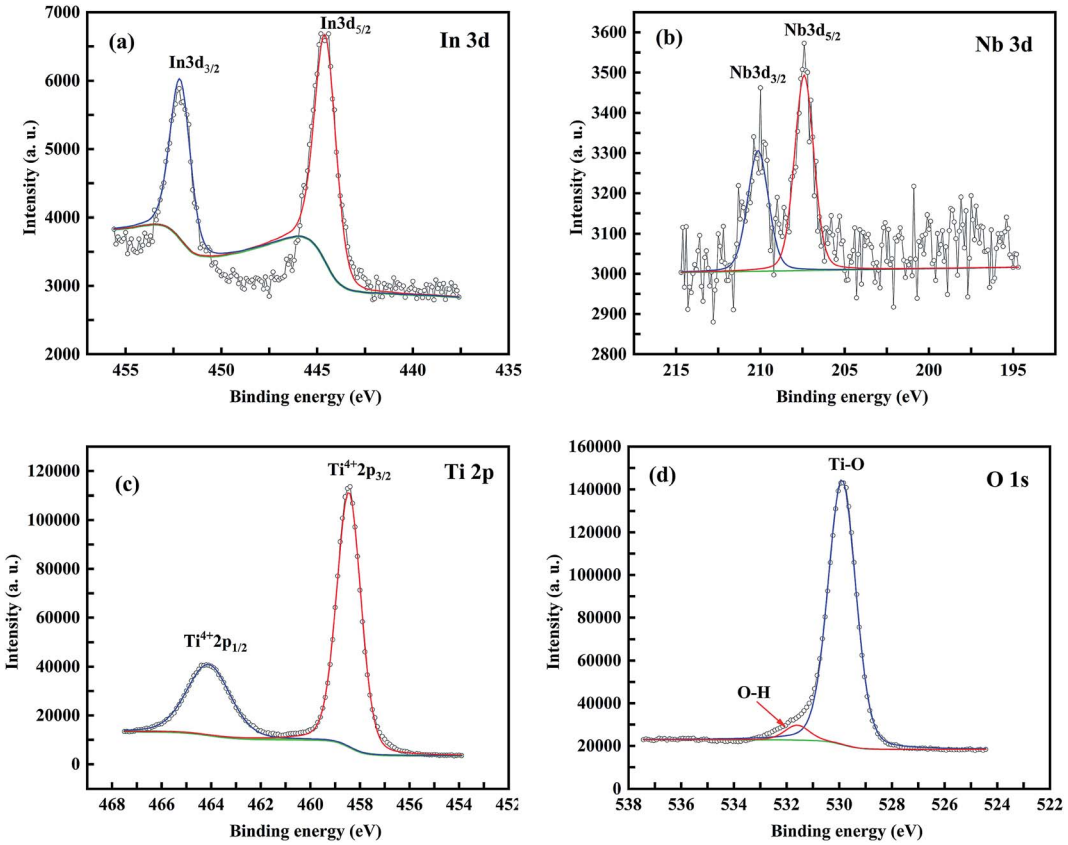

Fig. 6 XPS spectra of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ films on ITO/glass substrates annealed at 400 °C for 30 minutes, including: (a) In 3d, (b) Nb 3d, (c) Ti 2p, (d) O 1s.

temperatures. The black strips at the bottom of Fig. 2 are the diffraction peaks for the standard anatase phase. For the films annealed at 200 °C and 300 °C, the diffraction peaks of anatase phase could hardly be found, indicating that the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ films were amorphous. When the annealing temperature increase to 400 °C, the peaks of TiO_2-anatase phase (including (101), (004), and (105))[19] were observed, indicating that the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ films begin to crystallize. The strongest diffraction peak for the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ films was peak (004), which was the third strongest diffraction peak for the standard anatase phase, indicating that the films crystallized with high *c*-axis orientation. The average crystalline sizes for the films annealing at 400 °C, 500 °C, 550 °C, were calculated to be about 15.2 nm, 16.5 nm and 17.4 nm, respectively, by using the Scherer equation. The diffraction peaks (including (222), (400), (440))[20] of the In_2O_3 bixbyite phase were seem at the annealing temperature of 200 °C, showing that the ITO films were easily to be crystallized even at low annealing temperature. The SEM image (Fig. 3) also showed that the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film annealed at 400 °C were in polycrystalline state, which was consistent with the Fast Fourier Transform (FFT) patterns of the high-resolution transmission electron microscopy (HR-TEM) as discussed below.

Fig. 4a shows the scanning transmission electron microscopy (STEM) result of the cross-section of the glass/ITO/$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/IZO/ITO structure. Fig. 4b shows the HR-TEM image and the FFT patterns of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/IZO/ITO region in Fig. 4a. It was found that both of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ and ITO layers were crystallized, while the IZO film was in amorphous state. Fig. 5a–e show the high-angle annular dark-field (HAADF) STEM and elements distribution map obtained from energy-dispersion X-ray spectroscopy (EDS) of the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/IZO/ITO region. It could be seen that the elements were distributed uniformly in each film without segregated clusters. Because the signals of the elements (In and Nb) are too weak to be detected by EDS, they were characterized by XPS, as shown in Fig. 6a and b. The binding energies of In 3d electrons are 452.4 eV and 444.6 eV for $3d_{3/2}$ and $3d_{5/2}$, respectively,[21] while the binding energies of Nb 3d electrons are 210.1 eV and 207.3 eV for $3d_{3/2}$ and $3d_{5/2}$, respectively. And the spin orbit splitting between the Nb $3d_{3/2}$ and $3d_{5/2}$ was 2.8 eV, showing that the valence of Nb in the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ was +5.[22] Fig. 6c shows the binding energy spectra for the Ti 2p electrons (464.10 eV and 458.45 eV are for $2p_{1/2}$ and $2p_{3/2}$, respectively).[22,23] The doublet separation of Ti $2p_{1/2}$ and $2p_{3/2}$ peaks was 5.65 eV, which shows that the Ti^{4+} was the main state. Fig. 6d shows the XPS spectra for O 1s. The peak at 529.84 eV

was related to the Ti–O bonds while the peak at 531.4 eV was related to the oxygen vacancies or hydroxyl (OH) groups.[24] The results indicate that $[Ti^{4+}\cdot e - V_o^{\cdot\cdot} - Ti^{4+}\cdot e]$-related defects can be formed.[17] However, no peaks related to Ti^{3+} was observed. It means that the giant dielectric behaviour of $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ was not due to the electron hoping between Ti^{4+} and Ti^{3+}, which will be discussed later.

Fig. 7a shows the frequency dependences of capacitance and permittivity of the ITO/$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/ITO capacitors. The areal capacitance (C_i) was as high as 7607 nF cm^{-2} with a corresponding permittivity of 3266 at 1 kHz (the measured quasi-static C_i was about 36 156 nF cm^{-2} with a quasi-static permittivity of 15 525), as shown in Fig. 7b. But the permittivity reduced rapidly when the frequency increased from 1 kHz to 10 kHz, which is inconsistent with the single-crystal TiO_2-based giant dielectrics.[25] The strongly-frequency-dependent permittivity was ascribed to the extrinsic polarization mechanism, in which the electrons accumulated near the grain boundaries (see Fig. 3) and causing space-charge polarization. Although the permittivity reduced rapidly at higher frequency, the highest frequency required for the active-matrix displays is only 500 Hz (for the high-frame-rate 3D displays). Fig. 8 shows the input and output voltage of a resistor-loaded inverter with an $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/IZO TFT and a resistor (100 kΩ) at 500 Hz. It shows that the output voltage of the inverter responded well to a 500 Hz square-wave input voltage signal, which are fast enough for applications to active-matrix displays. The comparison for different kinds of gate dielectrics for the TFTs is shown in Table 1.

Fig. 9 shows the leakage current density *versus* voltage curve of the ITO/$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/ITO capacitor. The breakdown field was 64.2 kV cm^{-1}. The relatively high leakage current might be attributed to the electron conduction in the crystalline grains. Fig. 10a and b show the output and the transfer characteristics (I_D–V_D curve and I_D–V_G curve) of the IZO-TFT with $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate dielectric, respectively. The operation voltage is only 1 V. No "current crowding" effects is observed at low drain voltage (V_D) in the output curves, implying ohmic contacts between ITO S/D electrodes and IZO active layer. It is worth noting that there was not quadratic increase of saturation I_D with increasing V_G, which is because of space-charge polarization, in which some of the accumulated space charges will leak out at higher gate voltage (causing lowering of the permittivity). There was little hysteresis for the transfer curves between the forward and reverse sweeps (the measuring condition was presented in the ESI, see Fig. S2†), which was different from the TFTs with ferroelectric gate dielectrics. The threshold voltage (V_{th}) was 0.35 V. The mobility (μ) was calculated to be 1.88 $cm^2\ V^{-1}\ s^{-1}$ using the quasi-static capacitance. The mobility and V_{th} distributions of the IZO-TFT with the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate dielectric are shown in Fig. S1.† The average mobility of the devices was 1.94 $cm^2\ V^{-1}\ s^{-1}$, and the maximum mobility was 2.21 $cm^2\ V^{-1}\ s^{-1}$. The average V_{th} was 0.35 V. It is worth noting that the stability under gate bias stress was not good (the shift of V_{th} was −0.31 V under

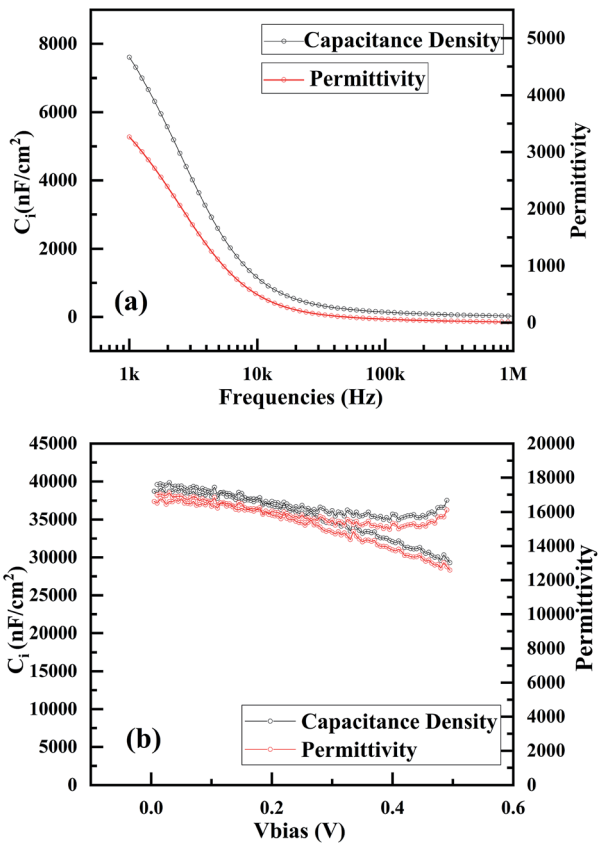

Fig. 7 (a) The frequency dependences of capacitance density (black curve) and permittivity (red curve), (b) the quasi-static C_i–V curve of the capacitor with the ITO/$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/ITO structure annealed at 400 °C for 30 minutes.

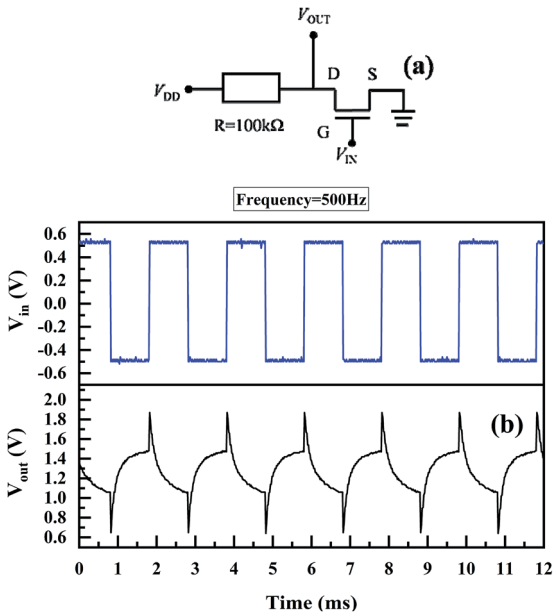

Fig. 8 (a) The circuit of the inverter; (b) the input and output voltage of a resistor-loaded inverter with an $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/IZO TFT and a resistor (100 kΩ) at 500 Hz (V_{DD} = 1.8 V).

Table 1 Comparison of different kinds of high dielectric constant gate insulator for TFTs

Dielectric materials	Dielectric types	C_i (μF cm^{-2})	Gate insulator thickness (nm)	k	SS (mV dec^{-1})	Channel layer	Mobility (cm^2 V^{-1} s^{-1})	Ref.	Year
HfO_2	High-k materials	0.151 (100 Hz)	104	18.5	~180	ZnO	40	1	2015
PEO/$LiClO_4$	Polymer electrolyte	100	~3000	~3.4 × 10^5	—	P3HT	0.7	9	2005
DEME-TFSI	Ionic liquid	0.12 (0.01 Hz)	~10 000	~1350	100	ZnO	—	10	2009
Mesoporous SiO_2	Proton conduction	1.7 (40 Hz)	~4000	~7680	110	$InGaZnO_4$	28.5	11	2009
$Ba_{0.7}Sr_{0.3}TiO_3$	Ferroelectrics	0.261(40 Hz)	670	~200	260	Pentacene	1.24	4	2012
$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$	Giant-dielectrics	7.6 (1 kHz) 36.1 (quasi-static)	380	3255 15 525	68	IZO	1.88	This work	2019

negative bias stress for 1 h, see Fig. S3†), which may be attributed to the defects at the interface between $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ and IZO.

Fig. 10c shows the SS as a function of V_G in the subthreshold regime. Theoretically, SS is expressed as,

$$SS = \frac{\partial V_G}{\partial(\log_{10} I_D)} = \frac{\partial V_G}{\partial \psi_s}\frac{\partial \psi_s}{\partial(\log_{10} I_D)} \quad (2)$$

where Ψ_s is the surface potential of the semiconductor channel at the gate dielectric/semiconductor interface. $\partial V_G/\partial \Psi_s$ given by

$$\frac{\partial V_G}{\partial \psi_s} = 1 + \frac{C_s}{C_{ins}} \quad (3)$$

where C_s is the capacitance of the semiconductor and C_{ins} is the capacitance of the gate dielectric, must exceed one (except for the negative capacitance). Because the carriers are confined into an ultrathin layer in close proximity to the gate dielectric/semiconductor interface, it is reasonable to assume that the carrier distribution within this ultrathin layer is uniform. Thus I_D can be expressed as

$$I_D = nevS = n_D \exp\left(\frac{e\psi_s}{kT}\right)evS \quad (4)$$

where n is the carrier (electron) density at the interface, e is the electron charge, v is the electron velocity in the semiconductor, S is the lateral area of the channel, n_D is the donor density, k is Boltzmann constant, and T is the absolute temperature. Thus,

$$\begin{aligned}\partial(\log_{10} I_D) &= \partial\left\{\log_{10}\left[n_D \exp\left(\frac{e\psi_s}{kT}\right)evS\right]\right\} \\ &= \partial\left\{\frac{1}{\ln_{10}}\ln\left[n_D \exp\left(\frac{e\psi_s}{kT}\right)evS\right]\right\} \\ &= \frac{1}{\ln_{10}}\partial\left[\frac{e\psi_s}{kT} + \ln(n_D evS)\right] \\ &= \frac{1}{\ln_{10}}\partial\left(\frac{e\psi_s}{kT}\right)\end{aligned} \quad (5)$$

$$\frac{\partial \psi_s}{\partial(\log_{10} I_D)} = \frac{\ln_{10}\partial\psi_s}{\partial\left(\frac{e\psi_s}{kT}\right)} = \frac{\ln_{10} kT}{e} \approx 0.06 \quad (6)$$

It can be deduced from eqn (2), (3) and (6) that SS should be greater than 0.06 V dec^{-1}.[26] For the IZO TFTs with $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate dielectrics, the gate leakage current of the forward sweep and much higher than that of the reverse sweep (see Fig. 10b), so the SS of the forward-sweep transfer curve was affected by the gate leakage current. For the reverse sweep of the transfer curve, the off current (I_{off}) was much higher than the gate leakage current, so the SS of the reverse-sweep transfer curve was more accurate. It can be seen from Fig. 10c that the SS of the reverse-sweep transfer curve was about 0.068 V dec^{-1}, very close to the lowest limit of the SS of the field-effect transistors (0.06 V dec^{-1}). And the SS is the same as the IGZO-TFTs with ultrathin Al_xO_y gate dielectrics (~3 nm).[27] These results prove

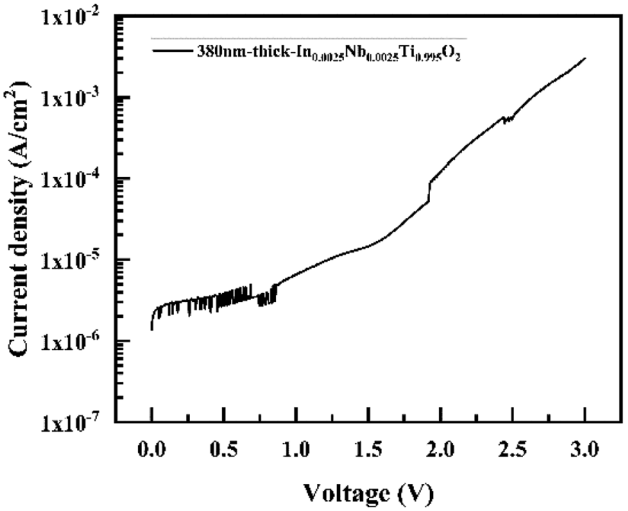

Fig. 9 The leakage current density *versus* voltage curve of the ITO/$In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$/ITO capacitor annealed at 400 °C for 30 minutes.

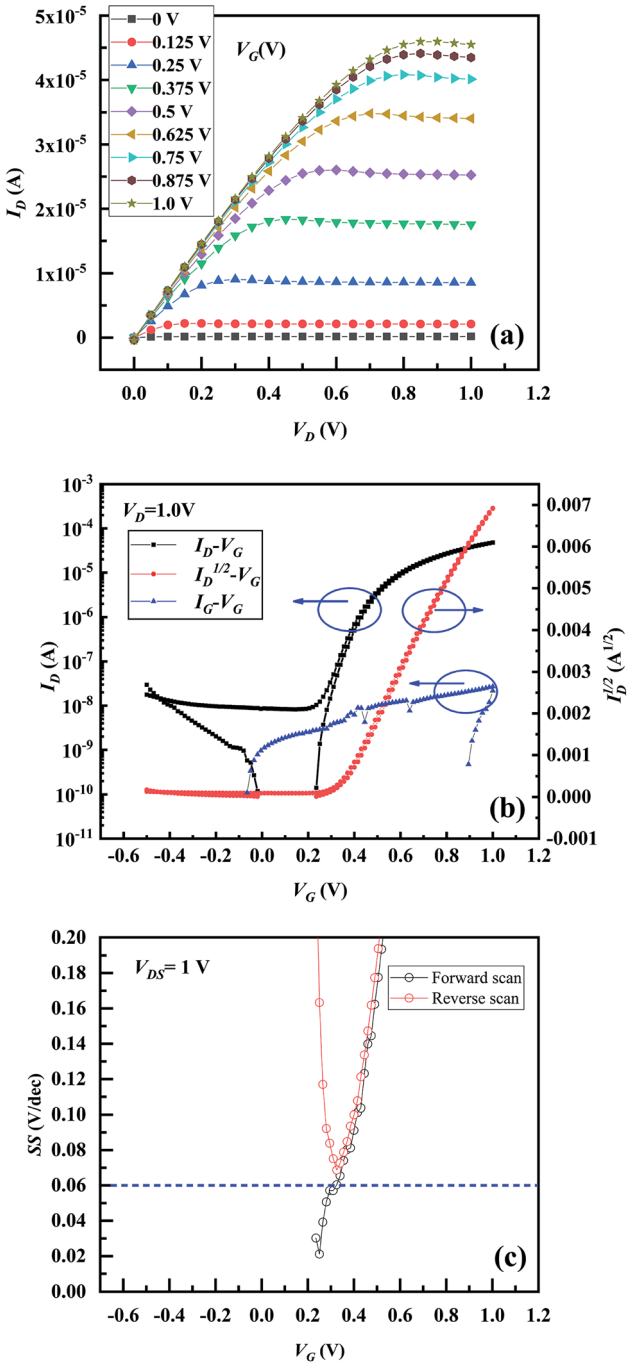

Fig. 10 (a) The output curve, (b) the transfer curve and (c) the SS–V_G curve of the IZO-TFT with the $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ insulator.

that the lowest limit of the SS (0.06 V dec^{-1}) of the filed-effect transistors cannot be broken no matter how high the gate dielectric capacitance is (except for ferroelectric negative capacitors).

4. Conclusion

In conclusion, low-temperature (400 °C) giant-dielectric-constant thin films ($In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$) fabricated with simply radio frequency (RF) sputtering on glass substrates are employed as the gate dielectrics for thin-film transistors (TFTs) for the first time. The 380 nm-thick $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ film was in polycrystalline state with a quasi-static capacitance of as high as 36 156 nF cm^{-2} with a quasi-static permittivity of 15 525, and the capacitance was as high as 7607 nF cm^{-2} with a corresponding permittivity of 3266 at 1 kHz. Indium zinc oxide (IZO) TFTs with $In_{0.0025}Nb_{0.0025}Ti_{0.995}O_2$ gate dielectrics exhibited high output current (the mobility was 1.88 cm^2 V^{-1} s^{-1}, and the V_{th} was 0.35 V.) at low operation voltage (less than 1 V) and little hysteresis in the transfer curves between forward and reverse sweeps. The subthreshold swing (SS) of the IZO TFTs is 0.068 V dec^{-1}, very close to the lowest limit of the SS of the field-effect transistors (0.06 V dec^{-1}). The results also proves that the lowest limit of the SS (0.06 V dec^{-1}) of the field-effect transistors cannot be broken no matter how high the gate dielectric capacitance is (except for negative capacitors). The TFTs demonstrate the potential for the application of low-power circuits and flat-panel displays.

Conflicts of interest

There are no conflicts to declare.

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