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# Vertically stacked SnSe homojunctions and negative capacitance for fast low-power tunneling transistors†

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The two-dimensional (2D) vertical van der Waals (vdW) stacked homojunction is an advantageous configuration for fast low-power tunneling field effect transistors (TFETs). We simulate the device performance of the sub-10 nm vertical SnSe homojunction TFETs with *ab initio* quantum transport calculations. The vertically stacked device configuration has an effect of decreasing leakage current when compared with its planar counterpart due to the interrupted carrier transport path by the broken connection. A subthreshold swing over four decades ( $SS_{\text{ave},4 \text{ dec}}$ ) of 44.2–45.8 mV dec<sup>-1</sup> and a drain current at  $SS = 60 \text{ mV dec}^{-1}$  ( $I_{60}$ ) of 5–7  $\mu\text{A } \mu\text{m}^{-1}$  are obtained for the optimal vertical SnSe homojunction TFET with  $L_g = 10 \text{ nm}$  at a supply voltage of 0.5–0.74 V. In terms of the device's main figures of merit (*i.e.*, on-state current, intrinsic delay time, and power delay product), the vertical SnSe TFETs and NCTFETs outperform the 2022 and 2028 targets of the International Technology Roadmap for Semiconductors requirements for low-power application (2013 version), respectively.

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## 1 Introduction

A tunneling field effect transistor (TFET) is a competitive post-CMOS low-power (LP) switch for future nano-electronics because avoiding thermionic carrier injection produces sub-60 mV dec<sup>-1</sup> subthreshold swings (SS).<sup>1–4</sup> The main challenge in adopting TFETs for real application is the low on-state currents ( $I_{\text{on}}$ ) despite the sharp minimum SS. The use of two-dimensional (2D) (instead of 3D) semiconductors (*e.g.*, black phosphorene (BP), bismuthine, GeSe, and SnSe) as channel materials can effectively improve  $I_{\text{on}}$  to enable TFETs even for high-performance (HP) applications with a single channel material and a simple planar p–i–n device configuration.<sup>5–8</sup> However, unacceptably high leakage currents ( $I_{\text{leak}}$ ) for LP applications are also found at the ultrashort sub-10 nm size. The planar ML SnSe TFET is one example.<sup>5</sup> To reduce  $I_{\text{leak}}$ , structural modifications that can produce an additional tunneling barrier are appreciated. The vertically stacked configuration, *i.e.*, to overlap a top and a bottom layer vertically

in the channel region, is one suggested structural modification to lower  $I_{\text{leak}}$ .<sup>9</sup>

As the first discovered 2D material with anisotropic charge transport characters, monolayer (ML) and few-layers BP are expected as the potential channel materials for next-generation nano-electronics like transistors and have been extensively investigated in labs.<sup>10–13</sup> However, the excellent semiconducting properties of 2D BP would rapidly lose upon exposure to ambient conditions, which would somehow ruin the original outstanding device performances. Though air-stable 2D BP devices are realized by protective layers<sup>14–16</sup> and ambient thermal treatment,<sup>17</sup> the increased cost would undoubtedly hamper future large-scaled applications. Therefore, exploring new 2D channels with both excellent electronic properties and high stability is crucial for the manufacturing process of future nano-electronics. As one of BP analogs, ML and few-layers SnSe have been synthesized in labs in recent years.<sup>18–20</sup> Similar to ML BP, ML SnSe is low-toxic and possesses excellent electronic properties like anisotropic electronic, moderate near direct bandgap, and high carrier mobility.<sup>21–23</sup> Moreover, 2D SnSe has good ambient stability<sup>22,24</sup> and economic earth-abundance elements, which are another two advantages for practical future nano-electronics. Considering the high current of the planar ML SnSe TFET and the above benefits, it's meaningful to find out whether the vertically stacked SnSe homojunction, which is much less studied than the planar configuration, could enable the SnSe TFET as fast LP device in regard to the International Technology Roadmap for Semiconductors (ITRS) requirements (2013 version). Besides, to find out whether the

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negative capacitance effect could improve the device performances evidently is also a meaningful issue.

In this paper, we investigate the device performances of the sub-10 nm vertical SnSe homojunction TFETs with *ab initio* quantum transport calculations. A sub-thermionic SS over four decades ( $SS_{\text{ave}_4 \text{dec}}$ ) of 44.2–45.8 mV dec<sup>-1</sup> and a drain current at  $SS = 60 \text{ mV dec}^{-1}$  ( $I_{60}$ ) of 5–7  $\mu\text{A } \mu\text{m}^{-1}$  are obtained for the 10 nm optimal vertical SnSe homojunction TFETs. The sub-thermionic  $SS_{\text{ave}_4 \text{dec}}$  and high  $I_{60}$  indicate a fast low-power device. The device performances (*i.e.*, on-state current, intrinsic delay time, and power delay product) of this sub-10 nm vertical SnSe TFETs and NCTFETs surpass the 2022 and 2028 targets of the ITRS LP device (2013 version), respectively.

## 2 Models and methods

We first optimized the ML SnSe and bilayer (BL) SnSe with the density functional theory (DFT) using QuantumATK.<sup>25,26</sup> We use a norm-conserving pseudopotential of 'SG15' with 'Medium' basis set, a cutoff energy of 100 Ha, an exchange–correlation functional in the form of generalized gradient approximation of Perdew–Burke–Ernzerh (GGA-PBE)<sup>27</sup> with Grimme DFT-D2 correction,<sup>28</sup> and a Monkhorst–Pack mesh<sup>29</sup> of  $31 \times 31 \times 1$  *k*-points, and an electron temperature of 300 K. To judge the DFT-

D2 functional, we compare the optimized lattice and band gap of bulk, bilayer, and ML SnSe obtained with three functionals, *i.e.*, PBE, Grimme DFT-D2, and Grimme DFT-D3, in Table S1.† The DFT-D2 functional gives the best lattice cells among the three checked functionals to reproduce the former theoretical and experimental results.<sup>30</sup>

The double-gated (DG) device model of the vertical SnSe homojunction TFET is presented in Fig. 1(a), where two optimized ML SnSe are stacked vertically with van der Waals interaction and the distance of the top and bottom layer of the vertical SnSe TFET is taken from optimized BL SnSe. Only the zigzag transport direction with lighter effective mass is studied due to the higher on-state current ( $I_{\text{on}}$ ), as shown in a previous work.<sup>5</sup> The stacked overlap region is around 1 nm, and the stacked sites (*i.e.*, the position of the 1 nm overlap region of the top and bottom layer of SnSe) at the left, central, and right and the source/drain doping concentrations ( $N_s/N_d$ ) are taken into consideration to optimize  $I_{\text{on}}$  of the vertical SnSe TFET with a physical gate length ( $L_g$ ) of 10 nm. The 1 nm overlap region at the central site is highlighted with a dotted rectangle box in Fig. 1(a). With the optimal stacked sites and  $N_s/N_d$ , vertical SnSe TFETs with a shorter  $L_g$  of 7 and 5 nm and a source underlap of  $UL_s = 10 - L_g$  nm are studied. The values of supply voltages ( $V_{\text{dd}}$ , equals to the bias voltage  $V_{\text{ds}}$ ) of 0.74 and 0.65 V are taken

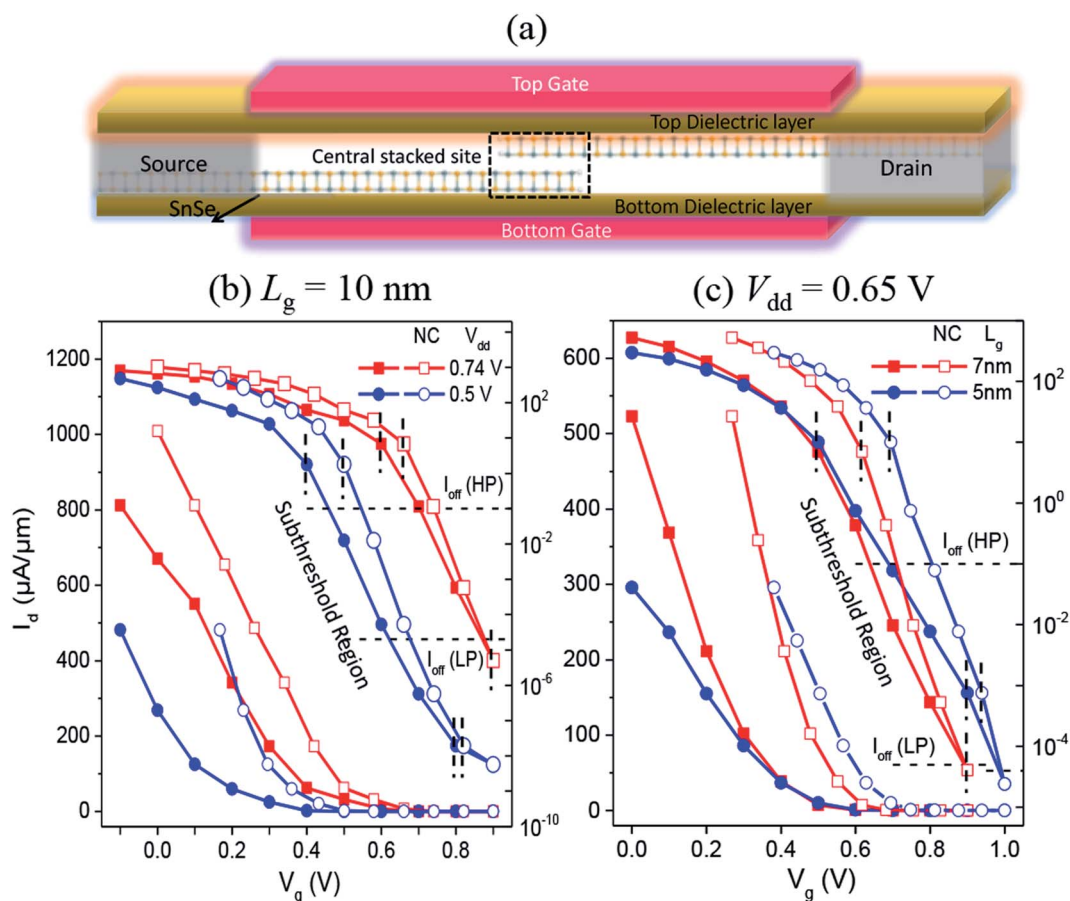


Fig. 1 (a) Device model and (b and c) transfer characteristics of the optimal sub-10 nm vertical SnSe homojunction p-TFETs and p-NCTFETs. The subthreshold region is marked with vertical black dash lines.



in regard to the International Technology Roadmap for Semiconductors (ITRS) requirements (2013 version) at similar  $L_g$ . We also scale down  $V_{dd}$  to 0.5 V for the optimal 10 nm vertical SnSe TFET.

The vertical SnSe homojunction TFETs are calculated by the DFT coupled with nonequilibrium Green's function (NEGF) using QuantumATK.<sup>25,26</sup> We use the same setting parameters as the DFT calculations for device simulations except for  $31 \times 1 \times 151$   $k$ -points. It's known that the GGA approximation has underestimate band gaps of intrinsic semiconductors. However, in a device model, the electrodes and channel are in a heavy doped condition, which induces a heavy screening effect to the electron–electron interaction. In the heavy doping case, the GGA approximation becomes a fine approach to the GW method for semiconductor's band gaps as discussed in a previous work.<sup>5</sup>

The transmission coefficient  $T(E)$  is obtained by averaging  $T(E, k_x)$  over 61  $k_x$ -points, where  $T(E, k_x) = T_{\uparrow}[G^r(E, k_x)I_{s/d}(E, k_x)G^a(E, k_x)I_{d/s}(E, k_x)]$ . Then the current  $I(V_{ds}, V_g)$  is then derived from  $T(E)$  from the Landauer–Büttiker formula:<sup>31</sup>

$$I(V_{ds}, V_g) = \frac{2e}{h} \int_{-\infty}^{+\infty} \{T(E, V_{ds}, V_g)[f_s(E - \mu_s) - f_d(E - \mu_d)]\} dE$$

Here,  $G^{r/a}$  is the retarded/advanced Green's function and  $I_{s/d}$ ,  $f_{s/d}$ , and  $\mu_{s/d}$  are the line width function in terms of self-energy, Fermi–Dirac distribution function, and electrochemical potential of the source/drain, respectively.

We then use a 100 nm-thick SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> to construct negative capacitance vertical TFETs with the SnSe stacked homojunction, where SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> is the best ferroelectric material among four checked ones for the ML GeSe and GeTe TFETs.<sup>32</sup> A negative voltage drop  $V_{NC}$  should happen across the ferroelectric layer so that a sharper subthreshold swing is expected. We

calculate the  $V_{NC}$  with the Landau–Khalatnikov (L–K) theory<sup>33</sup> as follows:

$$V_{NC} = 2\alpha t_{Fe}Q + 4\beta t_{Fe}Q^3 + 6\gamma t_{Fe}Q^5$$

Here,  $t_{Fe}$  is the thickness and  $\alpha$ ,  $\beta$ , and  $\gamma$  the Landau coefficients of the ferroelectric layer.  $Q$  is the electrical charge on the channel calculated from Mulliken population. We set  $t_{Fe}$  to 100 nm and  $\alpha$ ,  $\beta$ , and  $\gamma$  to  $-3.74 \times 10^8$ ,  $-9.4 \times 10^7$ , and  $1.18 \times 10^9$  from a former work.<sup>34</sup>

## 3 Results and discussions

### 3.1 Device optimization and current

Considering the stacked sites and  $N_s/N_d$  might have some effect on currents, we first optimize  $I_{leak}$  and  $I_{on}$  of the 10 nm vertical SnSe homojunction TFET at  $V_{dd} = 0.74$  V. The transfer characteristics of the vertical SnSe TFETs with stacked sites (fixed  $N_s/N_d$  of  $5/5 \times 10^{13} \text{ cm}^{-2}$ ) are given in Fig. S1(a).<sup>†</sup> Ambipolar characters are seen for the three TFETs as  $N_s$  and  $N_d$  are the same. All  $I_{leak}$  are  $\sim 10^{-3} \mu\text{A } \mu\text{m}^{-1}$ , which are low enough to meet the off-state current ( $I_{off}$ ) of  $0.1 \mu\text{A } \mu\text{m}^{-1}$  of the HP devices but too high to meet  $I_{off}$  of  $2 \times 10^{-5} \mu\text{A } \mu\text{m}^{-1}$  of the LP devices of the ITRS requirements (2013 version). Thus, we extract  $I_{on}$  from the transfer characteristics for both p- and n-type branches and give the values in Table S2.<sup>†</sup> The central site of the stacked position is the best one for  $I_{on}$  of both the p- and n-type vertical SnSe TFETs with the values of 791 and 695  $\mu\text{A } \mu\text{m}^{-1}$ , respectively, which meet 61% and 54% of 1287  $\mu\text{A } \mu\text{m}^{-1}$  of the ITRS HP device.

We then pick up the vertical SnSe TFET with the central stacked site and continue to lower  $I_{leak}$  by applying an asymmetric  $N_s/N_d$ . In general, the asymmetric  $N_s/N_d$  would destroy the ambipolar characters of a TFET, and an improved  $I_{on}$  would

**Table 1** Device performances of the optimal sub-10 nm vertical SnSe homojunction p-TFETs and p-NCTFETs for LP application. The ITRS requirements for LP devices and those of the planar GeSe,<sup>5</sup> planar BP,<sup>35</sup> vertical homojunction BP,<sup>9</sup> and vertical homojunction antimonene<sup>35</sup> TFETs are given for comparison.  $L_g$ : physical gate length; ULs: source underlap;  $V_{dd}$ : supply voltage;  $I_{off}$ : off-state current;  $I_{on}$ : on-state current; SS: subthreshold swing;  $g_m$ : transconductance;  $\tau$ : delay time; and PDP: power dissipation

	$L_g$ (nm)	$V_{dd}$ (V)	UL (nm)	$I_{off}$ ( $\mu\text{A } \mu\text{m}^{-1}$ )	$I_{on}$ ( $\mu\text{A } \mu\text{m}^{-1}$ )	SS (mV dec <sup>-1</sup> )	$g_m$ (mS $\mu\text{m}^{-1}$ )	$\tau$ (ps)	PDP (fJ $\mu\text{m}^{-1}$ )
Vertical SnSe	10	0.74	0	$2 \times 10^{-5}$	488	48.2	1.89	0.081	0.019
Vertical SnSe NCTFET	10	0.74	0	$2 \times 10^{-5}$	747	36.8	2.04	0.068	0.023
Vertical BP <sup>9</sup>	10	0.74	0	$2 \times 10^{-5}$	830	39	4.30	0.029	0.027
Planar GeSe <sup>5</sup>	10	0.74	0	$2 \times 10^{-5}$	759	45	3.92	0.062	0.035
ITRS 2022	10.1	0.72	—	$2 \times 10^{-5}$	461	—	—	1.556	0.52
Vertical SnSe	10	0.5	0	$1 \times 10^{-5}$	105	49.0	1.78	0.346	0.011
Vertical SnSe NCTFET	10	0.5	0	$1 \times 10^{-5}$	404	36.7	2.77	0.133	0.017
Vertical Sb <sup>35</sup>	10	0.5	0	$1 \times 10^{-5}$	193	22	—	—	—
Planar BP <sup>35</sup>	10	0.5	0	$1 \times 10^{-5}$	135	33	—	—	—
Planar GeSe <sup>5</sup>	10	0.5	0	$1 \times 10^{-5}$	146	—	—	0.19	0.014
Vertical SnSe	7	0.65	3	$4 \times 10^{-5}$	157	74.5	1.56	0.278	0.018
Vertical SnSe NCTFET	7	0.65	3	$4 \times 10^{-5}$	565	47.8	1.84	0.092	0.021
Vertical BP <sup>9</sup>	7	0.66	0	$4 \times 10^{-5}$	350	63	4.23	0.063	0.018
ITRS 2026	7	0.66	—	$4 \times 10^{-5}$	337	—	—	1.514	0.34
Vertical SnSe	5	0.65	5	$5 \times 10^{-5}$	62	91.4	0.75	0.721	0.018
Vertical SnSe NCTFET	5	0.65	5	$5 \times 10^{-5}$	346	60.1	1.14	0.154	0.021
Vertical BP <sup>9</sup>	5	0.64	5	$5 \times 10^{-5}$	312	76	3.9	0.078	0.018
ITRS 2028	5.9	0.64	—	$5 \times 10^{-5}$	295	—	—	1.493	0.28



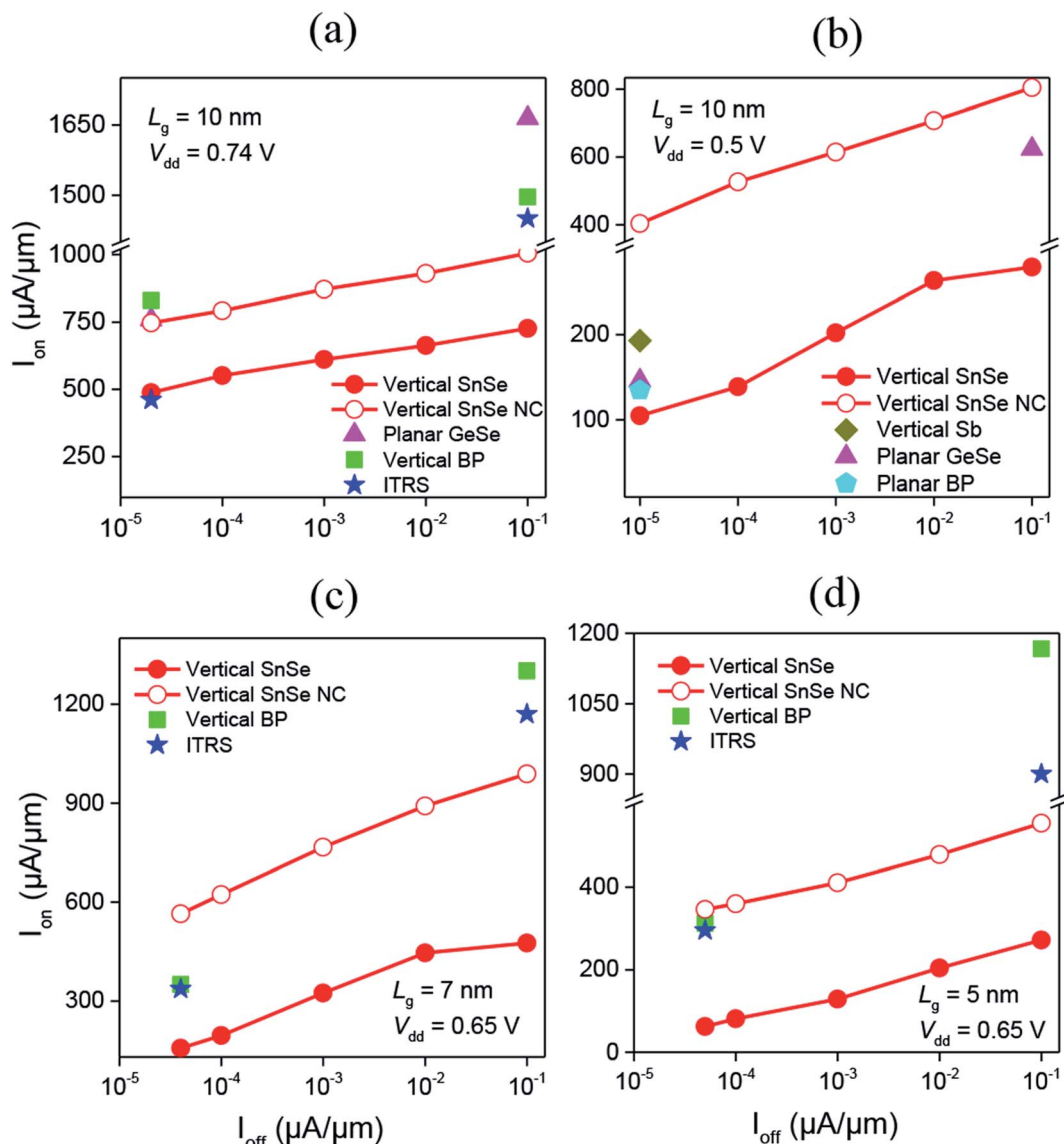


Fig. 2  $I_{\text{on}}$  vs.  $I_{\text{off}}$  of the optimal vertical SnSe homojunction p-TFETs and p-NCTFETs with (a)  $L_g = 10$  nm and  $V_{\text{dd}} = 0.74$  V, (b)  $L_g = 10$  nm and  $V_{\text{dd}} = 0.5$  V, (c)  $L_g = 7$  nm and  $V_{\text{dd}} = 0.65$  V, and (d)  $L_g = 5$  nm and  $V_{\text{dd}} = 0.65$  V.  $I_{\text{on}}$  of the ITRS requirements for LP and HP devices and those of the planar GeSe,<sup>5</sup> planar BP,<sup>35</sup> vertical homojunction BP,<sup>9</sup> and vertical homojunction antimonene<sup>35</sup> TFETs are given for comparison.

be acquired with a light- $N_s$ /heavy- $N_d$  for p-type branch and heavy- $N_s$ /light- $N_d$  for n-type one from previous studies.<sup>5-7</sup> The transfer characteristics of the vertical SnSe TFETs with  $N_s$  of  $1/0.3/0.1 \times 10^{13} \text{ cm}^{-2}$  (fixed  $N_d$  of  $5 \times 10^{13} \text{ cm}^{-2}$ ) and  $N_d$  of  $1/0.3/0.1 \times 10^{13} \text{ cm}^{-2}$  (fixed  $N_s$  of  $5 \times 10^{13} \text{ cm}^{-2}$ ) are drawn in Fig. S1(b) and (c),<sup>†</sup> respectively. A lower  $I_{\text{leak}}$  of  $10^{-4}$ – $10^{-7} \mu\text{A } \mu\text{m}^{-1}$  and an enhanced p- or n-type character are acquired as expected.  $I_{\text{leak}}$  is small enough for LP applications when either  $N_s$  or  $N_d \leq 0.3 \times 10^{13} \text{ cm}^{-2}$ . Benchmark of  $I_{\text{on}}(\text{HP})$  and  $I_{\text{on}}(\text{LP})$  against the ITRS HP/LP devices and its planar counterpart is presented in Table S3.<sup>†</sup> For HP application, the asymmetric  $N_s/N_d$  does not show a positive effect on  $I_{\text{on}}$ . Compared with its planar counterpart at the same  $N_s/N_d$  of  $1/5 \times 10^{13} \text{ cm}^{-2}$ ,  $I_{\text{leak}}$  decreased from  $\sim 10^{-2}$  to  $\sim 10^{-4} \mu\text{A } \mu\text{m}^{-1}$  and  $I_{\text{on}}(\text{HP})$  from 1667 to  $790 \mu\text{A } \mu\text{m}^{-1}$ . The descending currents come from the

interrupted carrier transport path by the structure modification of vertical stacking. For LP application, the lightest  $N_s$  or  $N_d$  is the best. In the following, we will focus on the device performances of the enhanced p-type region of the optimal vertical SnSe homojunction TFETs with central stacked sites and  $N_s/N_d = 0.1/5 \times 10^{13} \text{ cm}^{-2}$  for LP applications.

The transfer characteristics of the sub-10 nm optimal vertical SnSe homojunction p-TFETs are given in Fig. 1(b and c), and the key figures of merit for LP applications are presented in Table 1. As  $L_g$  decreases to 7/5 nm,  $I_{\text{leak}}$  is also low enough to meet  $I_{\text{off}}$  of  $4/5 \times 10^{-5} \mu\text{A } \mu\text{m}^{-1}$  of the ITRS LP devices. The ITRS targets for LP devices and the device performances of the planar GeSe,<sup>5</sup> planar BP,<sup>35</sup> vertical homojunction BP,<sup>9</sup> and vertical homojunction antimonene<sup>35</sup> TFETs are given for comparison in Table 1. We provide  $I_{\text{on}}$  as a function of  $I_{\text{off}}$  of the SnSe homojunction



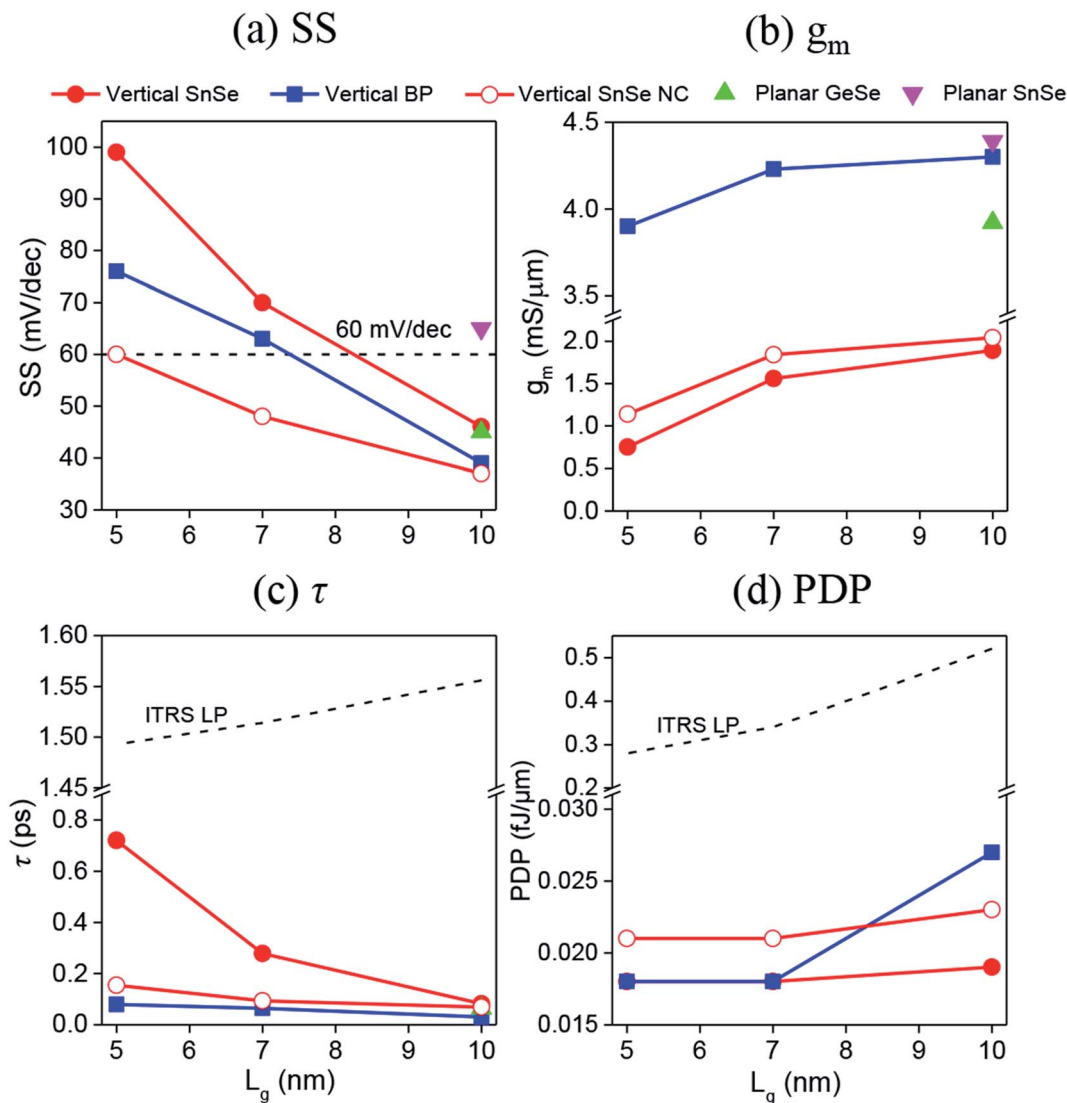


Fig. 3 (a) SS, (b)  $g_m$ , (c)  $\tau$ , and (d) PDP as a function of  $L_g$  of the optimal sub-10 nm vertical SnSe homojunction p-TFETs and p-NCTFETs ( $V_{dd} = 0.64$ – $0.74$  V) compared with those of the ITRS requirements for LP devices and those of the planar GeSe<sup>5</sup> and vertical homojunction BP.<sup>9</sup>

p-TFETs ( $L_g = 5$ – $10$  nm,  $V_{dd} = 0.5$ – $0.74$  V) and  $I_{on}$  of the devices mentioned above in Fig. 2(a–d). The optimal  $I_{on}(LP)$  are 488, 146, and  $62 \mu\text{A } \mu\text{m}^{-1}$  for the vertical SnSe p-TFET at  $L_g = 10$ , 7, and 5 nm, respectively, which surpass or meet 43% and 21% of 461, 337, and  $195 \mu\text{A } \mu\text{m}^{-1}$  of the 2022, 2026, and 2028 targets of the ITRS LP devices (2013 version) at similar  $L_g$ , respectively. As seen in Fig. 2, when  $I_{off}$  increases by  $\sim 4$  orders of magnitude from  $\sim 10^{-5}$  to  $10^{-1} \mu\text{A } \mu\text{m}^{-1}$ ,  $I_{on}$  increases slowly by 1.5–4.1 times, and the increment is more notable for the TFET with a shorter  $L_g$  or at a lower  $V_{dd}$ . Though  $I_{on}$  of the vertical SnSe p-TFET show no goodness when compared to other sub-10 nm TFETs, it's worthy to note that  $I_{on}$  of  $105 \mu\text{A } \mu\text{m}^{-1}$  of the 10 nm vertical SnSe p-TFET is comparable with those of  $135$ – $193 \mu\text{A } \mu\text{m}^{-1}$  of the vertical antimonene TFET and the planar phosphorene and GeSe TFETs at  $V_{dd} = 0.5$  V.<sup>5,35</sup>

### 3.2 Gate control ability and dynamic performance metrics

The gate control abilities are described by the subthreshold swing ( $SS = \frac{\partial V_g}{\partial \lg I_D}$ ) and transconductance ( $g_m = \frac{dI_D}{dV_g}$ ) in the subthreshold and superthreshold regions, respectively. A smaller SS (or a larger  $g_m$ ) stands for a stronger gate control ability. We give SS (in the subthreshold region as marked in Fig. 1) and  $g_m$  of the sub-10 nm optimal vertical SnSe homojunction p-TFET compared with those of the vertical BP and planar GeSe and SnSe TFETs<sup>5,9</sup> in Fig. 3(a and b). The subthreshold regions cover five to eight decades of currents for all the vertical SnSe p-TFETs. Both an increasing SS (48.2 to  $91.4 \text{ mV dec}^{-1}$ ) and decreasing  $g_m$  ( $1.89$  to  $0.75 \text{ mS } \mu\text{m}^{-1}$ ) with the decreasing  $L_g$  are seen for the vertical SnSe p-TFETs, which indicates the descending gate control ability with the decreasing  $L_g$  in both subthreshold and superthreshold regions. The slightly larger SS and much smaller  $g_m$  of the vertical SnSe



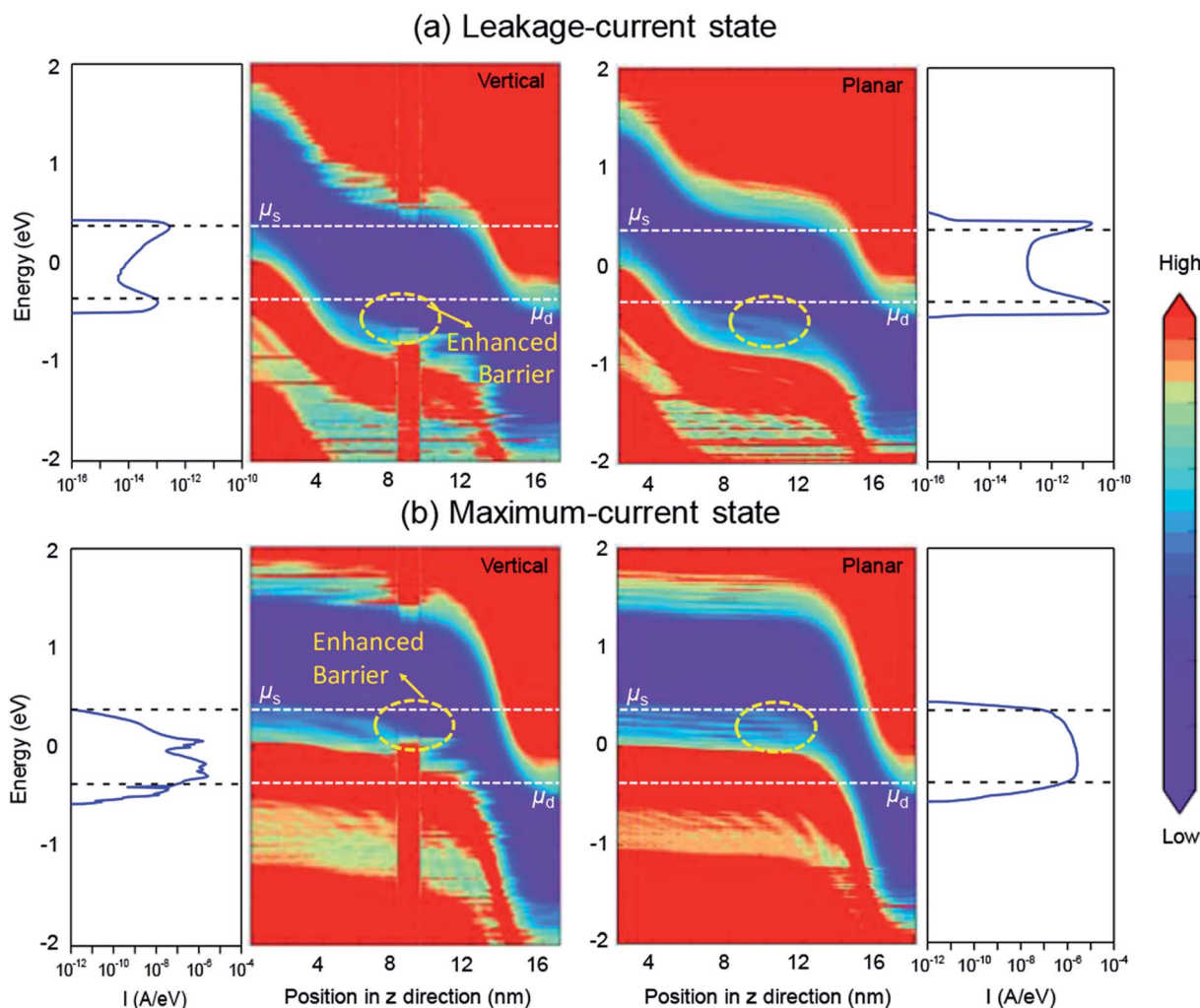


Fig. 4 Local device density of states (LDDOS) and spectral currents of the optimal vertical SnSe homojunction p-TFETs with  $L_g = 10$  nm at  $V_{dd} = 0.74$  V compared with those of the planar counterpart for the (a) leakage-current state and (b) maximum-current state.

p-TFETs compared with those of the vertical BP and planar GeSe TFETs<sup>5,9</sup> at the same  $L_g$  indicate a slightly weaker gate control in the subthreshold region and a much weaker gate control in the superthreshold regions, respectively. Whereas, in regard to its SnSe planar counterpart,<sup>5</sup> much enhanced and descended gate controls are found in the subthreshold and superthreshold regions, respectively.

The average SS over four decades of current ( $SS_{ave\_4\text{ dec}}$ ) and the drain current at  $SS = 60$  mV  $\text{dec}^{-1}$  ( $I_{60}$ ) are regarded as two metrics for fast low-power devices. Basically,  $SS_{ave\_4\text{ dec}}$  below 60 mV  $\text{dec}^{-1}$  and  $I_{60}$  above  $1 \mu\text{A} \mu\text{m}^{-1}$  are asked for a fast low-power device. We present the minimum SS ( $SS_{\min}$ ),  $SS_{ave\_4\text{ dec}}$ , and  $I_{60}$  of the vertical SnSe p-TFETs in Table S4.† The sharp  $SS_{\min}$  is harder to maintain over decades of current in the vertical SnSe p-TFETs with shorter  $L_g$ . Sub-thermionic  $SS_{\min}$  and  $SS_{ave\_4\text{ dec}}$  and high  $I_{60}$  are only obtained for the 10 nm vertical SnSe p-TFET, *i.e.*,  $SS_{\min}$  of 42.0–43.4 mV  $\text{dec}^{-1}$ ,  $SS_{ave\_4\text{ dec}}$  of 44.2–45.8 mV  $\text{dec}^{-1}$ , and  $I_{60}$  of 5–7  $\mu\text{A} \mu\text{m}^{-1}$  at  $V_{dd} = 0.5$ –0.74 V. For the 7 and 5 nm vertical SnSe p-TFETs,  $SS_{\min}$  are 60.7 and

66.7 mV  $\text{dec}^{-1}$  and  $SS_{ave\_4\text{ dec}}$  are 71.2 and 90.1 mV  $\text{dec}^{-1}$ , respectively.

The device dynamic performance metrics are represented by the intrinsic delay time ( $\tau = \frac{Q_{\text{on}} - Q_{\text{off}}}{W \times I_{\text{on}}}$ ) and the power delay

product ( $\text{PDP} = \frac{(Q_{\text{on}} - Q_{\text{off}}) \times V_{dd}}{W}$ ), which define the switching speed and energy consumption of a transistor, respectively. Here,  $Q_{\text{on/off}}$  is the on-/off-state overall charge of the channel and  $W$  the channel width. We benchmark  $\tau$  and PDP of the vertical SnSe p-TFETs against the ITRS LP devices and the planar GeSe and vertical BP TFETs<sup>5,9</sup> in Fig. 3(c and d).  $\tau$  of the vertical SnSe p-TFET increases rapidly from 0.156 to 0.721 ps with the decreasing  $L_g$  from 10 to 5 nm, indicating an obvious decaying of the device switching speed with the decreasing  $L_g$ .  $\tau$  of the vertical SnSe p-TFET is half to one-tenth of 1.493–1.556 ps of the ITRS LP devices, but much larger than those of the planar GeSe and vertical BP TFETs at the same  $L_g$ . The vertical SnSe p-TFET shows a generally better behavior on energy consumption



at a shorter  $L_g$  as a decreasing trend of PDP is seen. PDP of 0.018–0.035 fJ  $\mu\text{m}^{-1}$  of the vertical SnSe p-TFET is more than one order of magnitude below the ITRS LP devices (0.28–0.52 fJ  $\mu\text{m}^{-1}$ ) and nearly equal to those of the planar GeSe and vertical BP TFETs<sup>5,9</sup> at the same  $L_g$ .

### 3.3 Negative capacitance

The vertically stacked homojunction has a prominent effect of lowering  $I_{\text{leak}}$  of its planar counterpart, but unfortunately,  $I_{\text{on}}$  descends as well. We then import negative capacitance to make the SS sharper and therefore to improve  $I_{\text{on}}$ . The transfer characteristics of the vertical SnSe p-NCTFETs with a 100 nm-thick ferroelectric layer of SrBi<sub>2</sub>Nb<sub>2</sub>O<sub>9</sub> are given in Fig. 1(b and c). A remarkable enhanced of  $I_{\text{on}}$  by 53–458% is obtained as given in Table 1 and Fig. 2.  $I_{\text{on}}$  of 565 and 346  $\mu\text{A } \mu\text{m}^{-1}$  of the vertical SnSe NCTFETs surpass the 2026 and 2028 targets of 337 and 295  $\mu\text{A } \mu\text{m}^{-1}$  of the ITRS LP device at  $L_g = 7$  and 5 nm, respectively. At a lower  $V_{\text{dd}} = 0.5$  V,  $I_{\text{on}}$  of 404  $\mu\text{A } \mu\text{m}^{-1}$  of the 10 nm vertical SnSe NCTFET is 2–3 times the vertical antimonene TFET and the planar phosphorene and GeSe TFETs.<sup>5,35</sup> The SS and  $g_m$  of the vertical SnSe NCTFETs are given in Table 1 and Fig. 3(a and b). SS decrease to 36.7–60.1 mV dec<sup>-1</sup> and  $g_m$  increase to 1.14–2.77 mS  $\mu\text{m}^{-1}$ , implying an enhanced gate control of the NCTFET counterpart.  $\tau$  decrease to 0.068–0.154 ps and PDP increase slightly to 0.017–0.023 fJ  $\mu\text{m}^{-1}$  as given in Table 1 and Fig. 3(c and d).

### 3.4 LDDOS, spectral current, and discussion

The local device density of states (LDDOS) together with spectral currents of the vertical SnSe p-TFET at  $V_g = 1.0$  V (leakage current) and 0.0 V (maximum current) compared with its planar counterpart are presented in Fig. 4. An obvious enhanced barrier can be seen from the LDDOS of the vertical SnSe p-TFET for both the leakage-current and maximum-current states, which results in a sound decreasing of spectral currents. As a result, this vertically stacked modification of the SnSe TFET lower the leakage current of its planar counterpart by 2–3 orders of magnetite, but an unwanted descendant of  $I_{\text{on}}$  by around a half is accompanied.

In a word, the structural modification of vertical stacking is a certainly effective solution to lower  $I_{\text{leak}}$  of a TFET, and we have succeeded in tuning the SnSe TFET from HP device to LP device in this work and extending the BP TFET to LP application.<sup>9</sup> And to import a ferroelectric layer is a remarkable method to improve  $I_{\text{on}}$ . Noteworthy, this vertically stacked modification and negative capacitance introduction of a TFET structure is a prototype method, and could easily apply to other 2D planar TFETs, like the Bi and GeTe TFETs,<sup>8,32</sup> which possess both high  $I_{\text{leak}}$  and  $I_{\text{on}}$  simultaneously.

For the realization of 2D FETs in labs, sub-5 nm traditional FETs are reported based on the channel material of ML MoS<sub>2</sub>,<sup>36</sup> bilayer MoS<sub>2</sub>,<sup>37</sup> and bilayer MoTe<sub>2</sub>.<sup>38</sup> For 2D BP traditional FETs, the shortest experiment reported gate length is 20 nm.<sup>39</sup> As for 2D TFETs, the progress in experiment is much behind the traditional FETs. To the best of our knowledge, there're no reports of 2D TFETs in the nanometer scale. Recently, the

vertical homojunction TFETs based on multilayer BP have been realized in the micrometer scale in labs.<sup>40,41</sup> As an analog of BP, 2D SnSe is widely studied in recent years<sup>42–44</sup> but rarely reported as FET despite its excellent electronic properties like BP and good air-stability over BP. Our theoretical predicted good device performances of the sub-10 nm vertical SnSe homojunction TFET for a fast LP application would certainly encourage the corresponding experimental studies.

## 4 Conclusions

To summarize, we investigate the device performances of the sub-10 nm vertical SnSe homojunction TFETs with *ab initio* quantum transport calculations. The vertically stacked device configuration of the SnSe TFET is beneficial for a fast low-power device in regard to the planar configuration because the broken connected top and bottom layers lead to an enhanced transport barrier.  $SS_{\text{ave},4 \text{ dec}}$  of 44.2–45.8 mV dec<sup>-1</sup> and  $I_{60}$  of 5–7  $\mu\text{A } \mu\text{m}^{-1}$  are obtained for the optimal vertical SnSe homojunction TFET with  $L_g = 10$  nm at  $V_{\text{dd}} = 0.5$ –0.74 V. In terms of  $I_{\text{on}}$ , intrinsic  $\tau$ , and PDP, the vertical SnSe TFETs and NCTFETs outperform the 2022 and 2028 targets of the ITRS low-power device (2013 version), respectively. The impressive performance of the vertical SnSe TFETs would accelerate future TFET manufacturing.

## Conflicts of interest

There are no conflicts to declare.

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