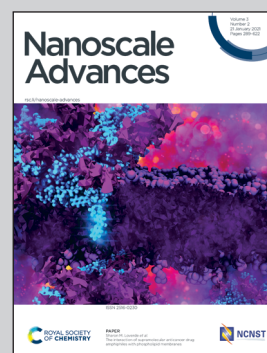


Showcasing research from Professor Zhipei Sun's laboratory, Department of Electronics and Nanoengineering, Aalto University, Espoo, Finland.

Dual-gated mono-bilayer graphene junctions

A dual-gate could be employed to change the Fermi level of monolayer graphene and open a tunable bandgap in bilayer graphene, respectively. Accordingly, an atomically sharp junction could be built at the interface between dual-gated mono- and bilayer graphene. This paper reports the measurement and simulation of the transport properties of dual-gated mono-bilayer graphene junction. The asymmetric transport properties indicate that a tunable junction is successfully built at the interface of dual-gated mono-bilayer graphene, which has the potential to be a promising candidate for functional graphene devices.

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Dual-gated mono–bilayer graphene junctions†

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A lateral junction with an atomically sharp interface is extensively studied in fundamental research and plays a key role in the development of electronics, photonics and optoelectronics. Here, we demonstrate an electrically tunable lateral junction at atomically sharp interfaces between dual-gated mono- and bilayer graphene. The transport properties of the mono–bilayer graphene interface are systematically investigated with I_{ds} – V_{ds} curves and transfer curves, which are measured with bias voltage V_{ds} applied in opposite directions across the asymmetric mono–bilayer interface. Nearly 30% difference between the output I_{ds} – V_{ds} curves of graphene channels measured at opposite V_{ds} directions is observed. Furthermore, the measured transfer curves confirm that the conductance difference of graphene channels greatly depends on the doping level, which is determined by dual-gating. The V_{ds} direction dependent conductance difference indicates the existence of a gate tunable junction in the mono–bilayer graphene channel, due to different band structures of monolayer graphene with zero bandgap and bilayer graphene with a bandgap opened by dual-gating. Simulation of the I_{ds} – V_{ds} curves based on a new numerical model validates the gate tunable junction at the mono–bilayer graphene interface from another point of view. The dual-gated mono–bilayer graphene junction and new protocol for I_{ds} – V_{ds} curve simulation pave a possible way for functional applications of graphene in next-generation electronics.

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Introduction

Two dimensional (2D) materials, such as graphene,¹ transition metal dichalcogenides (TMDCs)² and black phosphorus (BP),³ have been extensively investigated due to their unique physical properties. Until now, plenty of remarkable electronic and optoelectronic properties have been demonstrated in 2D materials,^{4–6} such as ultrahigh carrier mobility of $200\,000\text{ cm}^2\text{ V}^{-1}\text{ s}^{-1}$ and reduced noise levels in suspended graphene,^{7,8} high current on/off ratio of 1×10^8 in monolayer MoS_2 transistors² and ambipolar transport in BP transistors,⁹ as well as an anisotropic photoresponse and chiral light emission in BP and WS_2 based devices.^{10,11} Of particular importance, the electronic structures and physical properties of 2D materials strongly depend on the number of layers, and functional devices can be built based on this principle.^{12–15} For example, mono- and bilayer graphene possess massless Dirac-like energy band and nearly parabolic dispersion, respectively.⁶ The strongly distinct band structures of mono- and bilayer graphene make it possible

to construct a lateral junction with atomically sharp interface.^{16–20} Furthermore, bilayer graphene under dual-gate modulation acquires an opened bandgap as large as 200 meV.^{21,22} Consequently, ambipolar transport and current on/off ratio larger than 10^4 are obtained in dual-gated bilayer graphene.^{23,24}

Here, we investigate the interface between dual-gated mono- and bilayer graphene, with two types of top gate electrodes deposited above the graphene channels, covering only bilayer graphene (local top gate, LTG, Fig. 1a) or the whole graphene channel (global top gate, GTG, Fig. 1b). Transfer curves and I_{ds} – V_{ds} curves of the graphene devices are systematically measured with bias voltage V_{ds} applied in opposite directions along the length of the channel. In addition, I_{ds} – V_{ds} curves of the devices are simulated based on a new numerical model with measured transfer curves as the only input. The results of both measurements and numerical simulation indicate that an electronic junction is successfully built at the mono–bilayer graphene interface, and this junction is considerably enhanced when the doping level of graphene is close to zero. The gate tunable mono–bilayer graphene junction is a promising candidate for the practical applications of graphene.

Results and discussion

Architectures of the two different mono–bilayer graphene devices are demonstrated in Fig. 1a and b. The heavily doped silicon substrate works as the back gate electrode, where back

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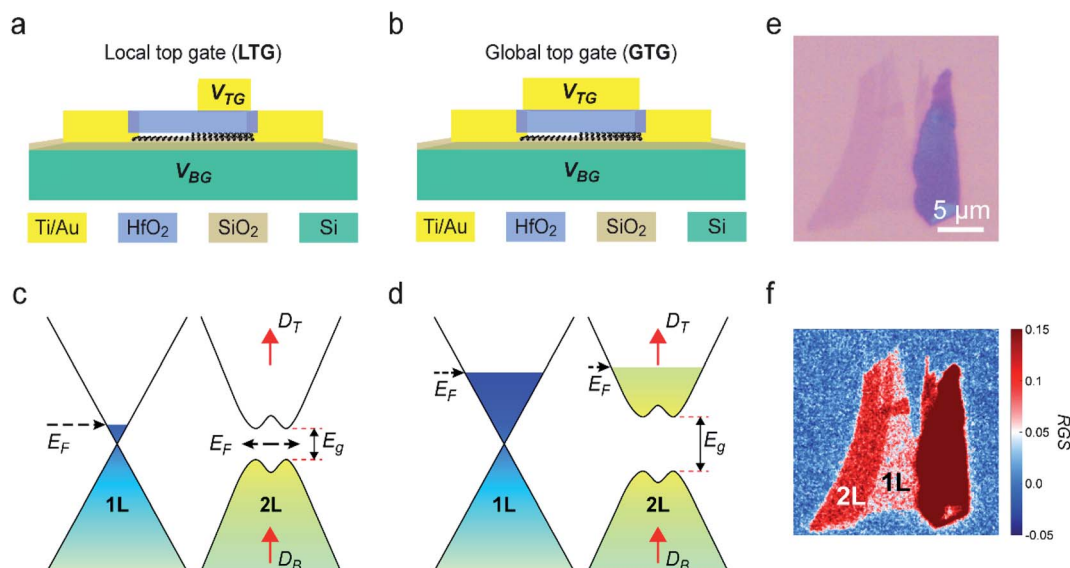


Fig. 1 Structure of mono-bilayer graphene junctions. (a and b) Architectures of dual-gated mono-bilayer graphene junction devices with local (a) and global (b) top gate electrodes. (c) Alignment between the Fermi level E_F of monolayer (1L) and bilayer (2L) graphene when the doping level is close to zero. (d) Alignment between E_F of mono- and bilayer graphene under heavy doping. A bandgap E_g is opened in bilayer graphene in the presence of top and bottom electrical displacement field D_T and D_B . (e) Optical microscope image of a typical mono-bilayer graphene flake. (f) RGS mapping of the flake in (e). The two areas with RGS of ~ 0.06 and ~ 0.12 are mono- and bilayer graphene, respectively.

gate voltage V_{BG} is applied to modulate both mono- and bilayer graphene in the channels. Top gate electrodes with two different coverings are assigned to the devices, to modulate the graphene channels with top gate voltage V_{TG} . The top gate electrode locally modulates bilayer graphene in the LTG device, while it globally modulates the entire graphene channel of the GTG device. In the presence of V_{BG} and V_{TG} , the induced bottom and top electrical displacement field D_B and D_T play a double role. Their difference $D_B - D_T$ determines net doping of mono- and bilayer graphene, and $(D_B + D_T)/2$ gives rise to bandgap opening in bilayer graphene.^{21,23} Therefore, a heterojunction is expected to be built between gapless monolayer graphene and bilayer graphene with an opened bandgap.

Conductance of the dual-gated mono-bilayer graphene is expected to highly depend on the Fermi level, as well as the opened bandgap in bilayer graphene. Here, we define a new parameter “effective gate voltage” ($V_{BG\text{-eff}}$ and $V_{TG\text{-eff}}$ correspond to back and top gate, respectively), that means, the voltage drop between gate electrodes and a point in the graphene channels. For example, when bias voltage V_{ds} is applied on the drain electrode and the source electrode is grounded, the “effective top gate” $V_{TG\text{-eff}}$ in the channel ranges from $V_{TG} - V_{ds}$ at the drain to $V_{TG} - 0$ at the source. $V_{TG\text{-eff}}$ can be approximated uniform in the graphene channel when V_{ds} is remarkably smaller than V_{TG} , whereas it significantly changes along the length of the channel when V_{ds} is comparable with V_{TG} . As illustrated in Fig. S1,[†] when V_{ds} is applied on the electrode connected to monolayer graphene and the electrode connected to bilayer graphene is grounded, $V_{TG\text{-eff}}$ in the monolayer section is lower than that in the bilayer section, and this configuration is called the “Mb” mode. Otherwise, in the opposite case when the V_{ds} is applied on the electrode connected to bilayer

graphene, $V_{TG\text{-eff}}$ in the monolayer section is higher than that in the bilayer section, and this configuration is called the “Bm” mode. Since $V_{TG\text{-eff}}$ directly influences the doping level and further the conductance of graphene, the difference between $V_{TG\text{-eff}}$ in Mb and Bm modes results in different conductance of the graphene channel. Meanwhile, the change of $V_{TG\text{-eff}}$ results in different bandgap opened in bilayer graphene, which contributes to the conductance change of the graphene channel as well. As illustrated in Fig. 1c, when the net doping of graphene determined by $D_B - D_T$ is close to zero, the channel conductance can be readily tuned by a small shift of gate voltage. However, when the net doping of graphene is quite heavy (Fig. 1d), the channel conductance tends to saturate and is almost independent of gate voltage. Therefore, the I_{ds} - V_{ds} curves measured with V_{ds} in opposite directions are expected to considerably differ from each other when the gate voltages approach the charge neutrality point (CNP).

In order to validate the principle design, mono-bilayer graphene flakes are carefully selected after mechanical exfoliation, followed by device fabrication. The optical microscope image of a typical graphene flake is shown in Fig. 1e, and its thickness is characterized by two methods. Based on the Raman spectrum shown in Fig. S2,[†] mono- and bilayer graphene areas in this flake can be identified according to the ratio of 2D/G and Lorentzian fitting of 2D peaks.²⁵ Additionally, the thickness of graphene could be confirmed by means of the relative green shift (RGS) based on optical microscope images.^{26–28} Fig. 1f demonstrates RGS results of this typical graphene flake. The two areas with RGS values of ~ 0.06 and ~ 0.12 are mono- and bilayer graphene. The agreement between the results of Raman and RGS proves the reliability of RGS based graphene thickness identification in our experiments. Details of Raman and RGS



based characterization are explained in the Experimental section. In the following sections, the thickness of the two graphene flakes shown in Fig. S3a and b† is characterized using the RGS method. Based on the RGS results in Fig. S3c and d,† both of the two flakes are composed of distinct mono- and bilayer graphene areas. Next, LTG and GTG dual-gated graphene devices are fabricated with the two flakes through a standard microfabrication process as illustrated in Fig. S4† and described in the Experimental section, and optical microscope images of the fabrication process are shown in Fig. S5.†

Transport properties of the graphene junction devices are firstly investigated using I_{ds} - V_{ds} curves measured in Mb and Bm modes. Fig. 2a–c demonstrate I_{ds} - V_{ds} curves of the LTG device measured at various gate voltages, showing that the I_{ds} of Mb measurements is different from that of Bm measurements. The significant difference between I_{ds} of Mb and Bm measurements is a characteristic of the electronic junction in the mono-bilayer graphene channel, because the I_{ds} of uniform channel

measured in Mb and Bm modes should be the same. It is apparent that this I_{ds} difference can be greatly modulated by V_{TG} and V_{BG} , similar to the modulation of graphene conductance in transfer curves. In addition, I_{ds} - V_{ds} curves of the GTG device measured at various gate voltages are demonstrated in Fig. 2d–f, where less difference between I_{ds} of Mb and Bm measurements is found. In order to quantitatively compare the I_{ds} - V_{ds} curves of Mb and Bm measurements, the ratio of I_{ds} measured in Mb and Bm modes (Mb/Bm I_{ds} ratio) is calculated, and the results of LTG and GTG devices are shown in Fig. 2g and h, respectively. For both LTG and GTG devices, the Mb/Bm I_{ds} ratio maintains ~ 1.0 when $V_{ds} < 0.5$ V, meaning that the mono-bilayer graphene works just like a uniform material. Nevertheless, this ratio greatly fluctuates around 1.0 when $V_{ds} > 1$ V, indicating that an effective electronic junction is built at the mono-bilayer graphene interface. The maximum ratio is achieved at decreased V_{TG} (-3 V, -4 V, and -5 V for the LTG device and 2 V, 0 V, and -2 V for the GTG device) when V_{BG} is increased, as indicated by

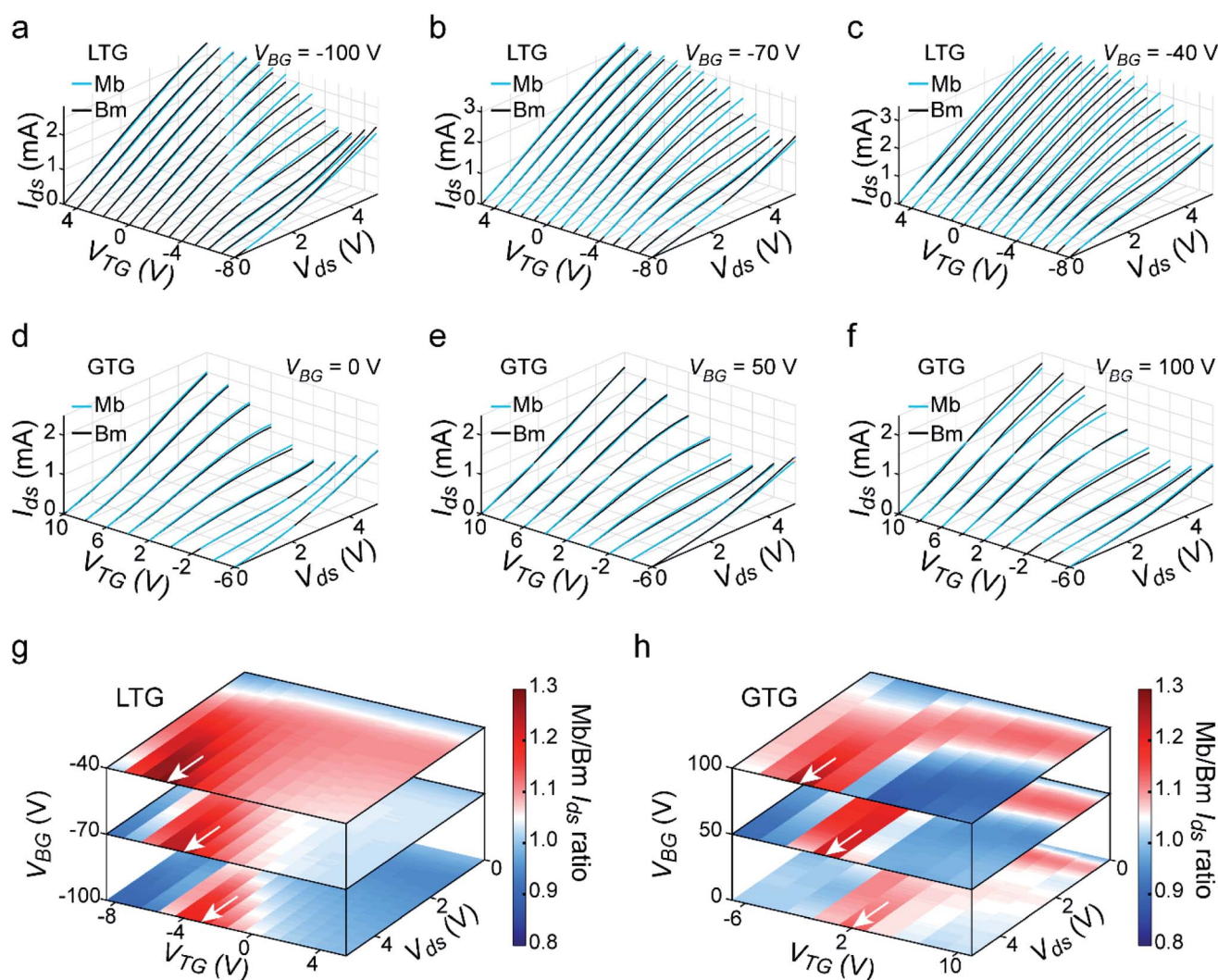


Fig. 2 I_{ds} - V_{ds} curves of mono-bilayer graphene junction devices. (a–c) I_{ds} - V_{ds} curves of the LTG device measured at $V_{BG} = -100$ V, -70 V and -40 V. (d–f) I_{ds} - V_{ds} curves of the GTG device measured at $V_{BG} = 0$ V, 50 V and 100 V. (g) Mb/Bm I_{ds} ratio calculated with the data of the LTG device in (a–c). (h) Mb/Bm I_{ds} ratio calculated with the data of the GTG device in (d–f). The maximum Mb/Bm I_{ds} ratios, as indicated with white arrows, are obtained at decreased V_{TG} when V_{BG} is increased.



the white arrows in Fig. 2g and h. The Mb/Bm I_{ds} ratio can be as high as roughly 1.3, in other words, the difference between I_{ds} of Mb and Bm measurements is around 30%. The reason behind the gate tunable Mb/Bm I_{ds} ratio could be explained by the transfer curves shown in the following section.

Fig. 3a and b show the transfer curves of LTG and GTG devices measured in the Mb mode. For both LTG and GTG devices, V_{TG} at charge neutrality points (V_{TG-CNP}) is shifted approaching negative when V_{BG} is increased from -100 V to 100 V with 10 V steps, indicating that the doping level of graphene is jointly tuned by both V_{TG} and V_{BG} . As shown in Fig. 3a, channel resistance R_{ds} at charge neutrality points (R_{ds-CNP}) of the LTG device has a minimum value of 3.27 k Ω at $V_{BG} = 70$ V, whereas the R_{ds-CNP} of the GTG device monotonically decreases from 21.45 k Ω to 9.48 k Ω as V_{BG} is increased. V_{TG-CNP} values in the transfer curves of Fig. 3a and b are extracted and plotted in Fig. 3c, showing that V_{BG} and V_{TG-CNP} have a roughly linear relationship similar to the published results of dual-gated graphene devices.^{21,29} The transfer curves measured in the Bm mode and corresponding V_{TG-CNP} , as shown in Fig. S6,[†] exhibit little difference from the results in Fig. 3a–c, because the V_{ds} of 0.1 V in transfer curves measurements leads to little difference between V_{TG-eff} in Mb and Bm modes. V_{TG} values for the maximum Mb/Bm I_{ds} ratio indicated with white arrows in Fig. 2g and h are present as red in Fig. 3c. In particular, V_{TG-CNP} of the GTG device at $V_{BG} = 100$ V, 50 V and 0 V are almost the same as V_{TG} where maximum Mb/Bm I_{ds} ratios in the GTG device are achieved. The similar V_{BG} dependence of V_{TG-CNP} and V_{TG} at the maximum Mb/Bm I_{ds} ratios suggests that the junction between dual-gated mono- and bilayer graphene heavily

depends on the overall doping of graphene determined by D_B and D_T . As shown in Fig. 3d, for both the LTG and GTG devices, the maximum Mb/Bm I_{ds} ratio is increased when R_{ds-CNP} is decreased. Since the decreased R_{ds-CNP} mainly results from the decreased bandgap of bilayer graphene, it is reasonable to say that the gate tunable bandgap opened in bilayer graphene contributes to the generation of this directional junction as well.

As further proof of the relation between the mono-bilayer graphene junction and gate voltages, a novel numerical model for simulating I_{ds} - V_{ds} curves based on measured transfer curves is proposed. I_{ds} - V_{ds} curves of graphene devices at high electric field when $V_{ds} \gg 0.1$ V have been extensively studied based on both experimental measurements and theoretical simulation.^{30,31} Results of the various models can perfectly explain and quantitatively fit the measured I_{ds} - V_{ds} curves. Nevertheless, there are multiple parameters (such as gate voltages at CNP, capacitance of dielectric layers, drift velocity of carriers, *etc.*) in these models that need to be measured or estimated initially, increasing a certain degree of difficulty and complexity. For easing the simulation process, a new numerical model is proposed to simulate output I_{ds} - V_{ds} curves with measured transfer curves as the only input, without any additional parameters needed to be measured or estimated. In the new model, every point in the I_{ds} - V_{ds} curves is determined using the formula: $I_{ds} = V_{ds}/R_{ds}$, where R_{ds} is simulated channel resistance based on the measured transfer curves. Taking the measurement of the LTG device at $V_{BG} = -100$ V as an example (Fig. 4a), the low bias voltage $V_{ds} = 0.1$ V in transfer curve measurements has little effect on V_{TG-eff} , therefore V_{TG-eff} is

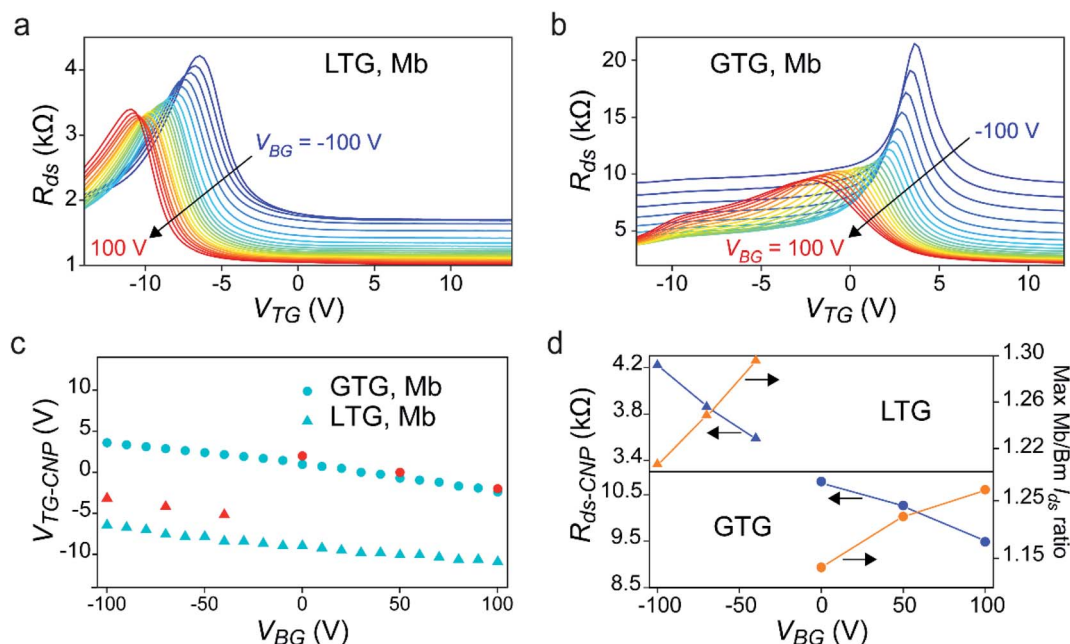


Fig. 3 Transfer curves of mono-bilayer graphene junction devices measured in the Mb mode. (a and b) Transfer curves of LTG (a) and GTG (b) graphene junction devices measured at various V_{BG} . The V_{BG} ranges from -100 V to 100 V with 10 V steps in the measurements. (c) V_{TG} at charge neutrality point (V_{TG-CNP}) of the transfer curves in (a) and (b). The red markers indicate where maximum Mb/Bm I_{ds} ratios are obtained, as shown in Fig. 1(g) and (h). (d) Dependence of R_{ds} at charge neutrality point (R_{ds-CNP}) in the transfer curves and maximum Mb/Bm I_{ds} ratios in I_{ds} - V_{ds} curves on gate voltages.



assumed to be equal to V_{TG} at every point in the graphene channel. The measured transfer curve describes a function: $R_{ds} = f_R(V_{TG})$, as illustrated in Fig. 4b. Since the steps of V_{TG} sweeping are quite small (0.28 V for LTG device measurements and 0.24 V for GTG device measurements), the curve between two measured points can be assumed to be linear. As illustrated in Fig. S7,[†] the corresponding R_{ds} for an arbitrary top gate V_0 can be calculated with the formula: $f_R(V_0) = \frac{f_R(V_1 + \Delta V_{TG}) - f_R(V_1)}{\Delta V_{TG}}(V_0 - V_1) + f_R(V_1)$, where V_1 is the lower V_{TG} point neighboring V_0 in the transfer curve and ΔV_{TG} is the sweeping step of V_{TG} ; details of the derivation of this formula are explained in Fig. S7.[†] When top gate voltage V_{T0} and source-drain bias voltage V_{d0} are applied on the device, the electric potential in graphene channel changes from 0 V at the source (S) electrode to V_{d0} at the drain (D) electrode as illustrated in Fig. 4c. Initially, the distribution of electric potential in the channel is assumed to be linear. Namely, if the positions of the source and drain are defined as $x = 0$ and $x = L$, the electric potential at position x along the channel length is $x/L \times V_{d0}$ (Fig. 4c). As a result, V_{TG-eff} at position x in the graphene channel is $V_{T0} - x/L \times V_{d0}$. Therefore, V_{TG-eff} at different positions in the graphene channel ranges from $V_{T0} - V_{d0}$ to V_{T0} , and total R_{ds} of the channel can be calculated with the transfer curve in the range of $V_{T0} - V_{d0}$ to V_{T0} in Fig. 4b. To calculate total R_{ds} , the whole graphene channel is divided into 100 sections with an identical length of $L \times 1/100$ (Fig. 4d). Effective top gate V_{TG-eff} of the n -th section at $x_n = L \times n/100$ is $V_{T0} - x_n/L \times V_{d0} = V_{T0} -$

$n/100 \times V_{d0}$, and as a result, resistance of this section is $R_n = f_R(V_{T0} - n/100 \times V_{d0}) \times 1/100$. Finally, resistance of the whole channel is calculated as $R_{ds} = \sum R_n = 1/100 \times \sum f_R(V_{T0} - n/100 \times V_{d0})$, and the I_{ds} at bias voltage V_{d0} in I_{ds} - V_{ds} curve is $I_{d0} = V_{d0}/R_{ds}$. The I_{ds} - V_{ds} curves of the GTG device can be simulated in a similar manner, with its own transfer curves as input.

To assess the simulation model, simulated I_{ds} - V_{ds} curves of LTG and GTG devices are compared with respect to the measured results. Fig. 5a-d present the simulated (Sim) I_{ds} - V_{ds} curves of LTG and GTG devices at the gate voltages in Fig. 2c and f, as well as the measured (Mea) results demonstrated for straightforward comparison. Apparently, the simulation accuracy seems quite acceptable at most of the (V_{TG} , V_{ds}) combinations, while the difference between simulated and measured I_{ds} - V_{ds} curves is enlarged at specific (V_{TG} , V_{ds}) combinations. This rule can be quantitatively understood with the ratio of simulated and measured I_{ds} (I_{ds} Sim/Mea ratio) shown in Fig. 5e-h, where the white dashed lines are defined by $V_{TG} - V_{ds} = V_{TG-CNP}$. The I_{ds} Sim/Mea ratio fluctuates between 0.9 and 1.1 at (V_{ds} , V_{TG}) combinations far from the white dashed lines, in other words, the simulation error is less than 10% when the graphene is heavily doped by dual-gating. Therefore, the dual-gated mono-bilayer graphene works like a uniform material as assumed in the simulation model, and this result could be interpreted with the transfer curves in Fig. 2a and b, indicating that R_{ds} tends to be independent of V_{TG} , when V_{TG} is far from CNPs. In contrast, the I_{ds} Sim/Mea ratio at (V_{ds} , V_{TG})

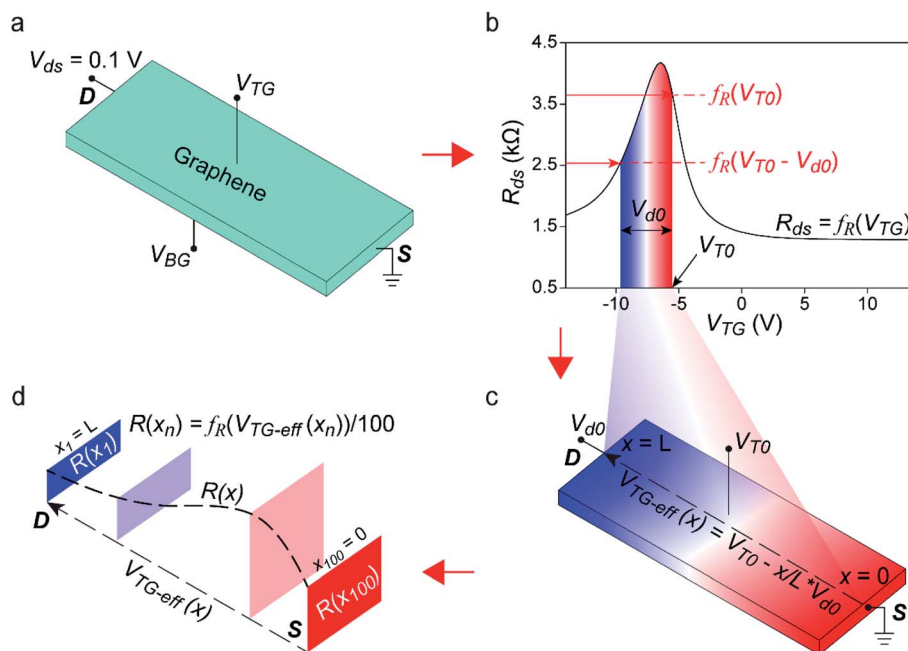


Fig. 4 Schematic of the model for simulating R_{ds} . (a) Nearly uniform distribution of electric potential in the graphene channel when $V_{ds} = 0.1$ V is applied for transfer curves measurements. (b) R_{ds} of graphene channel is assumed to be a function f_R of V_{TG} : $R_{ds} = f_R(V_{TG})$, which is described by the transfer curves. Total R_{ds} of the graphene channel measured at top gate voltage V_{T0} and source-drain bias voltage V_{d0} can be calculated based on the curve in the colored range. (c) When top gate voltage V_{T0} and bias voltage V_{d0} are applied on a graphene device, V_{TG-eff} at different positions in the graphene channel are assumed to linearly change from $V_{T0} - V_{d0}$ at drain (D) electrode to V_{T0} at source (S) electrode. (d) The whole graphene channel is divided into 100 sections along its length, and the resistance $R(x_n)$ of a section at x_n is defined as $1/100$ of $f_R(V_{TG-eff}(x_n))$, $V_{TG-eff}(x_n)$ is the effective top gate at x_n .



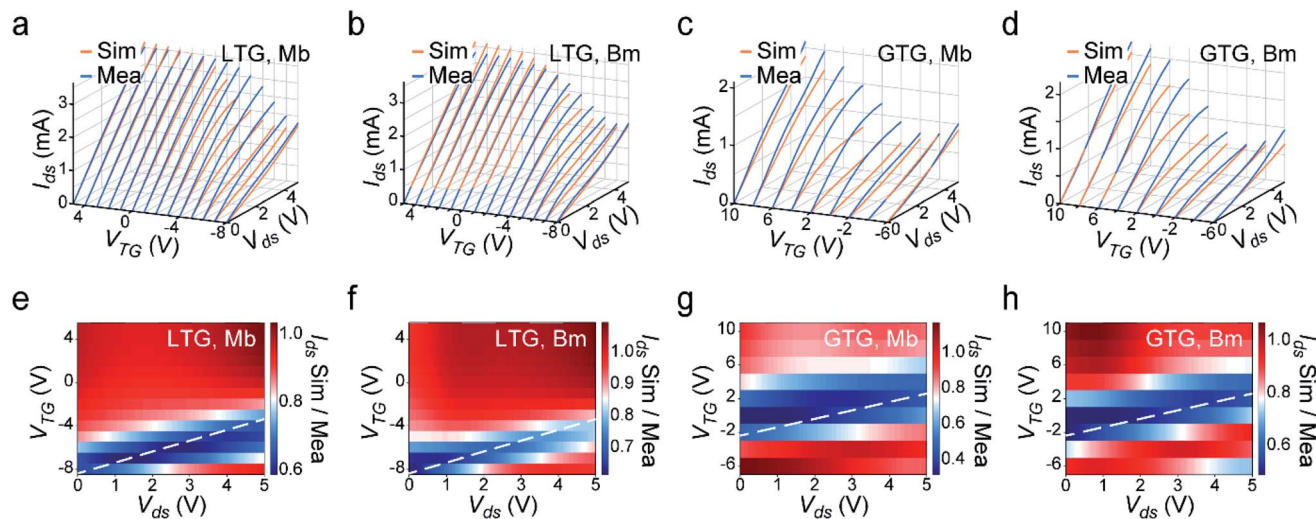


Fig. 5 Comparison between simulated and measured I_{ds} - V_{ds} curves. (a–d) Measured (Mea) I_{ds} - V_{ds} curves shown in Fig. 2 and the simulated (Sim) results based on transfer curves in Fig. 3 and S6.† V_{BG} of LTG and GTG devices are -40 V and 100 V. (e–h) Ratio of I_{ds} Sim/Mea calculated with the data in (a–d). The red areas with Sim/Mea ≈ 1 correspond to high accuracy R_{ds} simulation, while the blue areas with Sim/Mea $\ll 1$ present low simulation accuracy, because the simulated I_{ds} is much smaller than the measured counterpart. The white dashed lines correspond to $V_{TG} - V_{ds}$ equals to V_{TG-CNP} in Fig. 3 and S6.†

combinations close to the white lines can be lower than 0.4. In other words, the simulation error is larger than 60% when the doping level of dual-gated graphene is close to zero, where R_{ds} values of the devices are substantially sensitive to the shift of V_{TG} according to the curves in Fig. 3a and b. The I_{ds} Sim/Mea ratios of LTG and GTG devices under other conditions shown in Fig. S8† also confirm the dependence of simulation error on $V_{TG} - V_{ds}$. Since the graphene channel is assumed to be uniform in the simulation model, the considerable simulation error indicates that the graphene channel does not work as a uniform material, in other words, there is a junction built at the dual-gated mono-bilayer graphene interface. Accordingly, it is reasonable to say that the dual-gated mono-bilayer graphene works like a uniform channel at heavy doping, while like a heterojunction when the doping is close to zero. The gate dependent Mb/Bm I_{ds} ratios and Sim/Mea I_{ds} ratios suggest that a gate tunable electronic junction is successfully built in dual-gated mono-bilayer graphene, and the junction tends to be remarkable when the dual-gating induced doping is close to zero.

Conclusion

In conclusion, directional electronic transport across a dual-gated mono-bilayer graphene interface is systematically investigated, and a new protocol for I_{ds} - V_{ds} curve simulation is proposed. The measured I_{ds} - V_{ds} curves demonstrate that the mono-bilayer graphene has different conductance under bias voltage V_{ds} in opposite directions (Mb and Bm modes), indicating that an electronic junction is built at the atomically sharp mono-bilayer graphene interface. Additionally, the gate dependent Mb/Bm I_{ds} ratio and I_{ds} - V_{ds} curve simulation indicate that this electronic junction is gate tunable, and the junction could be enhanced when the doping level of graphene is close to zero. Overall, the electrical measurements and

numerical simulation prove the existence of a gate tunable junction at the dual-gated mono-bilayer graphene interface. Besides, the proposed simulation model explains I_{ds} - V_{ds} curves at a high electric field in a novel way and simplifies the prediction of output I_{ds} - V_{ds} curves with measured transfer curves. In the future, the mono-bilayer graphene junction can be enhanced by enlarging the bandgap opening of bilayer graphene with novel device structures,^{23,24} thus the junction would be more functional and valuable. These results indicate that dual-gated mono-bilayer graphene junctions are promising candidates for functional electronics in the future.

Experimental section

Preparation and characterization of graphene flakes

Graphene flakes are obtained by scotch tape based mechanical exfoliation of highly oriented pyrolytic graphite (2D semiconductors), and transferred to a cleaned Si wafer with a 280 nm thick SiO_2 top layer. The thickness of graphene flakes is critical in this project, so that they are carefully characterized by two methods before device fabrication. The first method is based on the color contrast of the optical microscope (Olympus BX60) images. Green channel G_0 in the RGB value of pixels in the optical images is extracted with a custom MATLAB script, and RGS is defined as $\text{RGS} = (G_0 - G_s)/G_s$, where G_s is the averaged green value of bare Si/ SiO_2 areas.^{26–28} The areas of mono- and bilayer graphene should have RGS values of ~ 0.06 and ~ 0.12 , respectively. The second method is the Raman spectrum. Graphene flakes are characterized using a Raman spectrometer (Horiba LabRAM HR) with a 514 nm excitation laser. According to the ratio of 2D/G and Lorentz fitting of 2D peaks, areas of mono- and bilayer graphene can be identified.²⁵ Consistency between the results of RGS and Raman characterization



indicates that RGS characterization based on our equipment is reliable for identifying the graphene thickness.

Device fabrication

The graphene devices are fabricated through the process flow illustrated in Fig. S4.† Firstly, source and drain electrodes of 5 nm/100 nm Ti/Au are deposited through standard electron beam lithography (EBL, Vistec EBP 5000), electron beam evaporation (MASA IM-9912) and lift-off process. Graphene areas between the source and drain electrodes are further patterned to a regular shape with EBL and reactive ion etching (RIE, Oxford Instruments PlasmaLab 80 Plus), to avoid the influence of interface states.¹⁶ The residues of EBL resist after RIE is removed with acetone, followed by high vacuum annealing (AML – AWB wafer bonding machine) at 200 °C for 2 hours. Right after annealing, the devices are transferred to evaporation equipment and a 2 nm thick Al layer is deposited on graphene. Subsequently, the Al layer is oxidized on a 130 °C hotplate in air for 3 min to form a Al₂O₃ seeding layer.²⁹ Above the Al₂O₃ layer, a 20 nm thick HfO₂ layer is grown by atomic layer deposition (ALD, Beneq TFS-500) at 200 °C, with TDMAH and water used as hafnium and oxidant sources. Finally, top gate electrodes are deposited through a process same to that of source and drain electrodes. The fabricated devices are connected to a printed circuit board for electrical measurements by wire bonding (Delvotec 53XX). Optical microscope images of the fabrication process are demonstrated in Fig. S5,† showing that source and drain electrodes are arranged to be parallel with the interface between mono- and bilayer graphene.

Electrical measurements

All the electrical measurements in this article are carried out with a semiconductor device parameter analyzer (Agilent B1500A) under ambient conditions. The I_{ds} - V_{ds} curves are measured by sweeping the bias voltage V_{ds} at various combinations of V_{TG} and V_{BG} , and transfer curves are measured by sweeping the top gate voltage at various back gate voltages. All the measurements are conducted at V_{ds} in opposite directions (Mb and Bm modes) along the channel length.

Numerical simulation

Values of simulated R_{ds} and I_{ds} are calculated with a custom MATLAB script based on the measured transfer curves.

Conflicts of interest

The authors declare no competing financial interest.

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