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Uniform self-rectifying resistive random-access memory based on an MXene-TiO_2 Schottky junction†

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For filamentary resistive random-access memory (RRAM) devices, the switching behavior between different resistance states usually occurs abruptly, while the random formation of conductive filaments usually results in large fluctuations in resistance states, leading to poor uniformity. Schottky barrier modulation enables resistive switching through charge trapping/de-trapping at the top-electrode/oxide interface, which is effective for improving the uniformity of RRAM devices. Here, we report a uniform RRAM device based on a MXene-TiO_2 Schottky junction. The defect traps within the MXene formed during its fabricating process can trap and release the charges at the MXene–TiO_2 interface to modulate the Schottky barrier for the resistive switching behavior. Our devices exhibit excellent current on-off ratio uniformity, device-to-device reproducibility, long-term retention, and endurance reliability. Due to the different carrier-blocking abilities of the MXene–TiO_2 and TiO_2–Si interface barriers, a self-rectifying behavior can be obtained with a rectifying ratio of 10^3, which offers great potential for large-scale RRAM applications based on MXene materials.

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Introduction

Metal oxide junctions are one of the most fundamental building blocks for practical electronic devices.[1–3]A Schottky barrier is formed at the metal–oxide interface due to the difference between metal work function and oxide electron affinity.[4] Recently, resistive random-access memory (RRAM) devices based on metal oxide junctions have been increasingly recognized as a mainstream technology to meet the requirements of the rapid development of non-volatile data storage,[5–11] logic operation[12] and neural computing[13–16] due to their simple configuration, and high reproducibility.[11,17,18]

However, due to the stochastic nature of the filamentary resistive switching mechanism, the inevitable variability should be a primary obstacle for RRAMs.[19,20] Theoretically, conductive filaments across the junction can be formed/ruptured by the redox process,[21] migration of oxygen vacancies,[11,22] or diffusion of atoms/ions of active metal electrodes,[23] depending on the various metal oxide junctions.[19,24–26] Nevertheless, switching between different resistance states is usually abrupt, and the random formation of conductive filaments usually makes large fluctuations of both resistance state and operating voltage, which greatly weakens the reliability of memory devices, and will either falsely program/erase the storage cell or make the storage states unrecognizable, imposing challenges to the peripheral sensing and programming circuits.[19] Therefore, seeking a resistive switching mechanism that could eliminate the involvement of the prominent local conductive filamentary is impending for the development of uniform RRAM devices.

Another acknowledged resistive switching mechanism is the field-induced modulation of the Schottky barrier profile, which usually occurs on the entire interface between the electrode and oxide to improve the uniformity. It is well accepted that the interface state seriously affects the formation of the Schottky barrier, and the field-induced modification of the interface state contributes to the memory effect.[27] The charge carriers injected from the electrodes may be trapped by charge traps in a storage medium to form a space charge, which can either modulate the barriers to injection of the charge carriers from the electrodes or affect the transport process of charge carriers through the storage medium, thereby leading to the resistive switching behavior.[25] Furthermore, by inducing a Schottky contact or asymmetric barrier into a charge trapping/detrapping system, a charge-trap-associated self-rectifying RRAM can be obtained to deal with the sneak path problem that leads to the misreading, false program and additional power consumption

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in a high-density, massively parallel crossbar array.[28–31] Therefore, designing a Schottky junction with abundant charge traps within the metal-oxide interface should be feasible to fabricate uniform self-rectifying RRAM devices.

MXenes are a new class of transition metal carbides or nitrides, which are widely used in electronic devices as electrode materials due to their excellent metallic conductivity and good hydrophilicity.[32,33] It is worth noting that during the preparation of MXenes, when a certain A atomic layer is removed from the MAX phase precursor by hydrofluoric acid etching, some adjacent atoms will inevitably fall off, leading to the disordered anion–cation vacancies or vacancy clusters, which greatly increase the trap density of MXenes inherently.[34–36] Recently, as the wafer-scale MXene film patterning with high resolution has been realized,[37] it opens up new avenues for designing highly-active and long-life electrode candidates for fabricating uniform RRAMs based on the interface-trap modulation model.

Here, we report a uniform RRAM device with the MXene-TiO_2 Schottky junction, while MXene and TiO_2 are used as the top-electrode and resistive layer, respectively. The resistive switching behavior comes from the MXene-TiO_2 junction, where the barrier profile is electrically modulated. The charge carriers injected from the MXene top-electrode can be trapped by charge traps within the MXene-TiO_2 interface to modulate the barriers. As a result, our device exhibits the uniformity of current on–off ratio with a standard deviation less than 0.25, device-to-device reproducibility, long-term retention of 10^4 s, and reliable endurance. Moreover, by introducing the bottom electrode with silicon, a self-rectifying behavior can be obtained with a rectifying ratio of 10^3 due to the different carrier-blocking abilities of the MXene-TiO_2 and TiO_2–Si interface barrier.

Results and discussions

Device design and characterization

Fig. 1a shows the schematic of a RRAM comprised of a MXene top-electrode, TiO_2 resistive layer and p^+-Si bottom-electrode. The fabricated device features an effective electrode junction

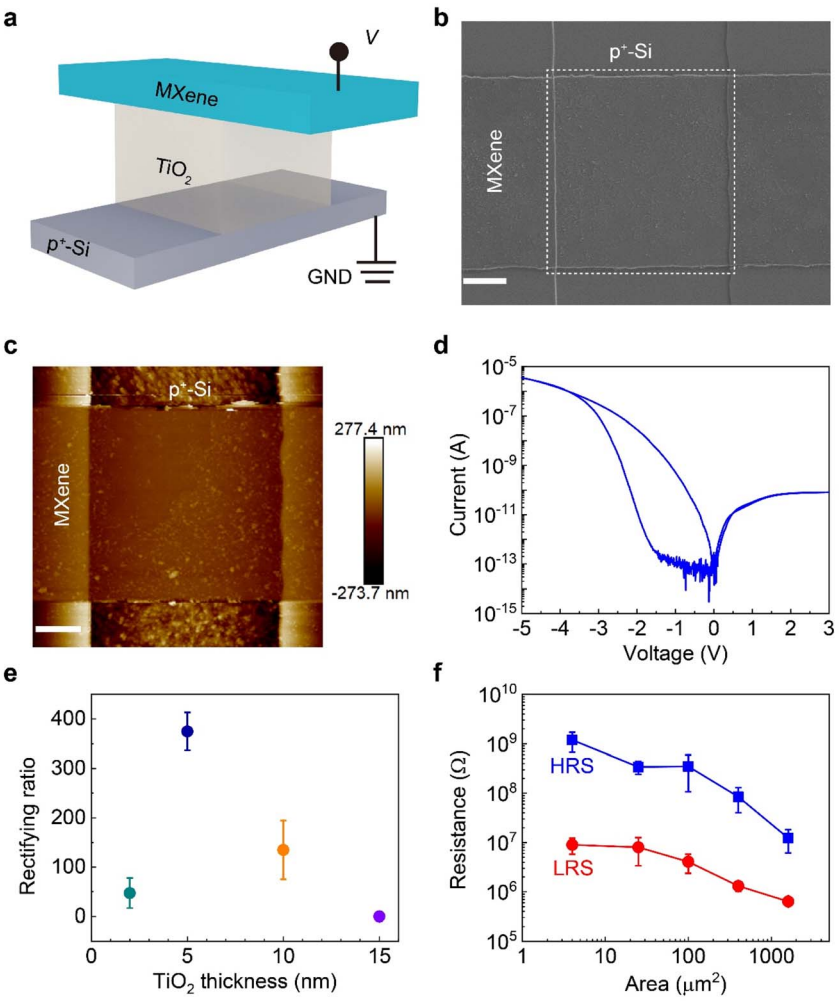

Fig. 1 Device design and characterization. (a) Schematic of a MXene-TiO_2-Si RRAM. (b) SEM image of the crossbar structure with a resistive area of 10 μm × 10 μm denoted by white dash lines. Scale bar, 3 μm. (c) AFM image of the morphology of a 25 nm-thick MXene film. Scale bar, 2 μm. (d) Typical *I*–*V* characteristic of a MXene-TiO_2-Si RRAM indicates the self-rectifying switching behavior. (e) Rectifying ratio of the RRAMs as a function of various TiO_2 thicknesses, calculated from the *I*–*V* characteristics of 5 devices for each TiO_2 thickness. (f) Relationship of the resistive area and the performance of MXene-TiO_2-Si self-rectifying RRAMs, extracted from the *I*–*V* characteristics of 10 devices for each resistive area.

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area of 10 μm × 10 μm, which is denoted by white dash lines in Fig. 1b. Fig. 1c shows an AFM image of the morphology of the deposited uniform MXene film with 25 nm as the top-electrodes according to the height profile (ESI Fig. S1†).

A typically measured current–voltage (*I–V*) characteristic of the device shows that the self-rectifying behaviors are realized successfully with a rectifying ratio of approximately 10^3 (Fig. 1d). During the SET process, when the SET voltage (V_{SET}) is approximately −2 V, the conduction of the resistive layer changes from a high-resistance state (HRS) to a low-resistance state (LRS), thereby switching the device to the ON state. During the RESET process, a RESET voltage (V_{RESET}) of 2 V is applied to "erase" the device and causing it to return to the OFF state, with the conduction of the resistive layer changing from the LRS to the HRS, where the current is evidently suppressed. The rectifying ratio is calculated by the currents at −2 V and 2 V (ESI Fig. S2†). It is also appropriate to set the read voltage of ±2 V due to the stable read disturbance for HRS and LRS with a current on–off ratio of approximately 10^2 (ESI Fig. S3†).

To determine the appropriate device structure, a comparison of RRAM switching behaviors with different thicknesses of TiO_2 as the resistive layer has been carried out, as shown in Fig. 1e, indicating that the optimum thickness of the TiO_2 resistive layer is 5 nm. As a matter of fact, at the ON state, a thinner TiO_2 film can result in the tunneling of charge carriers under the bias voltage, while a thicker TiO_2 film can be considered as a good dielectric to impede the conduction between the top and bottom electrodes completely without any resistive switching behaviors (ESI Fig. S4†). An appropriate thickness is helpful for the construction of devices with a better rectifying ratio.[38,39] In our study, as the TiO_2 thickness increases, the Schottky barrier height and contact resistance can be reduced; however, the thicker TiO_2 has a larger series resistance leading to the degradation of device performance at the contact.[40] As a result, 5 nm-TiO_2 should be just appropriate for obtaining the largest rectifying ratio by balancing the effects on the Schottky barrier height and series resistance simultaneously.

Fig. 1f shows the relationship between the resistive area and the performance of RRAMs extracted from the *I–V* characteristics of 10 devices each with different geometries (ESI Fig. S5†). Note that both the resistance of HRS and LRS decrease with the increased resistive area. Such an area-sensitive characteristic of the resistance states confirms the field-induced modulation of the Schottky barrier profile occurred on the entire MXene–TiO_2 interface.[4] In addition, the current of our devices with the smallest resistive area is more than 2 nA, which is big enough to read. In the practical chip design, even the current of fA level can be collected by adding auxiliary circuits, such as operational amplifiers.[41–43]

To verify the Schottky junction between MXene and TiO_2, we directly connect two probes with MXene and TiO_2, respectively (Fig. 2a). As a result, there is no rectifying behavior obtained in the case of either MXene or TiO_2 connected with two probes. We directly measure the *I–V* characteristic of the TiO_2–Si junction with a typical diode behavior (ESI Fig. S6†). When the MXene–TiO_2 junction is tested, one probe is connected with the MXene and the other is connected with TiO_2. Consequently, an obvious rectifying behavior is obtained, and we deduced that a Schottky

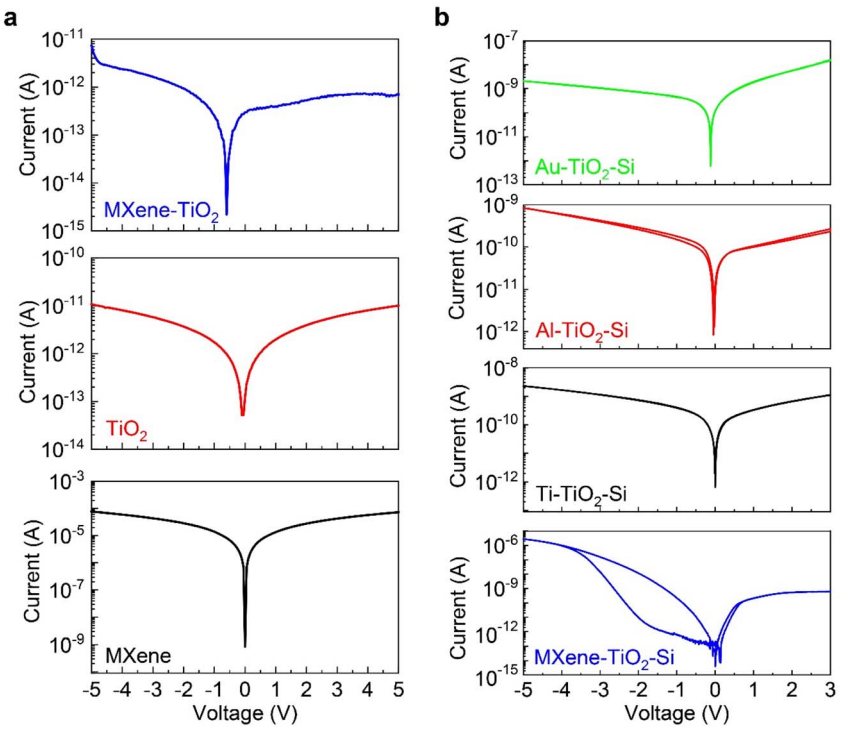

Fig. 2 a) *I–V* characteristics of the MXene–TiO_2 junctions, TiO_2 and MXene films. (b) Performance comparison of the RRAMs with various top-electrodes including Au, Al and Ti and MXene. The resistive area and the performance of MXene-TiO_2-Si self-rectifying RRAMs, extracted from the *I–V* characteristics of 10 devices for each resistive area.

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junction is formed between MXene and TiO_2 as a metal–semiconductor contact. Furthermore, several RRAMs using different metal materials as the top-electrodes have been fabricated to explore the importance of MXene, including Al, Ti and Au. As a result, no matter what kind of the metal top electrode is, no resistive switching behavior is observed for these RRAM devices (Fig. 2b) due to the lack of sufficient traps within the metal–TiO_2 interface.[44,45] Therefore, we clarify that the intrinsic traps of MXenes play an essential role in the switching of the resistance flow process.[46–49]

Switching retention and endurance are critical to evaluate the reliability of RRAM devices. As shown in Fig. 3a, the retention characteristics of the MXene-TiO_2-Si RRAM show that the HRS is not significantly degraded after 10^4 s, but the LRS increases slightly. This is because the modulation of the Schottky barrier at the HRS is stable and easily realized. However, for the LRS, it suggests that some electrons may be injected from the MXene electrode and occupied the charge traps entering the interface. As a result, some positive charge traps are neutralized and the Schottky barrier within the interface is recovered leading to a slight increase in resistance. Moreover, the endurance characteristics show a stable operation of 100 cycles (Fig. 3b). Actually, our RRAM device could be also maintained beyond 100 cycles depending on how to set the pulsed voltage stress (ESI Fig. S7†). In addition, to predict the lifetime of our RRAM devices, we have investigated the retention and endurance characteristics at different temperatures (ESI Fig. S8†). It is explicit that the stable retention and recognizable on/off behaviors are still maintained. According to the Arrhenius equation, the activation value E_a of our device is calculated as 1.78 eV, and the extrapolated retention time of our device at room temperature could be approximately 10^8 s (ESI Fig. S9†), which is estimated by temperature-dependence of the retention time following the Arrhenius equation. In fact, there is little degradation of LRS at a higher temperature. This is because the stability of LRS is related to the activation energy of the material, and the greater the activation energy, the poorer the thermal stability of LRS.[50] In addition, compared with some thermal-stability RRAM devices,[51,52] the E_a of our RRAM device is a little larger leading to the degradation of LRS at a higher temperature. All these results can prove the high reliability of the MXene-TiO_2-Si RRAM devices for long-term data storage.[49]

Fig. 3c shows the cumulative probability of 100 individual MXene-TiO_2-Si RRAMs based on the resistance of HRS and LRS with a device-to-device variation less than one order of magnitude indicating the good uniformity. Fig. 3d illustrates the statistical distribution of rectifying ratio extracted from 50 individual RRAMs (ESI Fig. S10†). Due to the logarithmic operation, the mean rectifying ratio is actually 4×10^2 with a standard deviation of approximately 0.25. Moreover, we also provide the *I*–*V* characteristics of a RRAM with 80 switching cycles ((ESI Fig. S11†) and plot the statistical variation of rectifying ratio from cycle-to-cycle. As a result, the rectifying ratio only distributed from 10^2 to 10^3, indicating the excellent cycle-to-cycle uniformity (ESI Fig. S12†). The narrow distribution of switching voltages and resistance states illustrates the robust programming/erasing of the memory or making the storage states recognizable. Similarly, even though the bottom electrode is replaced by n-Si, the self-rectifying behavior and retention characteristics of the MXene-TiO_2-n-Si are also achieved,

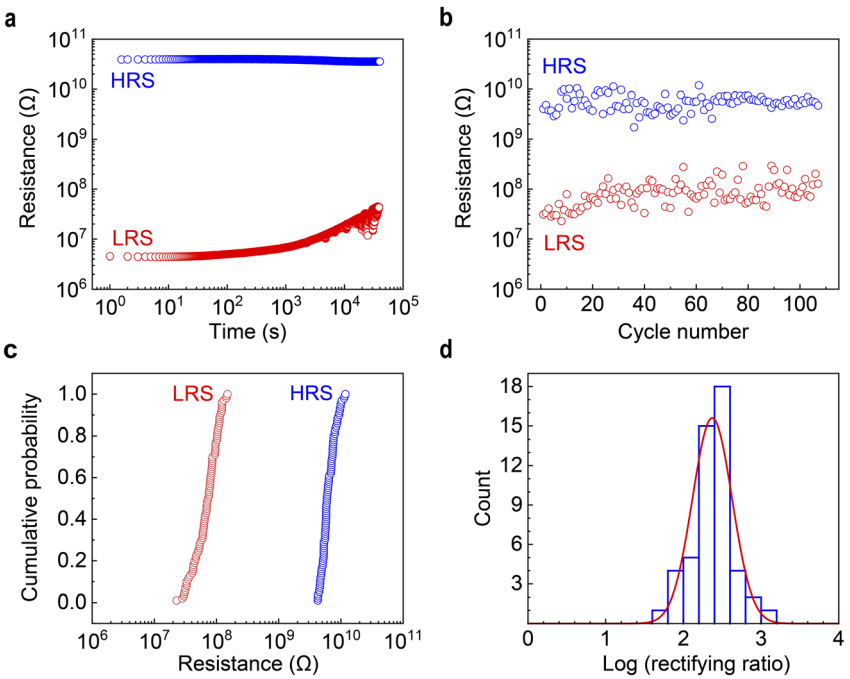

Fig. 3 Evaluation of the electrical performance. (a) Retention and (b) endurance characteristics of the MXene-TiO_2-Si RRAM obtained at ±2 V and the room temperature. (c) Device-to-device cumulative probability of 100 individual MXene-TiO_2-Si RRAMs based on the resistance of HRS and LRS. (d) Statistical distribution of rectifying ratio of 50 MXene-TiO_2-Si RRAMs with a standard deviation of 0.25.

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indicating the excellent reliability and stability of MXene–TiO_2 Schottky junction for fabricating the uniform self-rectifying RRAM devices (ESI Fig. S13†). All of these critical metrics can compare favourably with the reported TiO_2-based RRAMs[23,26,49,53–56] (ESI Table S1†).

Mechanism

The proposed mechanism of MXene-TiO_2-Si RRAM about the resistive switching and self-rectifying behaviors is elucidated. Theoretically, in the interface-type charge trapping/de-trapping mechanism, there are charge traps at the interface of the Schottky junction, and the trapping and de-trapping of charges can modulate the height of the Schottky barrier to induce the resistance transition.[19–23,53] In addition, the occupied state of the charge traps is affected by the carriers injected from the electrodes.[17] A reverse bias voltage relative to the Schottky barrier causes the trapped charges and increases the interface resistance, while a forward bias voltage makes the interface traps to release the trapped charges, thereby decreasing the interface resistance.[25–27]

As shown in Fig. 4a, when a relatively large negative bias is applied to the Schottky interface, electrons are extracted from the defect, resulting in the accumulation of positive charge traps at the interface, which changes the distribution of the potential at the interface. In order to maintain the suppression of the Fermi level position between MXene and TiO_2, the height of the Schottky barrier at the interface is reduced leading to the decrease of the interface contact resistance, while the device is transformed into LRS; however, when a large positive bias is applied, a large number of electrons are injected into the interface and fill the charge traps, thereby neutralizing these positive charge traps and restoring the interface Schottky barrier, while the device transitions back to HRS.[56–59]

Fig. 4b shows the absorbance spectra, which demonstrate the bandgaps of TiO_2 and p^+-Si are 1.70 eV and 1.12 eV, respectively. Therefore, the self-rectification of the device is approved based on the basic energy band structure of each material (Fig. 4c), which is drawn through their work function and other parameters (ESI Fig. S14†).

When the device is negatively biased (Fig. 4d), it is easier for carriers to cross the Schottky barrier between MXene and TiO_2,

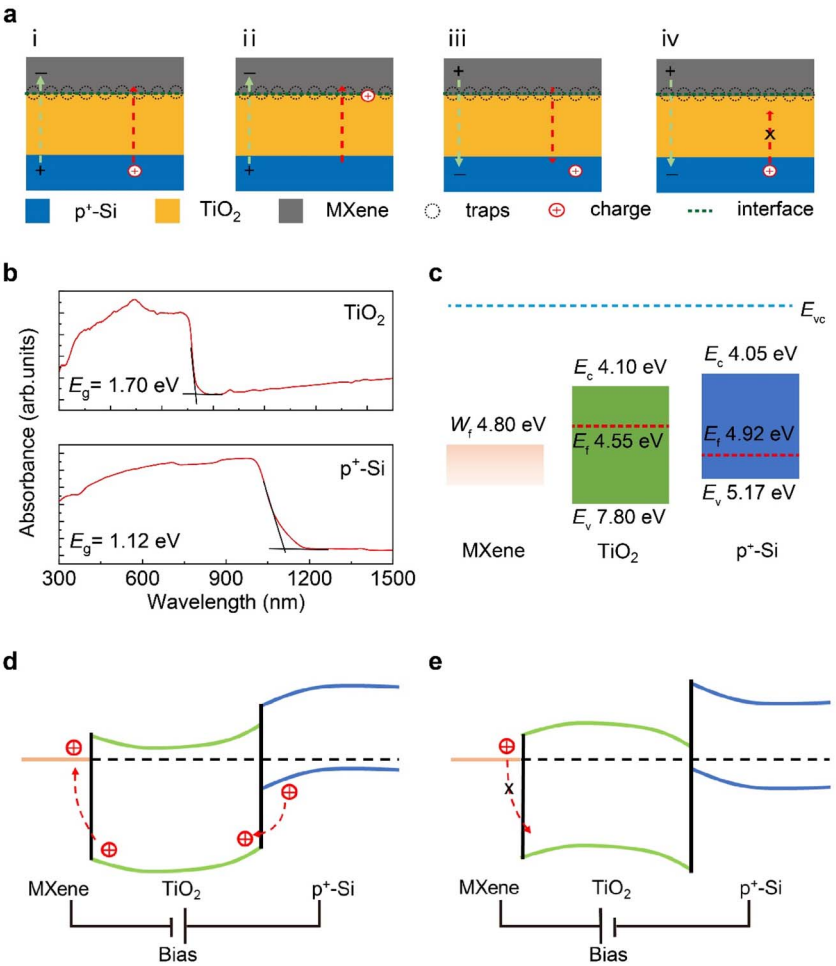

Fig. 4 Mechanism. (a) Resistive switching of the MXene-TiO_2-Si RRAM device (i. $V = V_{SET}$, ii. Trap, iii. Detrap, iv. $V = V_{RESET}$). (b) Absorbance spectrum of TiO_2 and p^+-Si. E_g is the bandgap. The red line is an auxiliary line for extracting E_g. (c) Energy band diagram of MXene, TiO_2 and p^+-Si. Band diagram of the MXene-TiO_2-Si heterojunction under (d) negative and (e) positive bias.

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allowing more current to flow through the device in the ON state. Conversely, when the device is positively biased (Fig. 4e), it is difficult for carriers to pass through the Schottky barrier between MXene and TiO_2 due to the different carrier-blocking abilities of the MXene–TiO_2 and TiO_2–Si interface barrier, resulting in the device self-rectifying behavior.[60]

In the case of n-Si, when n-Si contacts with MXene to form a Schottky junction, the holes as primary carriers cause the opposite built-in electric field inside this junction compared with p-Si. Therefore, under the same bias voltage, the voltage has the opposite effect on the device switching behavior.

Conclusions

We report a new design method to fabricate uniform self-rectifying RRAM devices with a rectifying ratio of approximately 10^3 based on the MXene–TiO_2 Schottky junction. The defect traps within MXene formed spontaneously during its preparation process play an essential role in the modulation of the Schottky barrier by charge trapping/de-trapping as a storage medium at the entire MXene–TiO_2 interface. Our devices exhibit the excellent uniformity, device-to-device reproducibility, long-term retention, and reliability, which paves a new path for the fabrication of large-scale memory devices based on MXene materials.

Material preparation

The MXene used for the top electrodes comes from a colloidal $Ti_3C_2T_x$ solution. First, Ti_3AlC_2 powder (2 g) synthesized using a high-temperature solid–liquid reaction was slowly added to an HCl solution (40 mL, 9 M) with LiF (2 g), preparing a $Ti_3C_2T_x$ suspension. Then, $Ti_3C_2T_x$ slurry was obtained by vacuum filtration and cleaned by deionized (DI) water until pH reaches 5, while the $Ti_3C_2T_x$ suspension was poured onto a porous filter membrane after the solution stops bubbling. At last, a colloidal $Ti_3C_2T_x$ solution was obtained after sonication of the $Ti_3C_2T_x$ slurry diluted with DI water for 30 min.

Other chemicals used include remover PG (MicroChem), CD-26 developer (MicroChem), acetone, isopropanol and ethanol. All chemicals were directly used without any further purification.

Fabrication of RRAM device

In a typical preparation, a heavily doped p^+-Si substrate with 100 nm SiO_2 (Silicon Quest International, Inc.) was firstly cleaned with acetone and isopropanol for 5 min each, followed by purging with nitrogen gas. The cleaned substrate was then patterned by standard photolithography and etched by reactive ion etching (15 sccm Ar, 20 sccm CHF_3, 20 sccm CF_4) to remove the redundant SiO_2 to expose p^+-Si, and it was used as the bottom electrode. To improve the cleanliness of the substrate, the oxygen plasma treatment was further applied for 10 min at 200 W and O_2 of 180 sccm. Subsequently, a 5 nm-thick TiO_2 was deposited on the bottom electrodes by atomic layer deposition (ALD) at 250 °C (precursor: tetraisopropyl titanate, TTIP and H_2O). According to the constant height profile and X-ray photoelectron spectroscopy of the structure of the bottom Si electrode before and after ALD, it is explicit that there is no redundant SiO_2 at all within the TiO_2–Si interface (ESI Fig. 15†). After that, MXene ($Ti_3C_2T_x$, 10 mg mL^{-1}) was spin-coated at 2000 rpm for 1 min to prepare the uniform MXene thin-films for the top-electrodes. The patterned Al (60 nm) was then prepared on the MXene as the metal mask, and the redundant MXene outside the electrode area was removed by reactive ion etching at 4 Pa, 5 W and 20 sccm CF_4 for 2.5 min. Finally, the Al metal mask was removed by immersing it into CD-26 developer for 2 min at room temperature, cleaned with DI water for 1 min, and then purged with nitrogen gas (ESI Fig. S16†).

Characterization of material and device

The fabricated devices were characterized using an optical microscope (Nikon ECLIPSE LV100ND), a scanning electron microscope (SEM, FEI Nova NanoSEM430, acceleration voltage of 1 kV), and an atomic force microscope (AFM, Bruker Dimension Icon). A semiconductor analyzer (Agilent B1500A), a probe station (Cascade M150) and an input signal generator (Tektronix AFG 3022C) were used to measure the electrical performance under ambient conditions, including retention and endurance characteristics. An ultraviolet-visible-near infrared spectrometer (UV-VIS-NIR Spectrometer, UV3600 Plus) was used to measure the absorbance spectrum. A Kelvin probe force microscope (KPFM, MultiMode 8, Bruker, Inc.) was used to measure the work function.

Author contributions

Y. S. and D. M. S conceived and designed the experiments. C. Z., Y. S. and B. L. performed the device fabrication, electrical characterization and the bandgap evaluation for the device mechanism. F. S. performed the SEM characterization of the device structure. X. Z. W performed the AFM characterization of MXene morphology. C. Z. performed the ALD of TiO_2 for the resistive layer. X. H. W. prepared the MXene solution. Y. S. and D. M. S. co-wrote the paper. All authors discussed the results and commented on the manuscript.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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