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Brain-inspired computing: can 2D materials bridge the gap between biological and artificial neural networks?

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This modern era of technology with data flood actively demands the development of excellent non-volatile storage (NVS) and computing devices, which can overcome the memory bottleneck of the traditional von-Neumann structure-based devices. Memristors, as potent and promising NVS devices, can efficiently mimic the biological synapse of a neuron, and therefore, have been immensely explored in recent years. In this context, the emergence and development of two-dimensional layered materials (2DLMs) have led to a multifold acceleration in the advancement of memory devices, owing to their atomically thin structures and superior electronic properties, in comparison to those of the conventional metal oxides. However, unlocking the full potential of 2DLMs in neuromorphic applications demands creative approaches. Here, we discuss in depth the challenges and limitations associated with these neuromorphic devices and finally conclude by outlining future perspectives and directions for this evolving field of next-generation electronics.

1. Introduction

In this modern digital world, data has become the new wealth.[1,2] Complementary metal oxide semiconductor (CMOS) technology has achieved remarkable milestones, transforming the electronics landscape. Its low power consumption, high integration density, and reliability have revolutionized microelectronics. Innovations in CMOS technology have paved the way for development of smaller, faster, and more energy-efficient devices, such as microprocessors, memory chips, and sensors. This technology has played a pivotal role in the digital revolution, enabling the development of smartphones, computers, and advanced communication systems. Advancements in CMOS technology continue to drive progress in emerging fields like the Internet of Things (IoT), artificial intelligence (AI), and quantum computing, showcasing its enduring impact on diverse technological domains.[3] One of the remarkable achievements is the development of FinFET (Fin Field-Effect Transistor) technology, which emerged as a breakthrough in CMOS design.[3–5] This three-dimensional transistor structure helped overcome some of the limitations of traditional planar transistors, allowing for better control over current flow and reduced leakage, thereby enhancing performance and energy efficiency. CMOS technology has also enabled the integration of an entire system onto a single chip, leading to the development of System-on-Chip (SoC) designs. This integration has resulted in smaller, more compact, and power-efficient devices, ranging from smartphones to IoT devices.[6] Another interesting area that the researchers are exploring is the use of quantum dots in transistors to push the limits of traditional CMOS technology. Quantum dot transistors have the potential to offer improved performance, energy efficiency, and novel functionalities compared to conventional transistors.[7–9] However, as the CMOS-based devices continue to show a decrease in dimensions and reach their physical limits, the continuation of Moore's law faces tough challenges.[10,11] Hence, innovative and efficient memory devices are being continuously explored to meet this rising demand.[10] AI, neural networks, and machine learning have played a vital role in the recent development of memory and data storage devices.[12] In conventional von Neumann computing devices, the processing and the memory units are different, and the mismatch of the speed between data fetching and processing leads to lower efficiency and higher power consumption, referred to as the von Neumann bottleneck.[13] However, in contrast to the von Neumann architecture, the human brain comprises a network of billions of neurons and synapses for information storage and transfer.[13] The brain can process and store multitudes of information simultaneously, thereby making the human brain the most advanced supercomputer that exists today. If the intelligence of the brain is mimicked in the state-of-the-art technology, next-generation energy efficient machines could be designed that can evolve and learn like the brain (Fig. 1). It has spurred tremendous research on devices that

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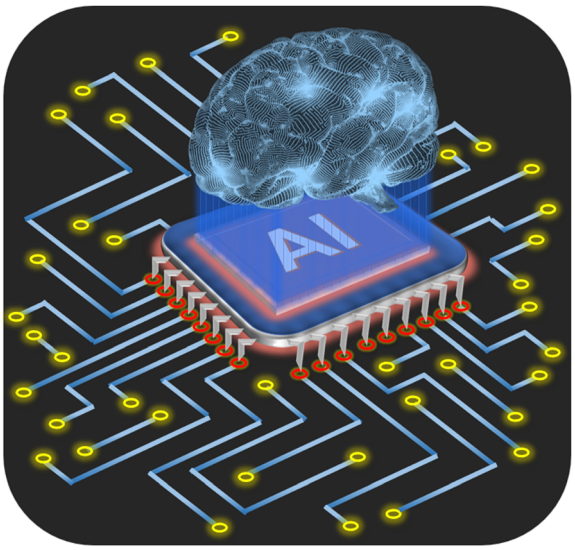

Fig. 1 Schematic depicting the integration of the human brain with modern day processors to produce neuromorphic devices.

can mimic the functionality of biological neurons. Devices that exhibit resistive switching (RS) or memristive behavior have garnered the most attention due to their ability to be utilized as potential synaptic hardware systems while consuming very low energy, fulfilling the criteria of brain-inspired or neuromorphic computing.[14–18] A memristor is a device proposed by Prof. Chua in 1971, considered as the 'fourth fundamental non-linear circuit element' relating charge with magnetic flux, and is characterized by a pinched hysteresis in its *I–V* curve.[19]

The term ''neuromorphic'' was coined in the late 1980s by Carver Mead,[20] who pioneered the development of neuromorphic silicon neuron circuits. Conventional electronic materials have played a major role in the early accomplishments of neuromorphic computing.[21–26] For instance, Zhang *et al.*[27] have implemented a robust machine-learning classifier in a standard 6T static RAM (SRAM) array. It is a prototype 128 × 128 SRAM array that has been applied in a 130 nm CMOS process. Frenkel *et al.*[28] have introduced ODIN, an online-learning digital spiking neuromorphic processor, in a 28 nm fully depleted silicon on insulator CMOS that measures 0.086 mm^2 and has 64 000 synapses, 256 neurons, and a minimum energy per synaptic operation of 12.7 pJ. Other well-known examples include the SpiNNaker Project,[29] part of the European Union Human Brain Program, which can do cognitive tasks, and the TrueNorth chip from IBM, which can identify different objects from video feeds in real-time.[30] The IBM's TrueNorth chip,[31] which consists of 4096 cores and 5.4 billion transistors and integrates 1 million programmable spiking neurons and 256 million adjustable synapses, makes full use of the matured silicon technology and is a good choice for multi-object detection and classification. Another step forward in this direction was the development of the Loihi chip from Intel,[32] which was unveiled in 2017. It features 128 neuromorphic cores, each of which contains 1024 basic spiking neural units arranged in tree-like architectures, for a total of over 131 thousand simulated neurons and nearly 130 million synapses. In contrast to the TrueNorth chip, the Loihi chip supports self-learning based on spiking neural networks in addition to inference. However, these CMOS-based devices may not be the eventual solutions for futuristic AI requirements, since these devices possess complex circuit topologies that consume a lot of power and require a large amount of chip area, in addition to the limitations in further scalability due to decline in the CMOS growth. Recently, two-dimensional (2D) materials have been actively deployed to fabricate various electronic and optoelectronic devices.[33–42] Their high charge carrier mobility,[43–45] band gap tunability,[46] high light absorption coefficient,[40,45] ease of heterojunction formation,[47] and high surface-to-volume ratios[48] make them promising candidates for realizing RS memory and other neuromorphic circuit elements.[10,12,49] Furthermore, van der Waals (vdW) heterojunctions synthesized by stacking two or more 2D layered materials (2DLMs) not only retain the properties of the individual 2D materials, but also exhibit more intriguing properties than the respective counterparts.[43] Recently, several 2DLMs and their heterostructures have been successfully utilized in memristive devices, for instance, graphene,[50] layered metal chalcogenides,[51,52] MXenes,[53] and various other 2D materials.[54] Wang *et al.*[55] have discussed in detail the huge potential of 2DLMs in the development of low power and multifunctional neuromorphic devices, with respect to advancements in the device, chip and circuit levels. The rigorous efforts in the search for novel 2DLMs and their heterostructures along with the progress in their high-quality and wafer-scale growth have proven to be critical for exploiting memory devices with new operational mechanisms. Moreover, it is equally important to explore new architectures for neuromorphic devices, which could be crucial for enhancing the overall figures of merit of these devices. The authors have also discussed the unique properties of various 2DLMs, for instance, (i) the gate-tunable physical properties of 2DLMs enable the realization of diverse optoelectronic devices; (ii) the semimetallic nature of graphene and other transition metal dichalcogenides (TMDCs) makes them suitable for use as electrodes in these memory devices; (iii) effective suppression of operating current due to low density of states in graphene reduces energy consumption; (iv) 2DLMs exhibit much higher mechanical strength as compared to conventional metal oxides, which is crucial for achieving reliable resistive switching characteristics. Chiang *et al.*[56] have also elucidated the utilization of 2DLMs in different memory devices based on their physical properties, such as ferroelectricity, ferromagnetism, phase change characteristics, filament formation, *etc.* In particular, they have emphasized the novel $MoTe_2$-based resistive random-access memories (RRAMs), whose functionality depends upon the electric field-driven transition between two crystalline phases. Additionally, they have also provided an experimental demonstration of a proof-of-concept heterostructure made up of $MoTe_2$ and WSe_2 with appropriate properties for RRAM integration. However, relentless investigation still needs to be done so as to fully unveil the potential of these 2DLMs towards the realization and actualization of futuristic memory technologies.

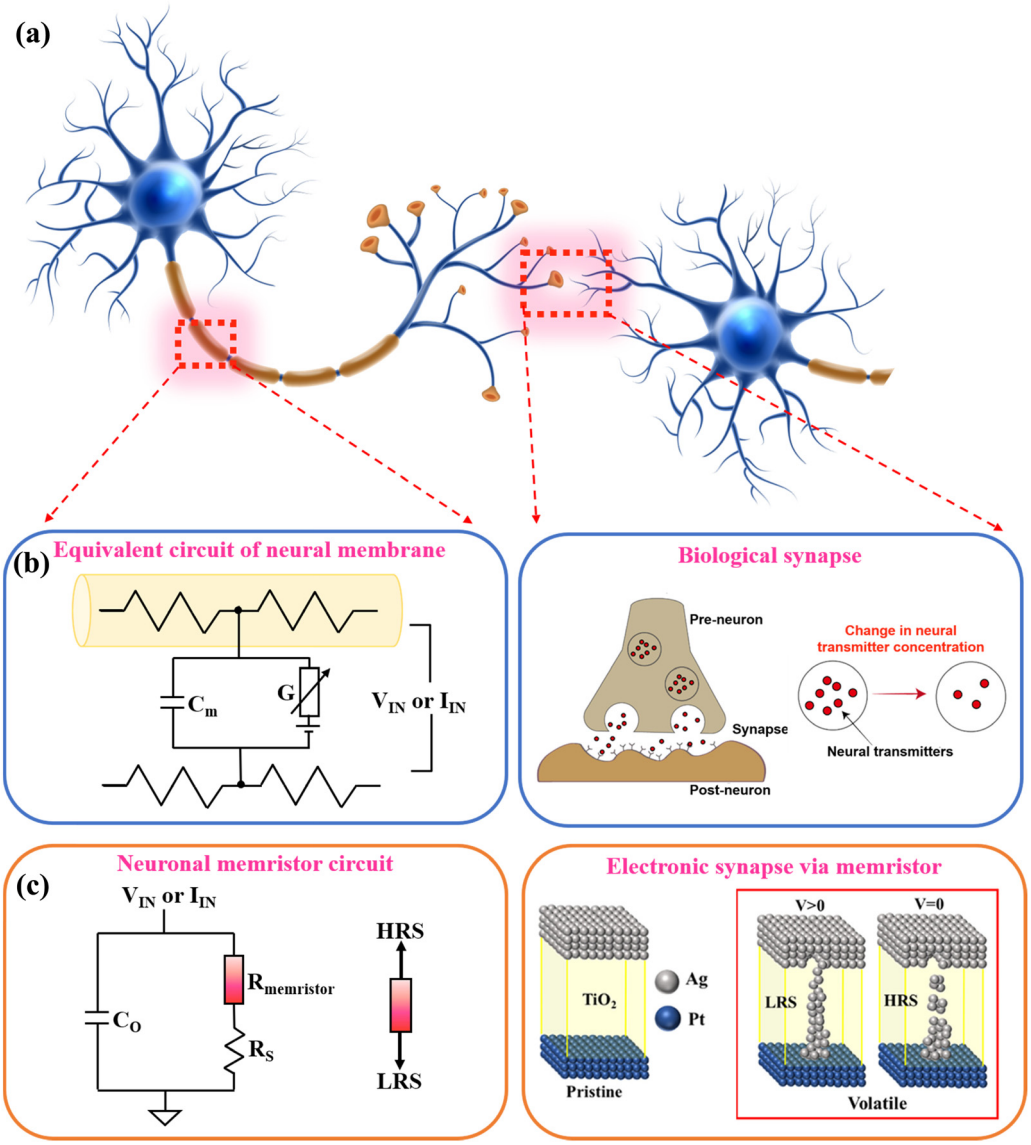

Fig. 2 (a) Schematic depicting biological connectivity in neural organisms, showing the fundamental components *i.e.* a neuron and synapse. (b) Electrical model of the neural membrane; by adjusting the concentration of neuronal transmitters at the synapses, neural systems can exhibit adaptive behavior. Reproduced with permission from ref. 13 and 57. Reprinted with the permission of AIP Publishing; copyright 2018, Frontiers. (c) Equivalent electrical circuit utilizing a memristor to mimic the neural membrane; electronic memristor synapse structure (Ag/TiO_2/Pt) that mimics a biological synapse. Reproduced with permission from ref. 13, 14 and 57. Reprinted with the permission of AIP Publishing; copyright 2023 and American Chemical Society; copyright 2018, Frontiers.

Neural networks are designed utilizing two essential building blocks – neurons and synapses, as depicted in Fig. 2(a). The parallel connection of membrane capacitance (C_m) and membrane conductance (G) can be used to mimic the membrane of a biological neuron (Fig. 2(b)).[13,57] When the membrane capacitance voltage crosses a threshold, the membrane conductance may undergo a change in its resistance, thus exhibiting multiple conductance states. Fig. 2(b) also depicts a synapse, which is the second essential neuromorphic building element. The synapse serves as a location for storage and modification of the input's weight (also known as the synaptic weight). These modifications are achieved by adjusting the concentration of neurotransmitters in synapses.[13] Fig. 2(c) shows the utilization of memristors in artificial neural circuits to emulate biological neurons and synapses. In the last few years, various reviews and perspectives have come up that have investigated this exciting field from the perspective of electrical properties of the devices, different materials for RS, device architectures, memristive synapses and the underlying mechanisms, external stimuli to achieve RS, *etc.*[12,58,59] and concluded by providing a brief discussion of the challenges and outlook. However, a comprehensive discussion regarding the current hurdles in the field of brain-inspired computing is still lacking. Moreover, there is a huge need to shed light on the strategies to overcome these challenges for the fabrication of next-generation devices. Therefore, in this Perspective, we focus mainly on the challenges and limitations

in the field of 2DLM-based neuromorphic devices reported to date, and discuss the plausible solutions for these challenges in terms of different growth techniques, design methods, utilization of novel materials such as phase change materials (PCMs), plasmonic metal nanoparticles, *etc.* We mainly highlight all the possible approaches and unexplored pathways to design highly efficient devices for this emerging research field.

2. Types of neuromorphic devices

Memristors encompass a wide range of electronic devices. They all carry out the fundamental functional concept of a memristor, despite using various structures, materials, and operating systems. Here, based on their structural differences, we divide the various memristors into two groups.

2.1. Two-terminal devices

These can either have lateral or vertical architecture, involving a single active material or a heterojunction.[60,61] Currently, the most popular types of memristors in this category are the cation- and anion-based ones. The input of these two-terminal memristors is typically a fixed voltage across the device; the synaptic weight of the device can be understood as its conductivity or the channel current at a fixed input voltage.[62] The electric field causes anions or cations to migrate when a voltage is applied across the device, progressively forming filaments between the electrodes that alter the resistance. Oxygen vacancies are thought of as the migratory species in anion-based memristors, and oxides are typically utilized in their fabrication,[62] such as TiO_2,[63] WO_3,[18] *etc.* On the other hand, the metal cations from the electrodes form the filaments in cation-based memristors. In this instance, the active anode (Ag or Cu) and inert cathode in this memristor are typically separated by a solid electrolyte.[64] Additional techniques for fabricating a two-terminal memristor have also been explored. For example, ferroelectric devices are subjected to electrical inputs that cause the ferroelectric materials to gradually polarize. By modifying the carriers' injection or tunneling, the degree of polarization influences the conductivity.[65,66] Other types of memristors that have been researched are the spin-based ones; examples of these include spintronic and spin transfer torque magnetoresistive RAM memristors.[67,68] The major ways to optimize two-terminal memristors are use of novel materials or modification of the existing ones by doping. Modifying the device's fabrication methods and/or structure is another way to optimize.[62]

2.2. Three-terminal devices or memtransistors

Memristive behavior can also be obtained using three-terminal devices, which are typically field effect transistors,[69,70] and are usually vertical devices utilizing a single or hybrid active material. The input and output ports of a three-terminal device are dependent upon the testing setup, in contrast to the input/output ports of a device with two terminals, where these are the same since the voltage can only be produced by the two electrodes through which the current passes. A dielectric layer separates the gate from the source/drain and the channel in a three-terminal device, and so the only current passing through a memristor is the channel current.[62] As a result, the source–drain port must be the output port. Conversely, the drain–source port or the gate-source/drain port can be used as the input port. In three-terminal memristors, the memristive function is often dependent on the gate terminals. Almost always, the gate voltage efficiently tunes the carrier activity by causing a gradual change in the channel area or the dielectric/channel interface. The fundamental needs of a memristor – conductivity tuning and memory – can be met if this change is long-lasting. For these devices, it is quite hard to discover a common optimization technique since different types of transistor-based memristors have distinct operating mechanisms behind the memristive functionalities.[62]

3. Different mechanisms of resistive switching

The basic principle behind any RS behavior is the existence of the active material in more than one interchangeable conductance states, which are termed a high resistance state (HRS) and low resistance state (LRS).[4] The switching between these multiple conduction states upon the application of external stimuli, such as light, bias, pressure, temperature, *etc.*, leads to the phenomenon of RS. Different mechanisms have been observed behind this reversible switching between the various conduction states, which have been reviewed here (Fig. 3).

3.1. Defect migration along grain boundaries

This mechanism is generally found in devices with lateral architecture, where the defects present in the system move towards the grain boundary upon application of an external stimulus, thereby creating a low resistance path for conduction. For instance, Sangwan *et al.*[71] have demonstrated a single layer MoS_2-based lateral device where the accretion of the sulfur vacancies along the grain boundaries leads to the changes in the conductance of the MoS_2 channel upon application of different biases, thereby causing memristive switching. Defect migration primarily occurs along grain boundaries due to the lower activation energy required for diffusion compared to migration through the bulk material. Grain boundaries provide energetically favorable pathways for defect migration, allowing defects to move and accumulate along these interfaces. These lateral memristors that make use of defect migration have the advantage of being able to produce multi-terminal and gate-tunable memristors, as well as eventually scaling a device down to atomic thickness. However, further requirements include carefully regulated defect engineering and lowering the operation voltage while maintaining a stable operation in devices in order to construct a memristor with the desired features.[12]

3.2. Phase change materials

Certain materials like VO_2 undergo phase transitions between metallic (LRS) and semiconductor states (HRS)[72–74] to exhibit neuromorphic properties. Similar to this unique feature of

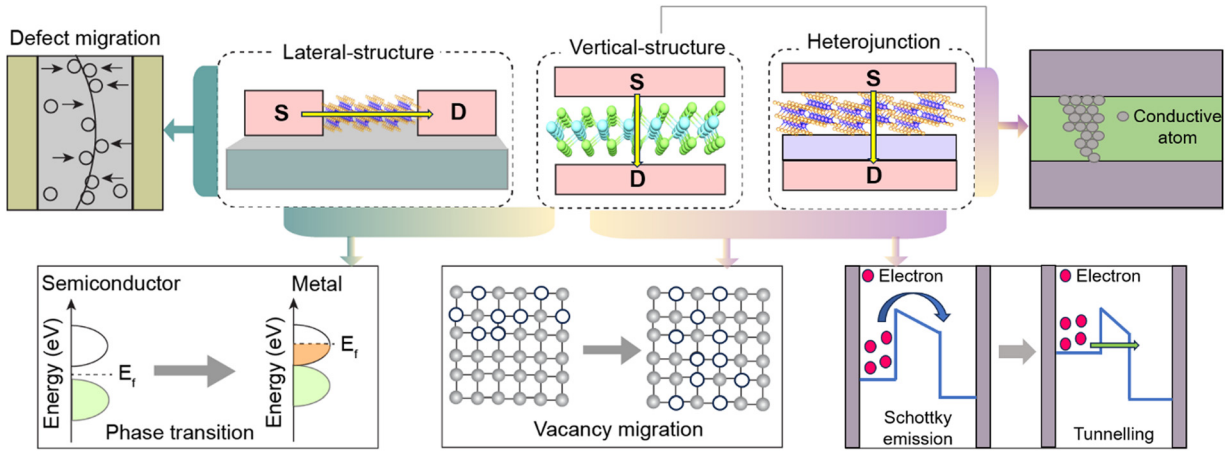

Fig. 3 Schematic depicting common mechanisms of RS. Reproduced with permission from ref. 12. Copyright 2020, John Wiley & Sons, Inc.

correlated oxides, several 2D materials such as MoS_2, WTe_2, $MoTe_2$, TaS_2, *etc.* have been stabilized in their low resistance phase (such as the metallic (1T) phase in MoS_2),[17,75] which can be reversibly switched to their high resistance phase (for instance, the hexagonal (2H) phase in MoS_2). These kinds of phase transitions have been demonstrated both in vertical and lateral devices, usually by application of external bias. Cheng *et al.*[17] have demonstrated an MoS_2-vertical memory device with a simple metal–semiconductor–metal architecture. The active MoS_2 layer contains 92.5% of the 1T phase and the remanent is the 2H phase. This 1T phase has an octahedral structure, and density functional theory calculations predict reversible semiconductor-to-metal transition in this phase owing to strong interactions between different orbitals. From the electrical measurements, the semiconductor-to-metal phase transitions occur at very low bias values, signifying the typical bipolar RS mechanism. Phase change memristors can switch between resistance states very quickly, on the order of nanoseconds to microseconds. This high-speed operation makes them suitable for applications where rapid switching is required, such as in memory and logic circuits. These memristors have also been exploited to realize neuronal memristor circuits, which mimic the behavior of neurons and generate action potentials,[57] as depicted in the left panel of Fig. 2(b) and (c). Furthermore, these memristors typically exhibit good endurance and retention characteristics along with high scalability, allowing for high-density integration on semiconductor chips. However, certain disadvantages are also associated with the PCM-based memristors. When compared to other non-volatile memories, these memristors exhibit high RESET voltage, which is required to cause local heating sufficient for the material layer to undergo phase switching.[76] Moreover, these devices are also associated with temperature sensitivity, which may impact the performance of the device. Variations in temperature might cause inadvertent resistance changes, which can affect the precision and consistency of data that are stored. There is also a change in the crystal structure linked to these phase transitions. Consequently, over time, mechanical wear and tear brought about by frequent structural transitions causes a decline in the device's performance.[13]

3.3. Conductive filament

This mechanism is mostly observed in the case of two-terminal devices, as discussed previously. Formation and rupture of conductive filaments is the most observed RS mechanism in vertical and lateral devices with the metal–semiconductor–metal or metal–insulator–metal configuration, where the active layer can be any oxide, a 2DLM, *etc.* In such configurations, a semiconducting film is sandwiched in between an active and an inert electrode. Ion-related migration and redox processes frequently result in the formation of localized conduction channels in the devices, and this process is aided by the external electric field. The migration of active metal ions is a significant subset of ionic effects. Conductive filaments in these memristors form and spontaneously rupture as a result of the active electrode materials (such as Ag or Cu), due to their limited thermodynamic stability and high diffusivity,[77] being oxidized ($X \rightarrow X^{n+} + ne^-$) and the generated cations migrating towards the inert electrode and being reduced ($X^{n+} + ne^- \rightarrow X$).[78] Therefore, the growth and dissolution of these conductive filaments realized by the electrochemical redox reactions taking place at each electrode/semiconductor junction and the subsequent transport of ions results into the RS behaviors. Such memristors have been recently utilized to achieve volatile switching behavior, emulating nociceptive behavior.[14] Yin *et al.*[79] have demonstrated an electrochemical metallization memory device based on the migration of Ag ions on the surface of 2D MoS_2 to form conducting filaments comprising Ag NP chains of diameter ~5 nm in its LRS. The biggest advantage of this mechanism is that a very large variety of materials can be used to obtain switching behavior, which makes it very promising for future applications. However, as already discussed, the device's low repeatability is caused by its inability to control the production and rupture of these nanofilaments, which has made it difficult to use the device in practical applications. Moreover, this mechanism is only

possible in devices with relatively thin active layers; otherwise, a high power consumption is required for the formation of these conductive filaments. Another drawback is the formation of dead cells from these filaments, which can cause short circuits in devices.

3.4. Vacancy formation and migration

Similar to the conducting filament-based memristors, the defects present in the system can form a vacancy-induced conductive filament (VICF) under application of an electric field, which results into the HLRS. Therefore, numerous families of compounds including oxides, sulfides, selenides, tellurides, *etc.* exhibit this mechanism, which gives it an upper hand for fabricating memristors. This mechanism is also analogous to the migration of defects along the grain boundaries, with the only difference being that these VICFs can be formed anywhere in the 2DLM layer, unlike the case where the defects line up along the grain boundaries. This mechanism is commonly observed in vertical devices with both metal-active layer-metal and heterojunction-based configurations. Devices dominated by ion transport appear to have superior retention performance, making them more attractive for applications like data storage.[80] Such devices usually show digital RS, which has applications in RRAMs.[60] Moreover, for applications involving data encryption and cybersecurity, the stochasticity in this switching behavior can be utilized as a real random number generator.[81] Chen *et al.*[82] reported a carbon-doped h-BN memristor, with a controlled number of defects induced by modulating the weight percentage of the carbon powder during synthesis. The defects in h-BN form a VICF when an electric field is applied, and the device exhibits bipolar NVS capability with low energy consumption along with a long retention time. Precise control over defect engineering becomes critical in such devices, which determines the performance of these memristors. Randomness in the formation of vacancy filaments, which leads to cycle-to-cycle and device-to-device variations, is one of the key issues that needs to be addressed in order to realize efficient, reliable and practical devices.

3.5. Modulation of Schottky emission

Another interesting mechanism in memristive devices is the reversible transition of the carrier transport between Schottky emission and other mechanisms, such as direct tunneling, Ohmic conduction, *etc.*[60] The alteration in the Schottky barrier height of the metal/semiconductor contact or the heterojunction is the key for RS. The continuous tunability of the resistive state is the most crucial aspect of the device in these cases, and hence electron-transport-dominated devices are significant for electrically simulating synaptic properties or learning/memory behaviors.[80] Type-II heterojunctions, which can be transformed into type-III heterojunctions, can potentially change their conduction mechanism from Schottky emission to tunneling.[47] The advantage of such memristors is that the thickness of the active layer can be reduced to the sub-nanometer range, without being affected by the leakage current due to atomic defects. However, higher energy required to alter the barrier height poses limitations on such memristors. Moreover, obtaining significant modulation in the barrier height is very crucial to achieve an appreciable HRS/LRS ratio. In 2018, Ge *et al.*[83] reported a stable non-volatile atomristor based on the Au–MoS_2–Au vertical device, showing RS. The device exhibited the HRS in the Schottky emission transport and the LRS when the carrier transport transitioned to direct tunneling.

4. Common terminology in neuromorphic computing

By exploiting suitable mechanisms discussed above, the performance of memristors can be modulated and enhanced. The performance can be evaluated through various critical parameters that determine their behavior. These parameters play a crucial role in understanding and designing memristor-based devices for specific applications. Some of the key critical parameters of memristors have been defined and are summarized in Fig. 4 and the common terminologies related to neuromorphic computing are summarized as follows:

4.1 Neurons

Neurons are the basic building blocks of the nervous system and brain, which receive sensory information from the outside environment and are responsible for sending motor commands to our muscles, and converting and relaying electrical signals at each stage.

4.2 Synapses

Synapses are the junctions between two neurons, which transmit information between these two neurons in the form of electrical and chemical signals.

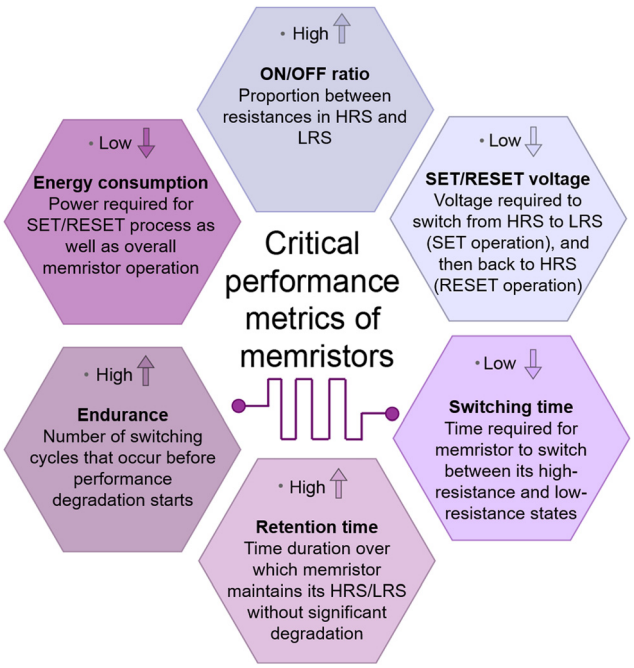

Fig. 4 Critical parameters for evaluation of the performance of memristors.

4.3 Synaptic weight or synaptic plasticity

Synaptic weight or synaptic plasticity refers to the amplitude or strength of a connection between two neurons.

4.4 Spike timing dependent plasticity

Spike timing dependent plasticity is the process that alters the strength of the connection between two neurons, which is based upon the relative timing of the input and output action potentials of a particular neuron.

4.5 Spike rate dependent plasticity

Spike rate dependent plasticity involves the modulation of synaptic plasticity based on the average firing rate or the firing frequency of the action potentials.

4.6 Short term memory (STM)

Short term memory (STM) involves the gradual increase of the synaptic weight, which persists for a short period of time (a few seconds or minutes).

4.7 Long term memory (LTM)

Triggering the STM repeatedly results into a long-lasting modification of the synaptic plasticity, which can last for months or years, and sometimes indefinitely.

4.8 Long term potentiation

Long term potentiation is the procedure that involves consistent synaptic strengthening, resulting into an increase in the signal transmission between neurons over time.

4.9 Long term depression

Long term depression is the process through which synapses lose some of their efficacy to transmit neural signals.

4.10 Non-volatile storage (NVS)

Non-volatile storage (NVS) is a memory that retains the stored data for a long time, even after the power is turned off.

4.11 Volatile memory

Volatile memory is memory that can retain the data for short time periods, only up to the time it gets a power supply.

4.12 Paired-pulse facilitation (PPF)

Paired-pulse facilitation (PPF) refers to the typical change in the short-term synaptic weight controlled by the temporal relationship between the two consecutive presynaptic electrical spikes. For instance, if two successive presynaptic action potentials occur at the presynaptic terminal having a time interval (Δt), then PPF is defined as the ratio of the postsynaptic currents because of the second spike (I_2) and first spike (I_1), that is, PPF = I_2/I_1.

5. Roadmap of memristive and neuromorphic devices

A brief timeline of some of the major milestones achieved in the field of neuromorphic computing is shown in Fig. 5. After the theoretical prediction of a memristor by Chua *et al.*[19] in 1971, immense efforts have been made to implement it in an electrical circuit. A few decades later, in 2008, Strukov *et al.*[63] from Hewlett–Packard Laboratories first revealed that memristive behavior can be experimentally realized in a real device utilizing the Pt/TiO_2/Pt structure. The migration of oxygen vacancies in the TiO_x layer, which caused the gradient change of the doping state, is responsible for the observed memristive switching characteristics. The initial application of synthetic synapses made of carbon nanotubes was first shown in 2013 by Gacem *et al.*[84] Two years later, the first report on a 2DLM-based memristor was published by Sangwan *et al.*,[71] in which an MoS_2 monolayer-based field effect

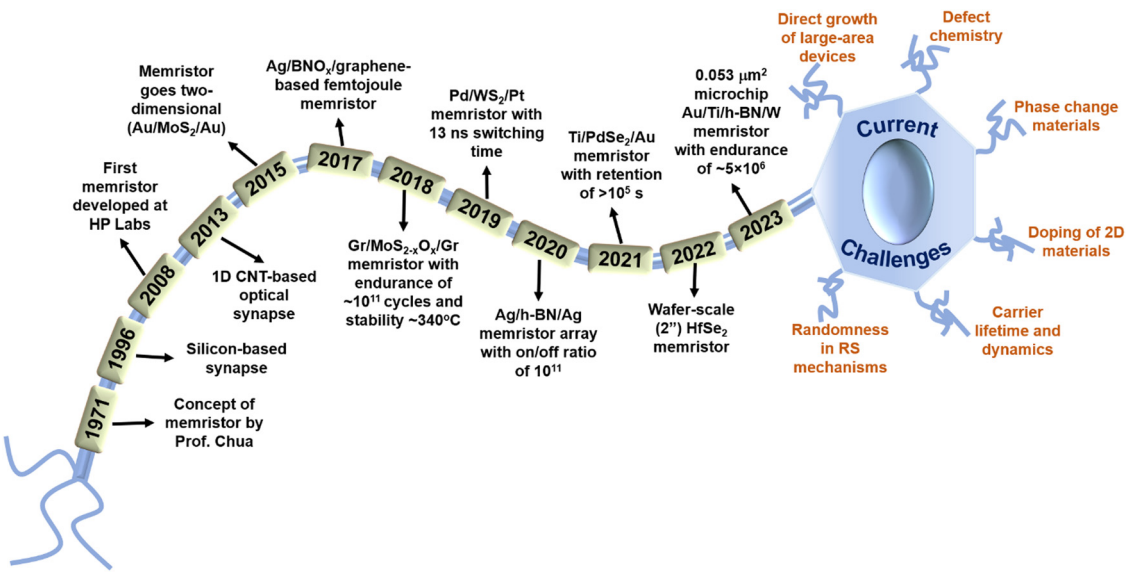

Fig. 5 Schematic showing important milestones and the current challenges in the area of brain-inspired computing.

transistor was utilized. The RS behavior in the three terminal device was attributed to the geometry of the grain boundaries present in the MoS_2 layer. Zhao *et al.*[85] in 2017 investigated the resistive switching of conductive filaments in a material medium with a sub-nanometer thickness for the first time. The oxidation of 2D hexagonal boron nitride (h-BN) was employed, which created an atomically thin switching medium layer. The resulting memristor device can function at femtojoule level energy usage per bit, sub-picoampere on-state current, and less than 1 V working voltage. Later, Wang *et al.*[86] demonstrated a vdW heterostructure utilizing graphene/$MoS_{2-x}O_x$/graphene with superior thermal stability. With an endurance of up to 10^7 cycles and a high operating temperature of 340 °C, the device exhibited exceptional switching capability. The high thermal stability has been attributed to the $MoS_{2-x}O_x$ switching layer, the graphene electrodes, and the atomically sharp interface between the electrodes and the switching layer. Yan *et al.*[87] have shown that 2D WS_2 with a 2H phase can produce high-performance memristors with low power consumption, which exhibit quick ON and OFF switching times of 13 and 14 ns, respectively, along with a low program current of 1 A in the ON state, and SET/RESET energy is on the order of femtojoules. It was revealed that the creation of sulfur and tungsten vacancies and electron hopping between vacancies are the most possible mechanisms responsible for the enhanced RS performance. Memristor crossbar arrays based on h-BN have been demonstrated by Chen *et al.*[88] with high yield (98%), low device-to-device variability (5.74%), and low cycling tolerance variability (1.53%). The Ag/h-BN/Ag device exhibited a very high ON/OFF ratio of up to 10^{11} and an extremely low SET energy consumption of 8.8 zJ. Subsequently in 2021, with the help of electron-beam irradiation, a Ti/$PdSe_2$/Au memristor was demonstrated, which was able to show a long retention duration of up to 10^5 s.[89] The production of conductive filaments can occur in channels created by the grain boundaries produced by electron-beam irradiation, which enables the memristor to display the distinct quasi-reset RS characteristics. In 2022, Li *et al.*[90] demonstrated a memristor crossbar array utilizing polycrystalline $HfSe_2$ grown by molecular beam epitaxy on a 2-inch wafer, followed by a metal-assisted vdW transfer method. The memristor mimics synaptic weight plasticity while exhibiting a low switching energy (0.82 pJ) and tiny switching voltage (0.6 V). Recently, a high-integration-density 2D-CMOS hybrid microchip has been presented by Zhu *et al.*[91] for memristive applications. The authors have integrated multilayer h-BN onto the silicon microchips, which contain CMOS transistors (180 nm node), enabling endurances of $\sim 5 \times 10^6$ cycles in memristors with an active area of ~ 0.053 μm^2. All these works move 2D materials one step closer to being used to fabricate high-density artificial neural electronic circuits, which could accelerate their adoption in semiconductor manufacturing processes.

6. Conclusions and outlook

While substantial progress in the area of 2DLM-based artificial synapses has been made in recent years, certain critical issues still need to be addressed for the real-world applications of these emerging devices. Even now, the research on 2DLM-based memristors is in its budding phase, and thus there still remains a large scope for improving these devices.[12] Future improvement strategies have been categorized and discussed below:

6.1. Regarding growth techniques

• *Large area growth and device arrays*: present studies on the 2DLM-neuronal devices have mostly focused on single nanodevices, only on the proof-of-concept basis, consisting of layers of 2D materials typically in the range of a few microns.[92–97] Few reports have shown large scale growth of 2DLMs to fabricate scalable memristive device arrays,[98,99] which is very vital for their commercialization. Currently, most of the reported 2D memristors are fabricated utilizing exfoliation of these 2D materials from their bulk crystals,[93] followed by transfer on a substrate. Due to the absence of ultrahigh vacuum, the devices fabricated are often associated with unclean interfaces and thus reduced performance. Therefore, physical vapor deposition techniques such as pulsed laser deposition, molecular beam epitaxy, atomic layer deposition (ALD), *etc.* should be highly applicable to synthesize ultraclean and atomically thin 2DLM-based memristors.

• *Cost-effective growth methods*: various chemical vapor deposition-based synthesis methods have been successfully reported to fabricate large area 2DLMs; however, drawbacks like high growth temperatures, use of toxic precursors, long processing times, *etc.*[100,101] hinder the use of flexible substrates (mica, paper, polyethylene terephthalate, *etc.*) for memristor technology.[102] Alternative methods such as solution-based techniques (hydrothermal and solvothermal synthesis methods) should be exploited because of their low processing cost and temperature, along with high output.[103] However, due to the absence of vacuum during material transfer and device fabrication procedure, utmost care should be taken in order to ensure high device quality, performance, and reliability. Additionally, deposition techniques such as magnetron sputtering and ALD can be utilized for low temperature deposition of 2DLMs.[104]

6.2. Optimizing defect chemistry and stoichiometry

• *Defects*: as most of the RS mechanisms depend upon the defects present in the material, engineering and controlling the defect chemistry of a material become very essential for repeatable and reliable memristive devices.[18,105] Moreover, Janus structures of TMDCs, referring to transition metal layers having different surfaces, have garnered intensive research interest in recent times in view of their exceptional features that originate because of the symmetry breaking in such structures.[106] Hence, these could play a pivotal role in tailoring the memristive characteristics of neuromorphic devices.

• *Doping*: doping of 2DLMs is another key strategy that should be vastly explored for memristive devices, as it would help in precisely controlling the defect states in the material. Additionally, there is an urgent requirement to optimise the p-type doping of 2DLMs, which would facilitate their easy

integration with wide band gap n-type semiconductors such as TiO_2 or Ga_2O_3 for realization of p–n diode-based photomemristors.

6.3. Exploiting heterostructures of 2DLMs

• *Heterostructures*: an alternative approach to design optimum materials is to combine a set of materials with the required properties rather than looking for a single material that possesses all of them. More focus should be put on neuromorphic devices based on heterojunctions of 2DLMs. Utilization of high electron conducting 2D materials such as graphene, graphene derivatives and semi-metallic phases of TMDCs like 1T-MoS_2 in place of the traditional metal contacts over 2DLMs may offer new avenues, as these hybrids exhibit excellent electronic properties along with maximizing the area for light absorption, in the case of photomemristors.[17,50] Transition metal oxides (TMOs) such as TiO_2,[14] ZnO,[16,107] HfO_2,[108] *etc.* have been immensely utilized for neuromorphic devices, and thus the oxide technology seems to be somewhat matured in this area. Therefore, integration of 2DLMs with TMOs to form hybrid devices is expected to result in superior performance because these devices can utilize the advantages of both the established technology of TMOs and the unique properties of atomically ultrathin 2D materials.

• *Band alignment*: it is high time to explore heterostructures of 2DLMs with other 2DLMs or traditional semiconductors that show type-III band alignment, such as MoS_2/InN,[47] SnS_2/black phosphorus,[109] *etc.*, which can be reversibly transformed into type-II, in order to exploit RS based on the mechanism of Schottky barrier and direct tunneling.

• *Phase change materials*: PCMs exhibiting an exciting phenomenon at the atomic level have always been a topic of interest for many decades and, recently, they have shown a lot of potential in neuromorphic devices.[13] Their combination with 2DLMs could be very intriguing in achieving multiple conductance states by exploiting the properties of individual PCMs and the effects of the 2DLM/PCM heterojunction. Moreover, the mechanism of phase transitions in 2DLMs (for instance, the 2H phase to 1T phase in MoS_2) should be explored more and more, in order to design energy efficient memristors. These phase transitions, which can be triggered by an external electric field, are associated with a change in the crystal structure too. Repeated transitions in the structure result in mechanical wear and tear, thereby opening new avenues of research on decoupling the change in crystal structure with different conduction states.[13]

6.4. Stabilizing switching mechanisms

• *Suppressing surface oxidation*: although 2DLMs have more inert surfaces as compared to the those of non-layered materials, oxidation of exposed surfaces is still thermodynamically favorable for most of the 2DLMs. Consequently, research on the oxidation kinetics of 2DLMs can be an intriguing area of investigation as the unintentional oxide formation might affect the device behavior in both positive and negative ways.

• *Nanopatterning of substrates*: the majority of memristors operate *via* the growth and dispersion of conducting filaments, and the growth and distribution of these filaments are random.[77,110] This affects the reliability and repeatability of such devices, and thus, measures should be taken to minimize randomness in the filament growth. An effective way could be the nano-patterning of the surface using techniques like e-beam lithography or putting seeds on the surface before making the contact electrodes, to facilitate systematic growth of these conducting filaments.

• *Mechanisms other than conductive filaments*: utilizing resistive switching mechanisms such as changes in the crystal phase and modulation in Schottky barrier height will promote a uniform, reliable and stable switching phenomenon over a large number of endurance cycles.

6.5. Role of nano-structuring

• *One-dimensional structures*: memory devices based on one-dimensional nanostructures and their heterojunctions are another intriguing field that should be thoroughly explored.[107,111] Nanowires and nanorods exhibit several advantages such as charge carrier confinement, high surface to volume ratios, shorter channel lengths, *etc.*,[45] which boost their light harvesting properties. One-dimensional nanorods offer straighter conduction channels that assist in the transport of charge carriers compared to the branched conduction paths, observed in thin films. These direct channels produce outstanding memristive behavior as the resistance states show a narrow distribution in one-dimensional structures.[56]

• *Plasmonic and defect passivation*: noble metal nanoparticles (NPs) have been utilized in the past due to their fascinating properties such as localized surface plasmon resonance (LSPR),[112–114] defect passivation,[115] *etc.* Metal NPs such as Au and Pt can be exploited as charge trapping elements in NVS devices due to their large electron affinity, higher chemical stability, easy synthesis procedure, *etc.* Larger electron affinity extends the charge carrier lifetime, thereby enhancing the memristor's retention characteristics.[111] Phenomena like LSPR have been used to modulate photoexcitation of electrons in NP-based composite systems, and defect passivation can be used to tune the defect states in memory devices.

6.6. Theoretical approaches and algorithms, and their integration into existing device assemblies

• *Modelling*: while the current research on memristors is driven by experiments, computational simulations and modelling using density functional theory (DFT) and molecular dynamics (MD) offer powerful tools to predict charge transfer, electronic band structures, carrier dynamics, *etc.*,[116,117] all of which can be critical for determining the memristor performance. Additionally, simulations also govern stability, defect behavior, and diffusion, expediting material design for better properties. Unraveling intricate atomic-level investigations can accelerate the advancements in high-performance memristors and neuromorphic devices.

• *Algorithms*: current neuromorphic technology may perform exceptionally well in some specialized tasks (such as pattern recognition and sensory processing), but may fall short in more general cognitive activities. It is still difficult to create

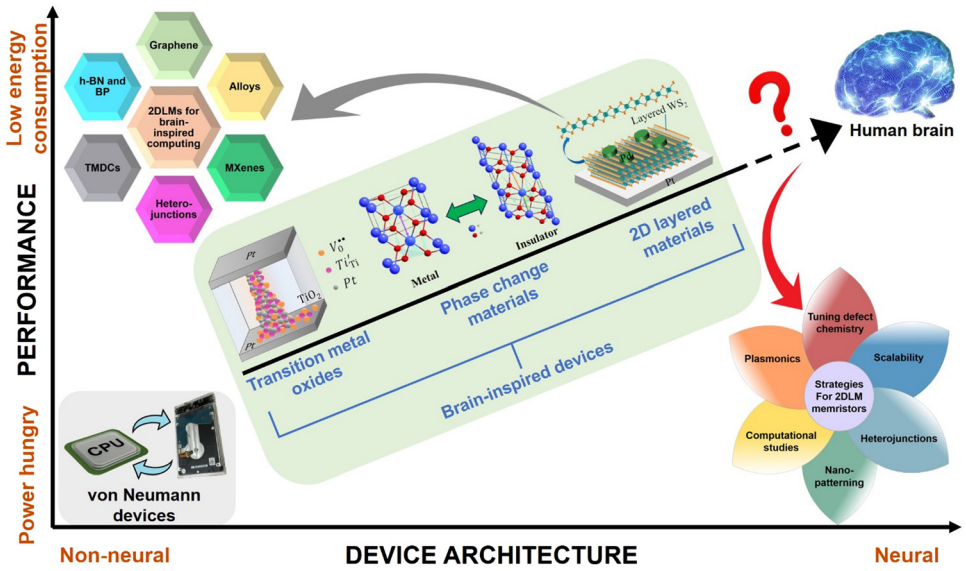

Fig. 6 2DLMs for neuromorphic computing. Performance scales up with the advancement of the design architecture, ranging from von Neumann devices to neuromorphic systems. The ultimate target is to design devices mimicking brain's activity and matching its efficiency. Recent progress in memristors fabricated utilizing TMOs, PCMs, and 2DLMs, and with certain strategic modifications in different 2DLMs, devices emulating intelligence and critical for non-von Neumann machines can be designed. Reproduced with permission from ref. 87, 119 and 120. Copyright 2019, John Wiley & Sons, Inc.; copyright 2023, Springer Nature; copyright 2020, Frontiers.

neuromorphic machines that can perform a variety of cognitive activities. Additionally, the neuromorphic devices try to mimic biological learning and adaptability; however, it is still difficult to develop effective and reliable learning algorithms that can be implemented on hardware. Although there have been convincing examples where neuromorphic solutions outperform other hardware implementations like neural hardware and edge GPUs in terms of energy efficiency, there has not yet been a machine learning algorithm/application combination for which neuromorphic computing significantly outperforms deep learning approaches in terms of accuracy.[118] The absence of widely available and usable hardware and software systems for the computer science communities is another major obstacle impeding the development of algorithms and applications for neuromorphic computers. There exist multiple neuromorphic implementations; yet, the quantity of each implementation is constrained, and the broader community can usually obtain them only through restricted cloud access.[118]

- *Issues with integration*: last but not least, neuromorphic devices may face competition from more established computing technologies, such as traditional CPUs, GPUs, and AI accelerators. Moreover, the current devices may not be fit to accommodate the neuromorphic chips and parallel computing, and thus, new device assemblies need to be built for the successful integration of these neuromorphic devices. It is probable that a multitude of applications for neuromorphic computers in the future will involve their integration into a more diverse computing environment, as opposed to their standalone usage. Emergent hardware systems, including neuromorphic and quantum computers, will be included in the computing landscape more frequently to speed up specific types of computation due to performance limitations (in terms of energy consumption or processing speed) of current hardware systems.[118] Additionally, neuromorphic technology may need to be shown to have definite advantages and value in order to persuade corporations and sectors to invest in and use it.

It is important to note that research and development in the field of neuromorphic computing are ongoing, and recent advancements in neuromorphic devices have shown promising strides towards bridging the gap between biological and AI neural networks. A summary of the progress and future perspectives on 2DLM-based devices for AI is pictorially depicted in Fig. 6. Continuous research and innovation are essential to unlock the full potential of neuromorphic devices and pave the way for a new era of efficient and brain-inspired computing paradigms.

Conflicts of interest

The authors have no conflicts to disclose.

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