Nanoscale Horizons

ROYAL SOCIETY OF CHEMISTRY

COMMUNICATION

View Article Online
View Journal | View Issue

Cite this: *Nanoscale Horiz.*, 2024, **9**, 1990

Received 12th July 2024,
Accepted 13th August 2024

DOI: 10.1039/d4nh00339j

rsc.li/nanoscale-horizons

Processes to enable hysteresis-free operation of ultrathin ALD Te p-channel field-effect transistors†

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Recently, tellurium (Te) has been proposed as a promising p-type material; however, even the state-of-the-art results couldn't overcome the critical roadblocks for its practical applications, such as large *I–V* hysteresis and high off-state leakage current. We developed a novel Te atomic layer deposition (ALD) process combined with a TeO_x seed layer and Al_2O_3 passivation to detour the limitations of p-type Te semiconducting materials. Also, we have identified the origins of high hysteresis and off current using the 77 K operation study and passivation process optimization. As a result, a p-type Te field-effect transistor exhibits less than 23 mV hysteresis and a high field-effect mobility of 33 $cm^2\ V^{-1}\ s^{-1}$ after proper channel thickness modulation and passivation. Also, an ultralow off-current of approximately 1×10^{-14} A, high on/off ratios in the order of 10^8, and a steep slope subthreshold swing of 79 mV dec^{-1} could be achieved at 77 K. These enhancements strongly indicate that the previously reported high off-state current was originated from interfacial defects formed at the metal–Te contact interface. Although further studies concerning this interface are still necessary, the findings herein demonstrate that the major obstacles hindering the use of Te for ultrathin p-channel device applications can be eliminated by proper process optimization.

New concepts

Developing an atomic layer deposition (ALD) technique of 2D tellurium (Te) is rarely reported because of the fundamentally low reactivity of the precursors. Therefore, reducing the thickness of ALD Te films has been difficult, making the formation of electrically suitable ultrathin Te very challenging. We report a novel Te ALD process combined with a TeO_x seed layer and Al_2O_3 passivation to detour the limitations of p-type Te semiconducting materials. Generally, ALD Te shows a two-step growth stage during deposition, which is faster at the initial stage and slower at the later stage. The TeO_x seed layer aids in forming a stable ultrathin film. As a result, a p-type Te field-effect transistor exhibits less than 23 mV hysteresis and a high field-effect mobility of 33 $cm^2\ V^{-1}\ s^{-1}$ after proper channel thickness modulation and passivation. Additionally, systematical temperature dependent analysis was carried out using high quality Te, which strongly indicates that the previously reported high off-state current originated from interfacial defects formed at the metal–Te contact interface. These results provide new insights into forming 2D Te using ALD and demonstrate that the major obstacles hindering the use of Te for ultrathin p-channel device applications can be eliminated by proper process optimization.

1. Introduction

Heterogeneous integration (HI) of multiple chips or monolithic 3D (M3D) integration of more functional circuit blocks in the back-end of line (BEOL) structure has become inevitable to overcome the physical scaling limit of silicon complementary metal–oxide–semiconductor (CMOS) technology.[1–4] With regard to both HI and M3D integration, novel technologies that can enable smart and efficient connections of chips or functional circuit blocks are necessary. Thus, various bridging technologies such as Intel's FOVEROS and embedded multi-die interconnect bridge (EMIB), inter-chip communication technologies such as peripheral component interconnect express (PCIe) and compute express link (CXL), and load distribution technologies, such as a processor in memory and logic in memory, are being actively developed.[5–11]

The natural evolution of these technologies requires smarter interconnections, including reconfigurable interconnect and logic functions in BEOL or bridges. Various materials, such as transition metal dichalcogenides (TMDCs), oxide semiconductors, and graphene, have been studied for the low-temperature integration of logic devices that can be incorporated into

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† Electronic supplementary information (ESI) available. See DOI: https://doi.org/10.1039/d4nh00339j

heterogeneous or multilayer chip systems. For these applications, new channel materials must be deposited and processed at low fabrication temperatures to minimize their influence on existing chips or devices.[12] So far, various n-type semiconductors, including indium gallium zinc oxide (IGZO), zinc oxide (ZnO), and molybdenum disulfide (MoS_2), have been proposed as new channel materials with reasonably satisfactory performances.[13–19] However, their counterpart p-type semiconductors with comparable performances are still a missing link and make complementary circuit design difficult. Thus, high-performance p-type inorganic semiconductors, which can be deposited on arbitrarily shaped three-dimensional surfaces, became one of the most wanted materials for future electronics.

Tellurium (Te), a material that belongs to the chalcogenide family, exhibits a high hole mobility owing to the hole pockets located near its valence band maxima.[20] Additionally, Te films comprising multiple one-dimensional (1D) Te helical chains, composed of covalently bonded Te atoms, have been constructed utilizing van der Waals interactions.[21] In the bulk state, Te is a narrow-bandgap material (0.35 eV). Te has been studied for thermoelectric applications owing to its high electrical conductivity and low thermal conductivity, as well as for photoelectric applications, piezoelectric effect and current-induced spin polarization.[22–28] Additionally, Te is being studied for various applications as a two-dimensional (2D) material across different fields.[29,30]

Recently, Te has been investigated for field-effect transistor (FET) applications owing to its high mobility and air stability, despite its narrow-bandgap, which can induce a high off-current.[25,31–33] An initial study was reported using 2D Te flakes obtained using exfoliation or solution synthesis.[32,34,35] Various large-scale Te processes have been explored, especially targeting to obtain sub-10 nm Te because the bandgap of Te increases at sub-10 nm thickness. However, for thinner Te, large hysteresis, which is caused by an increased portion of trap at thinner film sizes, has become a major showstopper for device applications.[36–41] Various studies have been conducted to reduce defects in Te channels using atomic layer deposition (ALD) and surface treatments. However, thickness reduction of ALD Te films has been difficult owing to the low reactivity of the precursors, so the formation of electrically suitable ultrathin Te remains very challenging.[42]

In this study, we successfully demonstrated the deposition of Te pFETs with ultrathin ALD Te (4.7 nm) on a 4-inch wafer at low temperatures (<200 °C), resulting in a high-performance Te channel layer with minimal hysteresis. The lowest hysteresis value $\sim$23 mV reported so far, a high on/off ratio (10^8), an excellent subthreshold swing of 79 mV dec^{-1}, and an ultralow off-current (10^{-14} A) at 77 K were obtained. Furthermore, we identified that the high off-current observed in previous studies is primarily due to the interfacial defects formed at the metal–Te contact region. Our findings pave the way for the development of high-performance Te pFETs, which can be a breakthrough for various complementary circuit applications in heterogeneously integrated systems.

2. Experimental

2.1 Thin film fabrication

A Te target (99.999%, iTASCO) was used to deposit the TeO_x seed layers using reactive magnetron sputtering at room temperature. The base pressure was maintained at approximately 3×10^{-6} torr. Ar (30 sccm) and O (30 sccm) gas mixtures were used, maintaining a working pressure of 2 mTorr. The DC power was fixed at 20 W for 10 s to deposit 2 nm thick TeO_x. For the ALD Te deposition on the TeO_x seed layer at 80 °C, two liquid-phase precursors, namely, BTMS-Te (Thermo Fisher Scientific) and Te ethoxide (Thermo Fisher Scientific), were used. Te ethoxide was heated at 80 °C, and Ar (50 sccm) gas was employed for the purging step. Each ALD cycle comprised 4 s BTMS-Te exposure, 10 s hold time, and 20 s Ar purge followed by 60 s Te ethoxide exposure, 10 s hold time, and 40 s Ar purge.

2.2 Thin film characterization

An Oxford Instruments Jupiter XR AFM was used for the surface morphology and thickness measurements. For the KPFM measurements on the Ni and Te surfaces, the same AFM was used with a Ti/Ir (5/20 nm)-coated tip (ASYELEC-01-R2, Asylum Research). FE-SEM (JSM-7800F Prime, JEOL) was used to monitor the quality of the Te surface at the microscopic level at an accelerating voltage of 5 kV. HR-TEM images and FFT patterns were acquired using a JEOL JEM-2200FS TEM microscope that operates at 200 kV. A Thermo Scientific Nexsa G2 XPS with an Al Kα beam, exhibiting a 400 μm spot size and 50 eV pass energy, was used to record the XPS spectra. Depth profiling with an Ar ion beam was conducted for up to 320 s. Survey scans and narrow scans of the O 1s, Te $3d_{5/2}$, and Te $3d_{3/2}$ peaks were performed and fitted with the relevant peaks. A UV-visible (vis) spectrometer (V-670, SEMES/JASCO) was used to measure the transmittance and absorbance of the Te films at a scan speed of 200 nm min^{-1}. The optical bandgaps were extracted from the absorbance spectra using a Tauc plot.

2.3 Te FET fabrication

First, 300 nm $SiO_2/p^{++}Si$ substrates (100 mm in diameter) were sequentially cleaned using acetone, methanol, and distilled water for 5 min with sonication. Subsequently, the SiO_2 layer was patterned and dry-etched using an ion-coupled plasma reactive-ion-etch (ICP-RIE) process with Ar and CF_4 gases to form a 70 nm SiO_2 trench. Subsequently, Ti/Al (10/60 nm) was electron beam-evaporated into the trench region to fabricate the buried-gate formation, and this was followed by chemical–mechanical polishing to flatten the surface. Thereafter, 12 nm Al_2O_3 gate dielectric was deposited using ALD at 200 °C. For the channel formation, a TeO_x seed layer was sputtered and Te was deposited using ALD. The channel regions were patterned using ICP-RIE with an Ar and CF_4 gas mixture. Following photoresist stripping, source/drain metal (Ni, 50 nm) electrodes were formed using a liftoff process. For passivation, 10 nm Al_2O_3 was deposited at 150 °C. Finally, for the measurements, the contact pad opening was performed *via* the wet etching of Al_2O_3 on the gate, source, and drain electrodes using

ammonium hydroxide. All patterning processes were performed using contact photolithography, and the channel width (W) and length (L) were 10 and 5 μm, respectively.

2.4 Te FET characterization

A semiconductor parameter analyzer (Keithley 4200A) was used to analyze the I–V characteristics of the Te pFETs. Low-temperature measurements were performed in a liquid nitrogen-cooled chamber with a temperature controller (MSTECH, MST-1000H). The field-effect mobility is estimated to be $\mu_{FE} = g_m L/WC_{OX}V_d$, where g_m denotes the transconductance, L denotes the channel length, W denotes the channel width, C_{OX} denotes the gate-oxide capacitance, and V_d is the drain voltage. The subthreshold swing was calculated as SS = $dV_g/d\log(I_d)$, and the threshold voltage was extracted using the linear extrapolation method. I–V hysteresis was calculated using the threshold voltage difference between forward and backward sweep, and the interface trap density was calculated as $D_{it} = \frac{C_{OX}}{q}\left[\frac{qSS\ln 10}{kT} - 1\right]$, where q denotes the electron charge and k denotes the Boltzmann constant.[43]

3. Results and discussion

A schematic of the Te formation process is illustrated in Fig. 1(a). The quality of the Te ALD process is strongly influenced by the surface conditions because of the low reactivity of the Te precursors, namely bis(trimethylsilyl) telluride (BTMS-Te) and Te ethoxide; this impedes the initial nucleation site formation on non-treated surfaces.[42] We utilized a 2 nm sputter-deposited TeO_x seed layer to facilitate the deposition of a few layers of Te. The TeO_x seed layer was patterned using a liftoff process, and then the ALD Te process was performed at 80 °C using two liquid-phase precursors—BTMS-Te and Te ethoxide. The anticipated chemical reaction of ALD Te is as follows:

$$2Te(SiMe_3)_2 + Te(OEt)_4 \rightarrow 3Te + 4Me_3Si\text{-}OEt \quad (1)$$

During the ALD process, a 10 s hold time was incorporated after each precursor cycle to provide sufficient reaction time for the low-adhesion precursors, particularly Te ethoxide, which has a low vapor pressure. Thus, our ALD process comprised a BTMS-Te dose–hold–purge and a Te ethoxide dose–hold–purge for each cycle. Finally, after the ALD process, 10 nm Al_2O_3 was deposited as a passivation and oxygen scavenging layer.

In the region having the TeO_x seed layer, the presence of sufficient nucleation sites facilitated the surface reactions between BTMS-Te and TeO_x. Once BTMS-Te was adsorbed on the seed layer, Te ethoxide reacted with the surface reactants, resulting in the formation of Te films. In contrast, no noticeable Te deposition was observed in the bare silicon region because of the poor adsorption of BTMS-Te on the silicon surface, matching with the observations shown in Fig. 1(b) (and Fig. S1 of the ESI†). The stable and reproducible selective deposition of Te indicates that the presence of the TeO_x seed layer is a critical factor in providing sufficient nucleation sites for the initial growth stages, enabling the selective deposition process.

To emphasize the selective deposition characteristics, ALD of Te was performed on a glass substrate to visually demonstrate selective deposition. First, a TeO_x seed layer was deposited and patterned. Subsequently, ALD of Te was performed. As the number of deposition cycles increased, the color contrast became increasingly evident, as shown in Fig. 1(c).

The thickness and surface roughness of Te layers shown in Fig. 1(b) were analyzed using atomic force microscopy (AFM) (Fig. 1(d) and Fig. S2 of the ESI†). The thickness of the TeO_x seed layer is 2 nm, and the total thickness of the Te layer including the seed layer linearly increases from 4.7 nm to 9.8 nm after 20 and 160 cycles of ALD. The average growth per cycle (GPC) is ~0.48 Å, which is similar to the value reported in the previous work.[42] The root-mean-square (RMS) roughness values measured *via* AFM increase from 0.47 nm at 20 cycles to 1.43 nm at 160 cycles.

X-ray photoelectron spectroscopy (XPS) analyses were performed at various stages of the Te deposition (after TeO_x, Te/TeO_x, and the Al_2O_3 passivation layer/Te/TeO_x) to investigate the oxidation state of Te using the Te^{4+} state (Fig. 1(e) and Fig. S3 of the ESI†). The TeO_x seed layer exhibited the highest Te^{4+} content, with a Te : O ratio of 1 : 1.48. The Te deposited on the seed layer exhibited a reduction in the oxidized Te portion, that is, a lower Te^{4+} ratio. Highly intrinsic Te was observed after passivation. The reduction of Te^{4+} states after passivation indicates that oxygen from the Te layer was absorbed into the Al_2O_3 layer during the ALD process at 150 °C. The oxygen scavenging effect of the ALD process is well-known; however, this process was particularly effective to the ALD deposited Te owing to its fundamental nanometer level controllability.[37,38,44] The depth profile of the atomic components of the Al_2O_3 passivation layer/Te/TeO_x stack showed the presence of a Te layer in the middle of the film stack with a very low oxygen concentration, confirming the XPS analysis results (Fig. S4 of the ESI†).

Single-crystal Te comprises helical Te chains bonded by van der Waals forces in a hexagonal lattice, as shown in Fig. 2(a). Cross-sectional high-resolution transmission electron microscopy (HR-TEM) was used to investigate the crystalline structure of the Al_2O_3 passivated Te film at the atomic level (Fig. 2(b)). As illustrated in Fig. 2(c), the presence of hexagonal Te was verified within the Te crystal domain, which is characterized by a lattice spacing of approximately 3.26 Å. The corresponding fast Fourier transform (FFT) pattern also confirms the highly crystalline structure with a bright sharp diffraction pattern in the yellow circle.

Fig. 3(a) and (b) shows the schematic structure and the top-down SEM image of the Te pFET. Further details of the device fabrication processes are provided in the Methods section and Fig. S5 of the ESI.† The buried-gate structure is used to minimize the influence of source/drain underlapping. The thickness of the Al_2O_3 gate dielectric deposited on the buried-gate electrode is 12 nm (equivalent oxide thickness (EOT) = 5.2 nm). The Te channel thicknesses varied from 4.7 nm to 9.8 nm. To emphasize the large-scale process integration capability, devices fabricated on a 4-inch Si wafer are shown in

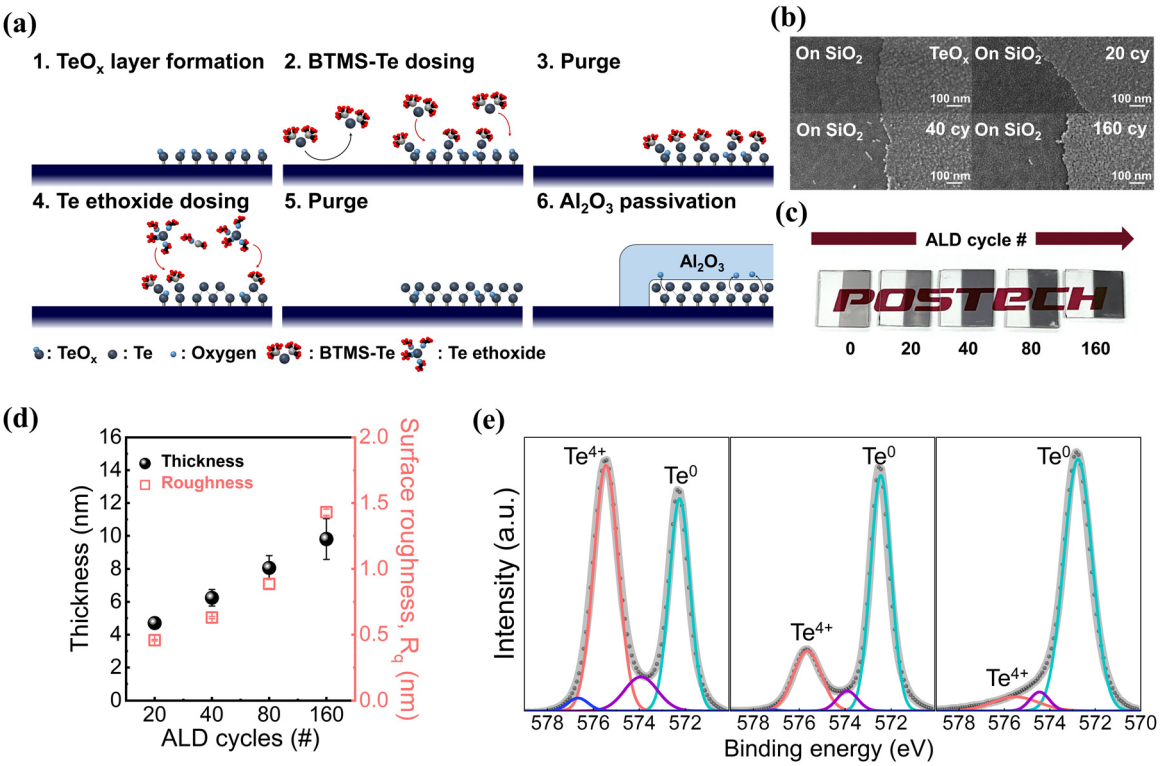

Fig. 1 Defect deficient Te thin film formation *via* ALD. (a) Schematic process sequence of the ALD process on the seed layer, followed by Al_2O_3 passivation. (b) Top-down SEM images of Te deposited on TeO_x-patterned samples from 0 cycles to 160 cycles. In each of the four sections, the left side of the SEM image displays deposition results on bare SiO_2, while the right side shows the results on the region having the seed layer. (c) Photographs displaying the color change at the TeO_x regions as the cycle of Te deposition increases. (d) Thickness and surface roughness (RMS) of Te including the seed layer, measured by AFM, after 0 to 160 cycles of ALD. (e) XPS spectra of Te $3d_{5/2}$, including the TeO_x layer, the Te layer on TeO_x, and the Al_2O_3 passivated Te layer from left to right.

Fig. 3(c). For the statistical analysis, at least 25 devices are measured for each thickness group. Typical Te pFETs show a huge hysteresis as shown in Fig. 3(d), ranging from 1 V at 160 cycles to 2.81 V at 20 cycles. Since hysteresis hinders proper circuit operation, it is crucial to minimize the hysteresis for practical applications. However, previously reported Te pFETs still showed a significant amount of hysteresis even after passivation. In our work, we were able to achieve near hysteresis-free transfer characteristics for a 4.7 nm Te channel case, as shown in Fig. 3(e). After the passivation, due to the oxygen scavenging effect by the TMA precursor during the Al_2O_3 passivation process, the hysteresis values of 4.7 nm Te devices substantially decreased by 128 times, from 3000 ± 53 mV to 23 ± 1.1 mV. The Te thickness dependence of hysteresis reduction indicates that the hysteresis is indeed related to oxygen-induced defects, which were more effectively eliminated at the thickness below a certain diffusion limit (Fig. 3(f) and Fig. S6 of the ESI†). For the devices showing the near

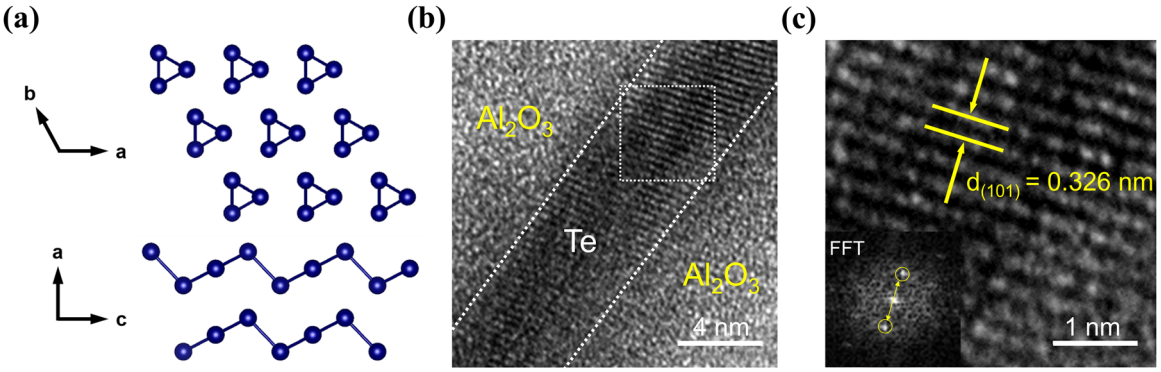

Fig. 2 Crystal structure analysis of Te at the atomic level. (a) Structure of hexagonal Te. (b) Cross-sectional HR-TEM image of the Al_2O_3 passivation layer/4.7 nm Te/TeO_x/Al_2O_3 gate dielectric stack. (c) Enlarged image of the white box in (b), highlighting the hexagonal Te structure with a *d*-spacing of 0.326 nm at the (101) plane; the inset image shows the FFT pattern and the yellow circled pattern indicates the (101) plane.[35]

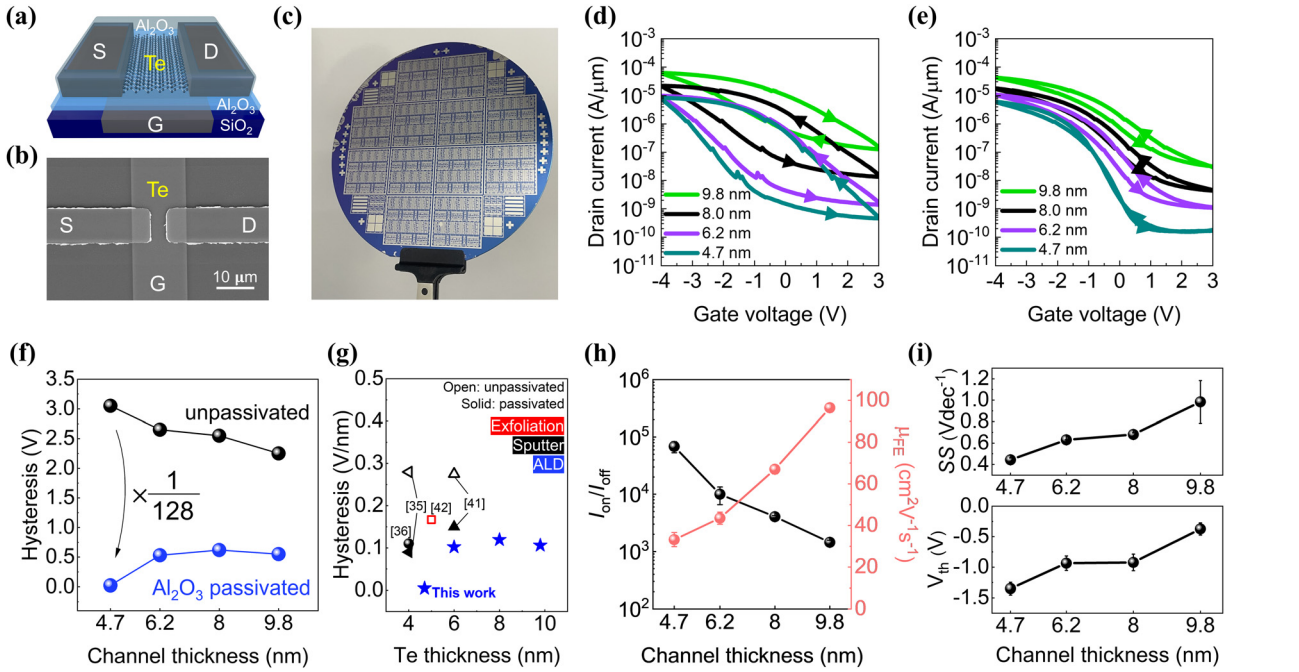

Fig. 3 Electrical characteristics of Te pFETs investigated as a function of the Te channel thickness. (a) Schematic structure of the buried-gated Te pFET. (b) Top-view SEM image of the Te pFET with a channel length of 5 μm and a width of 10 μm. (c) Optical image of Te pFETs on 4-inch Si wafer. (d) Transfer curves of unpassivated Te pFET with different Te channel thicknesses from 4.7 nm to 9.8 nm, measured at a drain voltage of −1 V. (e) The transfer curves of the Te pFETs, measured after Al_2O_3 passivation, exhibit a significant decrease in the hysteresis. (f) Extracted hysteresis of unpassivated (black spheres) and passivated (blue spheres) Te pFETs. (g) Normalized hysteresis *vs.* Te channel thickness of the present study together with previous works. (h) On/off ratio (black spheres) and field-effect mobility (red spheres) of Al_2O_3 passivated Te pFETs, shown as a function of the Te channel thickness. (i) Subthreshold swing and V_{th} shown as a function of the Te channel thickness.

hysteresis-free operation, the interface defect density was reduced to 2.56×10^{12} cm^{-2} from 8.08×10^{12} cm^{-2}, after the passivation for the 4.7 nm Te case. Fig. 3(g) compares the relative differences between the hysteresis of our device and that of previously reported Te pFETs. The hysteresis values of prior works shown in Fig. 3(g) were estimated from the published data, normalized by the EOT. This comparison clearly shows that the hysteresis could be drastically reduced by using the ALD process with the passivation, which could be more effective for thinner Te cases.

As the Te film thickness decreased, the optical bandgap, which is extracted from the absorption spectra, increased as expected, and the off-current decreased owing to the increase in the Schottky barrier height (SBH) at the source/drain contact (Fig. S7 of the ESI†). Due to the increment in the bandgap for thinner Te channels, the on/off ratio increased rapidly from 1.5×10^3 to 6.8×10^4. Thus, the device operation becomes increasingly stable with thinner Te channels. The hole mobility rapidly decreased from 96 ± 2.1 cm^2 V^{-1} s^{-1} at 9.8 nm to 33.2 ± 1.4 cm^2 V^{-1} s^{-1} at 4.7 nm (Fig. 3(h)). The lower hole mobility with a larger bandgap is an intuitively correct trend. Thus, the higher mobility values reported in the literature may be related to greater Te channel thicknesses.[36,39,42] The hole mobility of 33.2 ± 1.4 cm^2 V^{-1} s^{-1} for 4.7 nm Te is still a considerably high value compared with those of other p-type semiconductor materials of comparable thickness. The subthreshold swing also improved to 0.44 V dec^{-1} for a 4.7 nm Te channel from 0.98 V dec^{-1} for a 9.8 nm Te channel, whereas the threshold voltage (V_{th}) increased to −1.35 V from −0.37 V (Fig. 3(i)). Even though the substantial hysteresis reduction for the 4.7 nm Te pFET is an important process for practical device applications, the threshold voltage over −1 V is still a technical concern; therefore, further study is necessary to determine the appropriate method to modulate the V_{th} value to ensure the compatibility of the Te pFET with silicon CMOS technology. The electrical characteristics of the Te pFETs were analyzed in detail over a range of operating temperatures from 77 to 300 K to further investigate the origin of high off-current, high V_{th}, and hysteresis (Fig. 4(a)). Al_2O_3 passivated devices with a 4.7 nm Te channel are used for this study. As the temperature decreased, both on current and off current decreased gradually, but the off-current decreased much more abruptly. As a result, the on/off ratio was improved from 6.8×10^4 at 300 K to 2.7×10^8 at 77 K. At 100 K, the off-state current decreased below the sub-picoampere level, indicating that the device characteristics, particularly the subthreshold region observed at temperatures above 150 K, are primarily dominated by the high-temperature-activated diffusion current. Fig. 4(b) shows that the field-effect mobility decreased to 13.2 cm^2 V^{-1} s^{-1} at 77 K owing to lower carrier injection, which is induced by high SBH at low temperatures. These are the typical behaviors of metal–oxide–semiconductor field-effect transistors (MOSFETs) having direct metal–semiconductor contacts, that is, the Schottky barrier FETs (SBFETs).[45,46] When the thickness of Te decreases to a

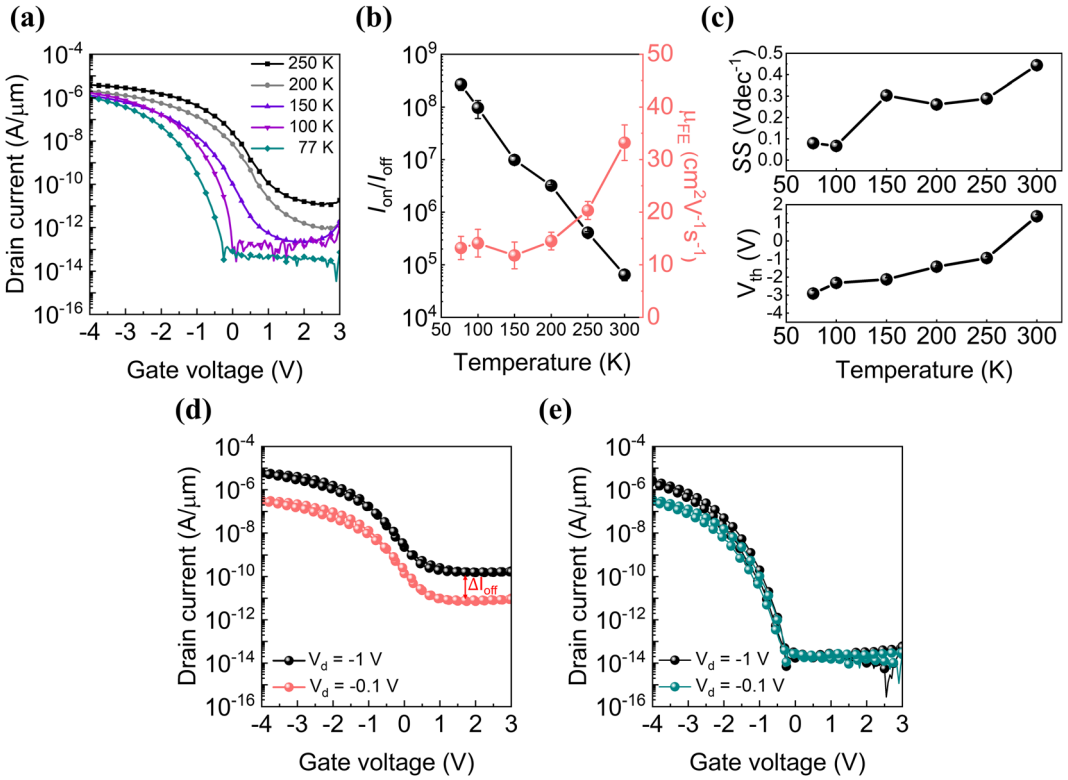

Fig. 4 Temperature-dependent electrical characteristics of Te pFETs. (a) Transfer curves of 4.7 nm Te pFET measured over the range of 77 K to 250 K. (b) Temperature dependence of the on/off ratio (black spheres) and field-effect mobility (red spheres). (c) Subthreshold swing and threshold voltage. Drain voltage dependence of transfer curves measured at (d) 300 K and (e) 77 K.

few nanometers, the metal–Te contacts become a larger portion of current conduction, resulting in the formation of SBFETs. In the case of SBFETs, the mobility values extracted for low temperature cases have a strong series resistance component due to the thermally activated defects. Thus, the actual mobility value of Te FETs would be higher than the values shown in Fig. 4(b).

The subthreshold swing of Te pFETs was reduced to 79 mV dec^{-1} at 77 K from 440 mV dec^{-1} at 300 K (Fig. 4(c)). The significant swing reduction as a function of temperature confirms that additional current components activated at higher temperatures dominate the subthreshold region. We assume that the defects mediating the higher off current are present near the Schottky barrier region because the injection current *via* these defects can be strongly influenced by the temperature. Interestingly, both the on-current and the off-current were strongly modulated by the drain bias at high temperatures, as shown in Fig. 4(d). This is significantly different from the typical characteristics of a silicon long channel MOSFET where the only on-current is modulated by the drain bias. Again, these abnormal behaviors can be explained if the Te pFET is an SBFET where the effective Schottky barrier height is modulated by the drain bias. Then, the strong V_d dependence of the on- and off-currents can be attributed to the field-induced current injection *via* the defect sites near the metal–Te contact. As expected from our assumption, because these defect sites can be deactivated at low temperatures, the influence of drain bias on the off-current decreased in the low temperature cases (Fig. 4(e)).

Based on the device operation scheme discussed above, we analyzed the transport characteristics of the Te pFET using the SBFET model.[43] The SBH between Ni and Te was determined using the reverse-bias thermionic emission equation[47] as follows:

$$I_d = AA^* T^{1.5} e^{-\frac{q\phi_B}{kT}} \left(1 - e^{-\frac{qV_d}{kT}}\right), \quad (2)$$

where I_d denotes the drain current, A denotes the contact area, A^* is the Richardson constant, q denotes the magnitude of the electron charge, T denotes the temperature, ϕ_B represents the effective SBH, k is the Boltzmann constant, and V_d denotes the drain voltage. Thus, using the subthreshold leakage current in the region that corresponds to the gate voltage $V_g = -2.5$ to 1 V, the Arrhenius plot of $\ln(I_d/T^{1.5})$ *versus* $1000/T$ is plotted in Fig. 5(a). The activation energy (E_A) was extracted from the slope of this plot. As V_g is varied from positive to negative values, E_A varies linearly until V_g reaches the flat-band voltage. After the flat-band voltage, E_A exhibits nonlinear behavior, and the corresponding E_A value at this point is equal to the effective SBH. For the $V_d = -0.1$ V case, the extracted effective SBH is 79.2 meV with −0.15 V of the flat-band voltage (Fig. 5(b)). Using the SBHs extracted at different V_d values, an SBH value of approximately 84.2 meV at zero bias can be obtained, as shown in Fig. 5(c). Using the surface potential value measured with Kelvin probe force microscopy (KPFM) and the work function of Ni measured with ultraviolet photoelectron

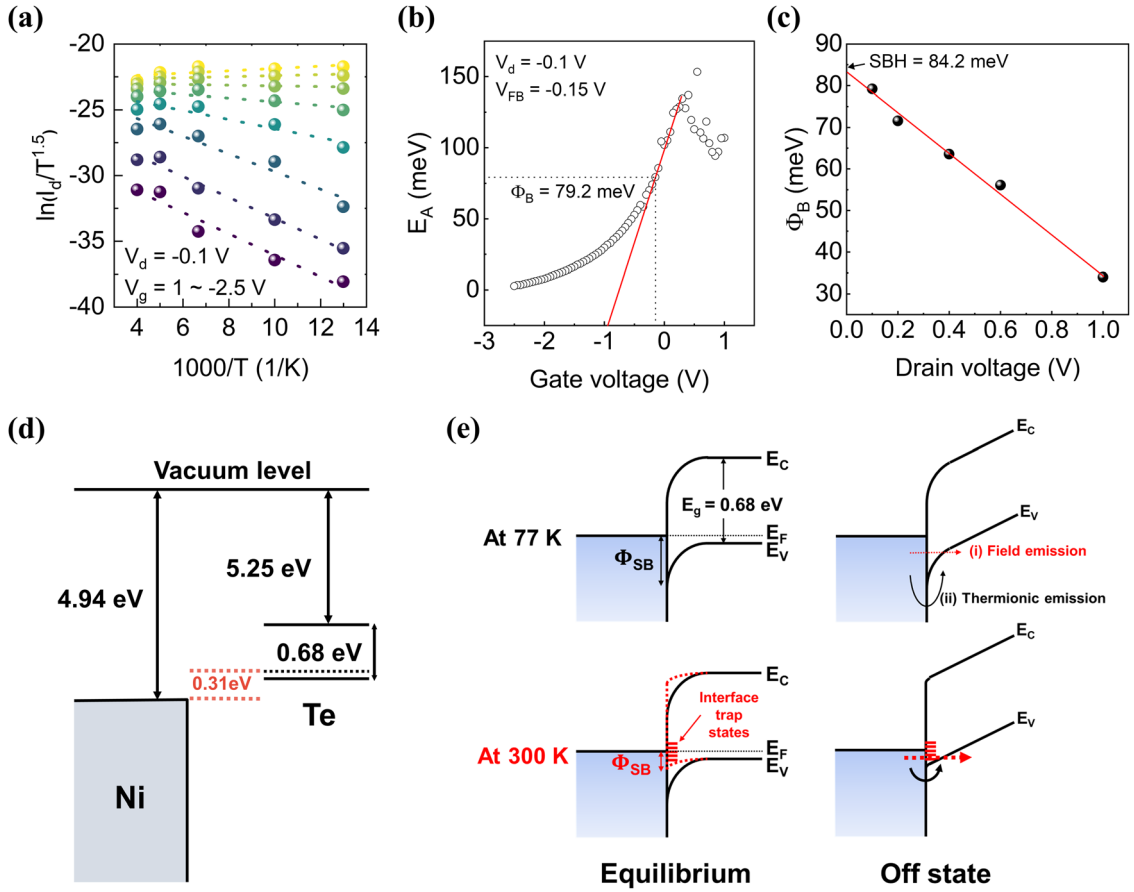

Fig. 5 Transport mechanism investigation through effective Schottky barrier analysis. (a) Arrhenius plot measured at a drain voltage of −0.1 V and a gate voltage in the subthreshold region from −2.5 V to 1 V. (b) Gate bias-dependent activation energy extracted from the slopes of the curves shown in (a). An effective SBH of 79.2 meV was extracted at a flat-band voltage of −0.15 V. (c) SBH extracted as a function of the drain voltages. Linear extrapolation results in a zero-drain bias SBH of approximately 84.2 meV. (d) Theoretical band alignment of Te and Ni without contact. (e) Energy band diagrams that show the role of defects at the Schottky contact. The three cases show the differences of SBH at different temperatures and biases.

spectroscopy (UPS), an ideal band diagram can be constructed (Fig. 5(d) and Fig. S8 and S9, ESI†). The ideal SBH of 310 meV is much higher than the experimentally extracted value of ~84.2 meV. This discrepancy can be explained by assuming the presence of interfacial defects, which reduce the effective SBH, as illustrated by the energy band diagrams (Fig. 5(e)). Without gate and drain bias, the band alignment should be in an equilibrium state with the SBH close to the ideal value. However, due to the intervention of thermally activated defect states, effective SBH is lowered to 82 meV at 300 K. When a drain bias is applied, the low effective SBH at the metal/Te junction becomes a source of the strong off state leakage current. On the other hand, at 77 K, the effective SBH is restored because most of the oxygen induced defects residing in the metal/Te interface region are deactivated and the off state current decreases to a level of 10 fA. At this point, there is no direct evidence relating the thermally activated interface trap states with oxygen-induced defects in the Te channel region. Yet, it is reasonable to assume that the Te region under the metal contact is less likely influenced by the passivation process because the passivation was only effective for the 4.7 nm Te channel. Thus, the oxygen induced defects under the metal contact most likely originated from thermally activated defects causing the bias dependent off-current at room temperature.

4. Conclusions

We successfully demonstrated the hysteresis-free intrinsic operation of a Te pFET by realizing ultrathin atomic layer deposition of Te (4.7 nm). The entire fabrication process was performed at low temperatures (<200 °C), opening possible applications for HI and monolithic 3D integration with large-scale scalability. We identified oxygen as the primary source of instability in Te devices and achieved an extremely low hysteresis of 23 mV with 4.7 nm Te. Our results indicate that the high off-current, high mobility, and high on-current values reported in previous studies can be attributed to the defect-induced field injection current at the Schottky contact of Te FETs. Near-intrinsic device operation of properly passivated Te pFETs, such as an ultralow off-current of approximately 1×10^{-14} A at 2 V, a high on/off ratio of approximately 3×10^{8}, and a subthreshold swing of 79 mV dec^{-1} at 77 K, indicates that the ideal device

characteristics of Te pFETs are competitive. For further study, we suggest that the oxygen induced defects in the Te–metal contact should be minimized to realize the ideal device operation at room temperature.

Author contributions

M. K. and B. H. L. conceived the idea and designed the experiments. G.-H. P., M. M. S., and B. H. L. supported the resources. M. K. executed the experiments and performed material characterization studies and electrical characteristic measurements. M. K. and B. H. L. co-wrote the manuscript, and all authors were involved in the discussions.

Data availability

The data supporting this article have been included as part of the ESI.† The authors will supply the relevant data in response to reasonable requests.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

This research was supported by the Nanomaterials Development Program (2022M3H4A1A04096496) and the Innovative Research Center Program (no. RS-2023-00260527) through the National Research Foundation of Korea (NRF), funded by the Ministry of Science and ICT (MSIT), Korea.

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