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Enhanced bending stability of flexible perovskite solar cells on stainless steel substrates via C₆₀ buffer layer integration†

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Flexible perovskite solar cells (PSCs) based on stainless steel (SS) substrates offer a highly promising platform for next-generation Building-Integrated Photovoltaics (BIPV) and Vehicle-Integrated Photovoltaics (VIPV), owing to their superior durability, mechanical strength, and thermal resilience. However, achieving long-term operational stability under bending stress remains a significant hurdle. In this work, we identify fractures in the TiO₂ electron transport layer as the dominant source of performance degradation under mechanical deformation. To address this issue, we introduce a C₆₀ buffer layer atop the TiO₂, which serves dual functions: mechanical protection and enhanced interfacial charge extraction. The C₆₀ layer functions by redistributing strain through a shift of the neutral axis closer to the TiO₂ layer and by passivating interfacial trap states, as confirmed by SEM, AFM, PL, TRPL, and EIS analyses. As a result, SS-based PSCs with an optimized 20 nm C₆₀ layer demonstrate a remarkable ~5% increase in PCE before bending and an ~92.84% improvement in PCE retention after bending, compared to control devices. Furthermore, devices maintained superior performance over 100 bending cycles and continuous bending for 100 hours. These findings establish the C₆₀ buffer layer as a powerful strategy for enabling flexible PSCs with both high efficiency and mechanical reliability, accelerating their practical deployment in BIPV and VIPV systems where mechanical stress is unavoidable.

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Broader context

Flexible and durable perovskite solar cells (PSCs) are essential for emerging applications in building-integrated photovoltaics (BIPV) and vehicle-integrated photovoltaics (VIPV). This study addresses the mechanical and electrical challenges faced by stainless steel (SS)-based PSCs under bending conditions and proposes a strategy to enhance their stability and efficiency. By incorporating a 20 nm thick C₆₀ buffer layer, we significantly improved bending durability and charge extraction efficiency, mitigating damage to the TiO₂ layer. The optimized SS-based PSCs achieved a 92.84% improvement in PCE retention after bending, demonstrating the potential of C₆₀ integration as a viable approach for robust and flexible PSCs. These findings contribute to the advancement of high-performance, flexible photovoltaics for next-generation energy applications.

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Introduction

Recent years have witnessed substantial progress in the development of flexible solar cells tailored for Building-Integrated Photovoltaics (BIPV) and Vehicle-Integrated Photovoltaics (VIPV).^{1–4} Among these advancements, stainless steel (SS)-based perovskite solar cells (PSCs) have garnered significant attention due to their remarkable durability, superior mechanical strength, and flexibility, which surpass those of conventional flexible substrates.^{5–8} These attributes render SS-based PSCs highly suitable for demanding applications in BIPV and VIPV, where structural stability under mechanical stress is essential.^{9–12} Despite these advantages, SS-based PSCs continue to face critical challenges, particularly efficiency degradation when subjected to bending and mechanical stress. While SS-based PSCs have emerged as a promising alternative to overcome these limitations, the majority of research to date has remained focused on polymer-based substrates, such as polyethylene terephthalate (PET) and polyethylene naphthalate (PEN).^{13–16} Li *et al.* reported a flexible PSCs incorporating a bio-inspired multisite polymer, which achieved a power conversion efficiency (PCE) of 24.43% and retained 94.1% of its initial performance after 10 000 bending cycles under high humidity conditions.¹⁷ Similarly, Chalkias *et al.* demonstrated a carbon-based flexible PSCs fabricated under ambient air, achieving a PCE of 20.09% and maintaining mechanical stability over 5000 bending cycles.¹⁸ Furthermore, Dong *et al.* developed a fully printed flexible PSCs module that preserved 95% of its original efficiency after 3000 cycles of mechanical deformation.¹⁹ These studies collectively highlight key strategies to simultaneously enhance efficiency and mechanical robustness, including the introduction of elastic or ductile interlayers, surface modifications to improve interfacial adhesion and stress distribution, and structural designs that position functional layers near the neutral mechanical plane.

In environments such as construction and automotive applications, solar cells are frequently exposed to a range of stressors, including temperature fluctuations, physical impacts, prolonged moisture, and ultraviolet (UV) radiation.²⁰ The inherent mechanical strength of stainless steel offers a robust foundation capable of withstanding bending and deformation, ensuring the structural and functional stability of PSCs under such adverse conditions. Research into SS-based PSCs has shown considerable progress in recent years. For instance, in 2022, Feleki *et al.* achieved a PCE of 16.5% in p–i–n structured SS-based PSCs fabricated on polymer-coated SS substrates.⁵ Zheng *et al.* improved the PCE to 17.1% in 2023 by introducing an 80 nm indium tin oxide (ITO) interlayer and applying surface passivation techniques.⁷ In 2024, Zhou *et al.* further enhanced SS-based PSC performance, achieving a PCE of 20.2% by incorporating single crystals into the precursor solution to reduce perovskite defects and passivating the surface of the perovskite film.⁸

Despite these advancements, efficiency degradation under mechanical stress remains a persistent challenge for SS-based PSCs. Bending and deformation can lead to micro-crack

formation, delamination within the functional layers, and hindered charge transport, ultimately resulting in power loss.^{21,22} Moreover, mechanical stress exacerbates ion migration and layer instability within the perovskite material, further reducing operational efficiency. Therefore, improving the mechanical and operational stability of SS-based PSCs under bending conditions remains a pivotal research focus. While significant progress has been made in advancing SS-based PSCs, there is a notable gap in understanding the specific causes of efficiency degradation under bending conditions. Investigating these mechanisms is essential for enabling the practical application of SS-based PSCs in BIPV and VIPV, where mechanical robustness and long-term performance are critical.

In this work, we address the key mechanical limitations of SS-based PSCs, which are highly promising for real-world flexible photovoltaic applications. We identify the fracture of the TiO₂ electron transport layer as a critical factor contributing to performance degradation under bending conditions and propose the integration of a C₆₀ buffer layer as a dual-function solution that provides both mechanical stress relief and enhanced interfacial charge extraction. Unlike conventional approaches that focus solely on either flexibility or efficiency, our strategy simultaneously enhances both mechanical robustness and electronic performance. This study presents a novel design principle for realizing high-efficiency, mechanically stable SS-based PSCs, paving the way for their practical implementation in BIPV and VIPV. Notably, the optimized device incorporating a 20 nm C₆₀ buffer layer exhibited a PCE of 17.51% before bending and retained approximately 92.84% of its initial performance after bending.

Results and discussion

To explore the causes of efficiency degradation in SS-based PSCs, scanning electron microscopy (SEM) measurements were performed to observe structural changes induced by bending. The samples were subjected to a bending diameter of 10 mm for 1 hour prior to analysis. Fig. 1a and c present schematic representations of surface damage phenomena observed without and with the incorporation of a C₆₀ buffer layer, respectively. As depicted in Fig. 1b, the TiO₂ layer exhibits a smooth surface prior to bending, while clear fractures appear after bending. Conversely, when a C₆₀ buffer layer is incorporated, as shown in Fig. 1d, the TiO₂ layer remains intact, exhibiting no fractures even after bending. In addition, atomic force microscopy (AFM) measurements were conducted to evaluate surface roughness. The TiO₂ film displayed roughness values of 49 nm before bending and 144 nm after bending, indicating significant surface damage due to bending (Fig. S1a and S1c, ESI†). In contrast, the C₆₀/TiO₂ hybrid film showed roughness values of 15 nm before bending and 44 nm after bending, maintaining a significantly smoother surface compared to the single TiO₂ film (Fig. S1b and S1d, ESI†). Although both films displayed a similar relative increase in roughness, the absolute roughness of the C₆₀/TiO₂ film remained significantly lower. It should be noted, however, that the AFM measurements represent localized surface



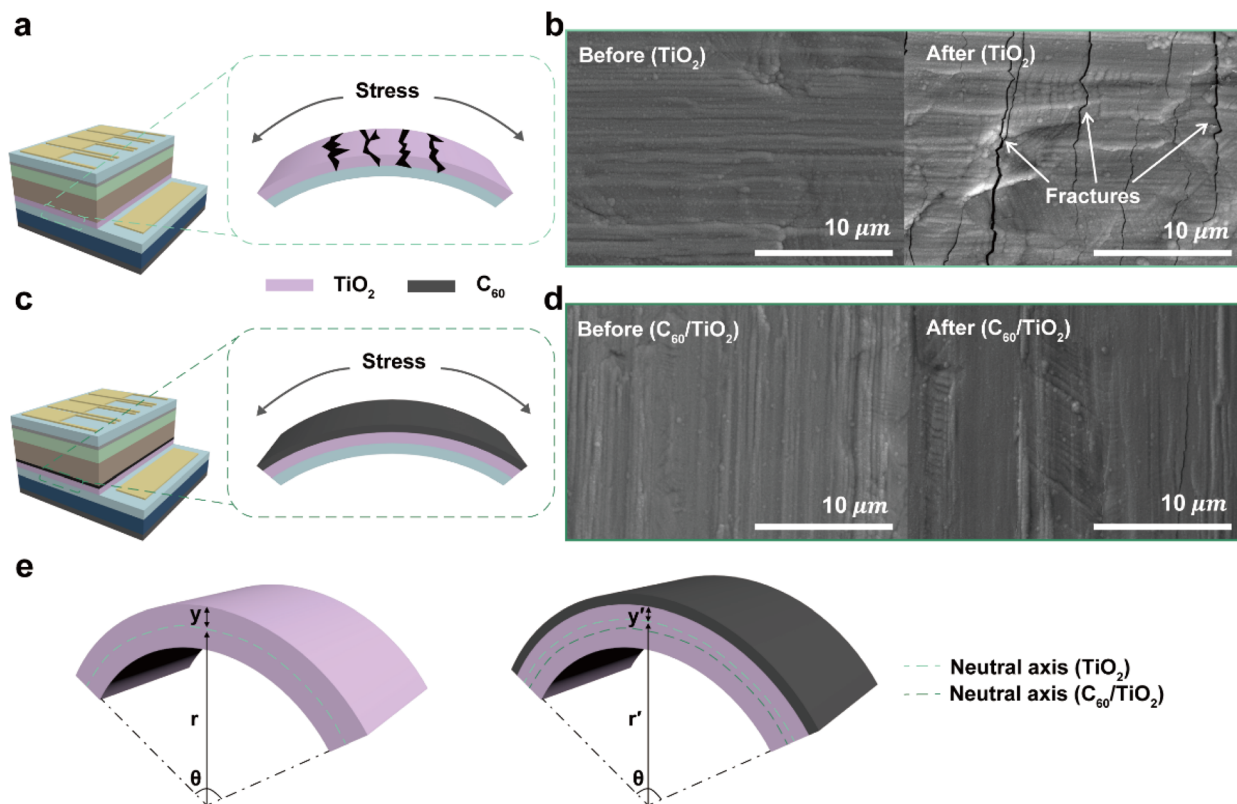


Fig. 1 Surface damage assessment of TiO₂ due to bending: (a) schematic illustration showing the surface damage of TiO₂ after bending. (c) Schematic illustration of C₆₀/TiO₂ deposited on SS-based PSCs after bending. (b) SEM images of TiO₂ before and after bending. (d) SEM images of C₆₀/TiO₂ deposited on SS-based PSCs before and after bending. (e) Schematic illustration of the neutral axis shifts in SS-based PSCs without and with the C₆₀ buffer layer.

characteristics and may not comprehensively reflect the overall stress distribution within the complete multilayered device under bending conditions. Therefore, the roughness data are used here as supportive indicators of morphological trends rather than as definitive predictors of mechanical failure. Further analysis of the indium tin oxide thin film using the same methodology revealed no fractures in the ITO layer after bending (Fig. S2, ESI†). These results indicate that preventing fractures in the TiO₂ layer is crucial for enhancing the efficiency and mechanical stability of SS-based PSCs.

The changes experienced by each layer in multilayered structures before and after bending are illustrated in Fig. S3, ESI†. In this analysis, y represents the distance from the neutral axis, R denotes the radius relative to the neutral axis, and θ indicates the central angle with respect to the neutral axis. When bending is applied, each layer undergoes stress (σ)—the force exerted to maintain its shape against external forces—and strain (ϵ), the deformation resulting from these forces.^{23–27} Specifically, layers above the neutral axis experience tensile forces, while layers below it are subjected to compressive forces. According to the stress–strain behaviour of ceramic materials, exceeding a certain stress threshold causes the material to lose its ability to return to its original state, ultimately leading to failure.²⁸ The relationships between ϵ and σ in the layers during bending are described by the equations shown in Fig. 1e.^{21,29,30}

$$\epsilon = \frac{(r + y)\theta - r\theta}{r\theta} = -\frac{y}{r} \quad (1)$$

$$\sigma = E \times \epsilon = -E \times \frac{y}{r} \quad (2)$$

While eqn (1) and (2) provide a fundamental analytical framework for evaluating strain and stress distributions in multilayer structures, they are based on idealized assumptions, including uniform Young's modulus and linear elastic behavior. Notably, the Young's modulus values used in the analysis are derived from bulk materials reported in the literature and may not accurately reflect the mechanical response of nanostructured thin films under bending deformation. As such, the results should be interpreted qualitatively, emphasizing relative trends rather than absolute values.

When a C₆₀ layer is introduced on top of the TiO₂ layer, the neutral axis (N) of the layered structure is theoretically expected to shift slightly. The position of the neutral axis can be estimated using eqn (3), assuming ideal layer homogeneity and isotropy:^{21,31}



$$N = \frac{\sum_{i=1}^n E_i t_i \left[\left(\sum_{j=1}^i t_j \right) - \frac{t_i}{2} \right]}{\sum_{i=1}^n E_i t_i} \quad (3)$$

where E is Young's modulus, n is number of layer, and t is thickness of layer. During bending, layers above the neutral axis experience tensile forces, increasing surface stress. Consequently, layers with a higher Young's modulus are more susceptible to damage, as Young's modulus quantifies the material's elastic deformation under applied stress (σ). Materials with higher Young's modulus values are more prone to failure than those with lower values. Among the components of SS-based PSCs, TiO_2 has the highest Young's modulus of 151 GPa (Table S1, ESI†). For the TiO_2 and $\text{C}_{60}/\text{TiO}_2$ composite structures, the neutral axis values are 25.00 nm and 29.94 nm, respectively, indicating that the C_{60} buffer layer slight shifts the N. The ε and σ values for the TiO_2 layer are 5.00×10^{-6} and 7.55×10^{-4} GPa, respectively. However, in the $\text{C}_{60}/\text{TiO}_2$ composite structure, the ε and σ on the C_{60} layer are 8.01×10^{-6} and 4.96×10^{-4} GPa, respectively, while the values for the TiO_2 layer decrease to 4.01×10^{-6} and 6.05×10^{-4} GPa, respectively. These reductions in ε and σ for the TiO_2 layer—approximately 19.80% and 19.87%, respectively—significantly mitigate the risk of damage to the TiO_2 thin film. This shift—together with

the relatively compliant nature of the C_{60} interface—may help reduce stress and strain within the brittle TiO_2 layer during bending. This reduction is attributed to the shift in the neutral axis, which brings the TiO_2 layer closer to the neutral plane, reducing ε , and to the ability of the C_{60} layer to absorb strain energy. Additionally, the low Young's modulus of the C_{60} layer enables it to effectively redistribute σ , providing enhanced protection for the TiO_2 layer. The calculated values align closely with experimental results, underscoring the importance of introducing a buffer layer to improve the bending stability of SS-based PSCs.

To fabricate SS-based PSCs with a C_{60} buffer layer, the effects of C_{60} on the perovskite crystal structure were investigated. Fig. 2a shows the SS304 substrate and the chemical structure of C_{60} used as the buffer layer in this study. To investigate molecular interactions between perovskite and C_{60} , X-ray photoelectron spectroscopy (XPS) was conducted. In Fig. 2b, the binding energy peaks of $\text{I } 3\text{d}_{5/2}$ and $\text{I } 3\text{d}_{3/2}$ in the MAPbI_3 film appear at 618.68 eV and 630.18 eV, respectively. For the $\text{MAPbI}_3/\text{C}_{60}$ composite layer, these peaks shift to lower values by 0.4 eV and 0.2 eV, respectively, indicating strong electronic interactions between C_{60} and I^- ions due to charge transfer.^{32,33} Similarly, Fig. 2e shows that the binding energy peaks of $\text{Pb } 4\text{f}_{7/2}$ and $\text{Pb } 4\text{f}_{5/2}$ in the MAPbI_3 film, originally at 136.98 eV and 141.88 eV, shift to lower values by 0.3 eV and 0.4 eV, respectively, in the $\text{MAPbI}_3/$

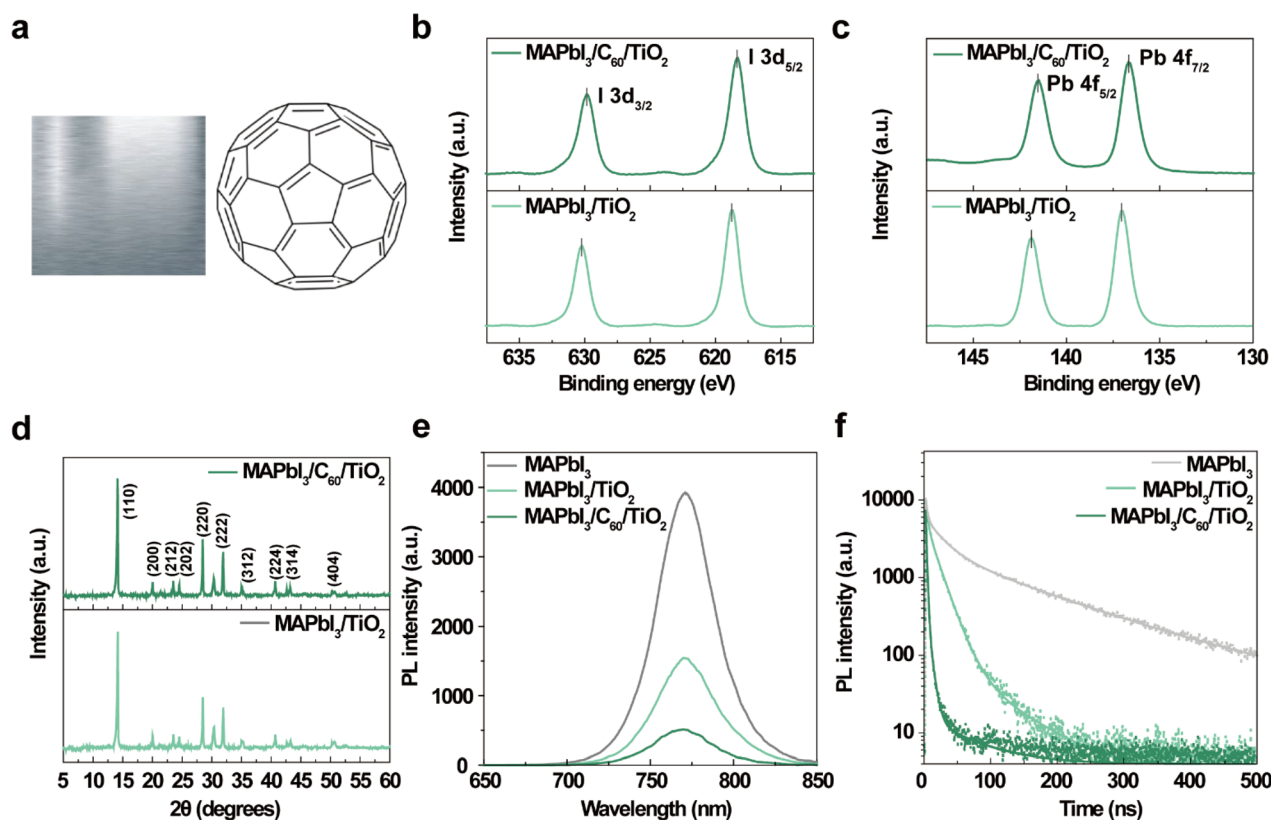


Fig. 2 Assessment of C_{60} characteristics and suitability as an interlayer: (a) image of SS substrate (left) and chemical structure of the C_{60} (right). (b) XPS spectra showing the I 3d peaks for $\text{MAPbI}_3/\text{TiO}_2$ and $\text{MAPbI}_3/\text{C}_{60}/\text{TiO}_2$ hybrid films. (c) XPS spectra showing the Pb 4f peaks for perovskite/ TiO_2 and $\text{MAPbI}_3/\text{C}_{60}/\text{TiO}_2$ hybrid films. (d) XRD patterns of the $\text{MAPbI}_3/\text{TiO}_2$ and $\text{MAPbI}_3/\text{C}_{60}/\text{TiO}_2$ hybrid films. (e) Steady-state PL spectra and (f) time-resolved PL decay spectra of $\text{MAPbI}_3/\text{TiO}_2$ and $\text{MAPbI}_3/\text{C}_{60}/\text{TiO}_2$ hybrid films.



C₆₀ composite structure. This negative shift indicates strong interactions between C₆₀ and Pb²⁺ ions, which contribute to defect passivation and enhanced interfacial charge transfer.³² The crystallization of perovskite on the SS substrate was analyzed using X-ray diffraction (XRD), as shown in Fig. 2d. MAPbI₃/C₆₀/TiO₂ films and MAPbI₃/TiO₂ films were prepared on SS substrates *via* the same deposition process. Both samples exhibit distinct diffraction peaks at 14.11° and 28.45°, corresponding to the (110) and (220) planes of MAPbI₃, respectively.^{34,35} The similarity in diffraction intensity between MAPbI₃/C₆₀/TiO₂ and MAPbI₃/TiO₂ indicates that the incorporation of C₆₀ does not alter the crystallinity of the perovskite, confirming that a highly crystalline MAPbI₃ thin film can be formed on the SS substrate even in the presence of C₆₀. Charge extraction properties were

further analyzed using steady-state photoluminescence (PL) and time-resolved photoluminescence (TRPL) measurements. Fig. 2e shows that all samples exhibit a PL peak at 770 nm, originating from MAPbI₃. The PL quantum yield significantly decreases with the incorporation of TiO₂ and C₆₀, demonstrating efficient charge carrier extraction from MAPbI₃ to C₆₀.^{36,37} The most pronounced PL quenching observed in the MAPbI₃/C₆₀/TiO₂ structure indicates superior carrier extraction facilitated by C₆₀.³⁸ TRPL decay curves for MAPbI₃, MAPbI₃/TiO₂, and MAPbI₃/C₆₀/TiO₂ samples are shown in Fig. 2f, with detailed lifetime values provided in Table S2.† For the MAPbI₃ sample, the fast lifetime (τ_1) and average lifetime (τ_{ave}) were calculated as 14.09 ns and 66.30 ns, respectively. With the introduction of the C₆₀ buffer layer, these values decreased to 8.24 ns and 52.34 ns, respectively,

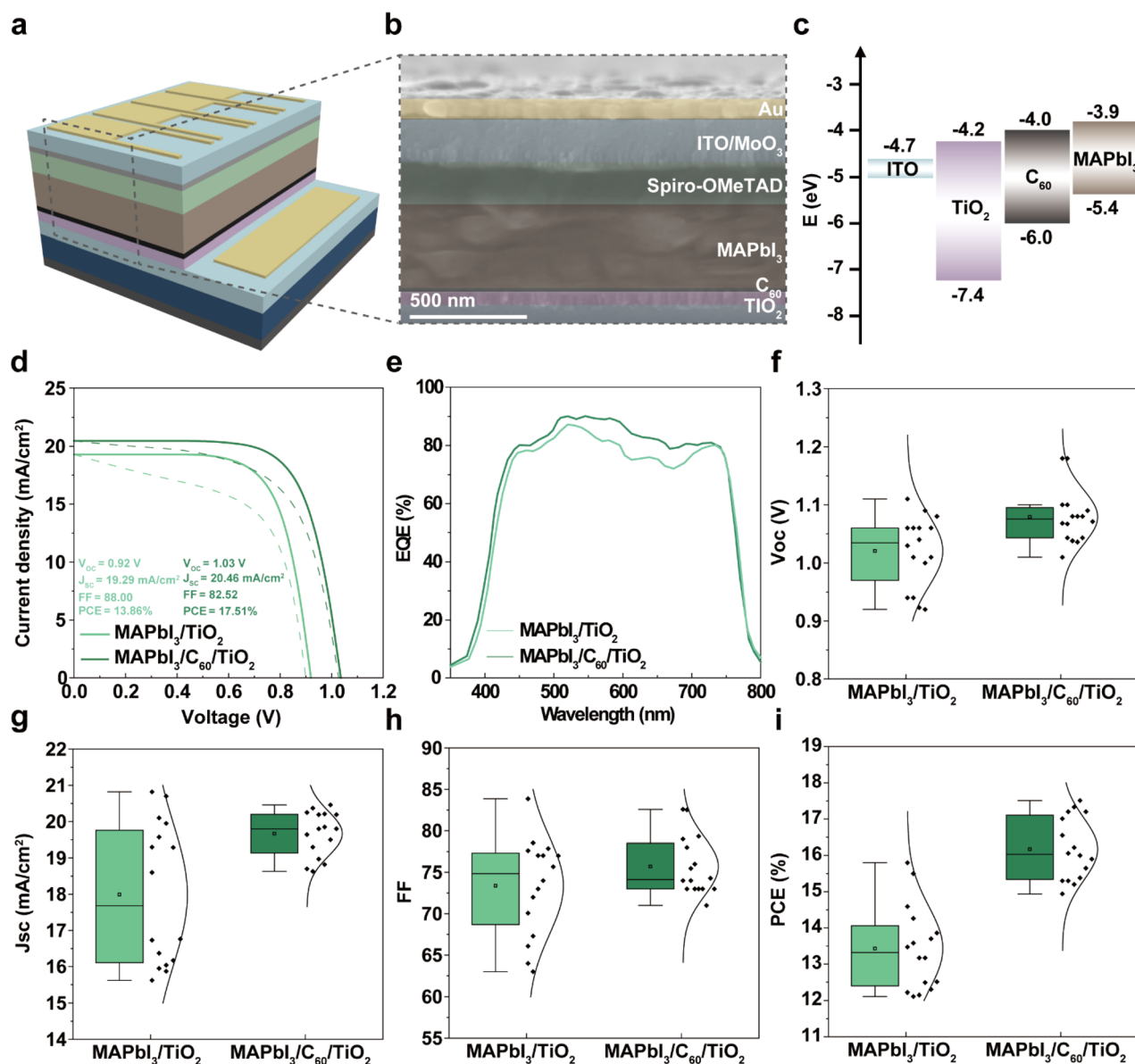


Fig. 3 Characterization and performance of SS-based PSCs: (a) schematic illustration of SS-based PSCs. (b) Cross-sectional SEM image of SS-based PSCs. (c) Energy level diagram of SS-based PSCs. (d) *J*–*V* characteristics of the most efficient devices with and without the C₆₀ layer (solid: reverse, dash: forward). (e) EQE plots of devices with and without the C₆₀ layer. (f–i) Statistical deviation of the photovoltaic parameters of the SS-based PSCs with and without the C₆₀ layer in the reverse scanning direction. (The error bar represents standard deviation from 16 devices).



indicating faster PL quenching and higher electron injection efficiency, ultimately enhancing photovoltaic performance.³⁹

Fig. 3a shows the schematic of the fabricated SS-substrate-based PSC. The corresponding SEM cross-sectional image of the device is shown in Fig. 3b. The fabrication process of the device is illustrated in Fig. S4, ESI†. Due to the opaque nature of the SS substrate, light illumination was applied from the top side of the device. To enable this, a transparent ITO electrode was deposited on the top surface, followed by patterned Au deposition that served as the charge-collecting electrode while allowing light to pass through the ITO openings. This top-illumination configuration ensures accurate photovoltaic characterization of the SS-based PSCs (Fig. S5, ESI†). Fig. 3c shows the energy level diagram of the SS-based PSC, where the C₆₀ buffer layer efficiently extracts photogenerated electrons from the perovskite to the TiO₂ layer. This highlights the role of C₆₀ in facilitating charge separation and enhancing photovoltaic performance. To optimize C₆₀ thickness, devices with varying C₆₀ layers (5 nm, 10 nm, 20 nm, and 30 nm) were fabricated and measured under AM 1.5G illumination at 100 mW cm⁻² (1 sun). The perovskite crystal structure remained unaffected by C₆₀ variation (Fig. S6, ESI†). At 5 nm, the device achieved an open-circuit voltage (*V*_{oc}) of 1.00 V, a short-circuit current density (*J*_{sc}) of 21.48 mA cm⁻², a fill factor (FF) of 68.90, and a power conversion efficiency of 14.83% (Fig. S7a, ESI†). At 10 nm, the device showed a slightly improved PCE of 16.07%, while *V*_{oc}, *J*_{sc}, and FF remained nearly unchanged (Fig. S7b, ESI†). The highest performance was achieved at 20 nm with a *V*_{oc} of 1.03 V, a *J*_{sc} of 20.46 mA cm⁻², an FF of 82.52, and a peak PCE of 17.51% (Fig. 3d). At 30 nm, the PCE dropped to 14.75% due to a decrease in FF to 74.60 (Fig. S7c, ESI†). EQE spectra (Fig. S8, ESI†) confirmed that performance improved with increasing C₆₀ thickness up to 20 nm, but declined at 30 nm. Devices with thinner C₆₀ layers (5 nm and 10 nm) exhibited incomplete surface coverage on ITO, limiting performance. In contrast, the 20 nm C₆₀ layer achieved better surface coverage, improved charge extraction and overall efficiency. At 30 nm, the thicker C₆₀ layer partially absorbed sunlight, which reduced carrier generation and lowered performance.⁴⁰ These results indicate that 20 nm is optimal for C₆₀ thickness. Fig. 3d shows *J*-*V* curves comparing devices with and without 20 nm C₆₀. The champion device achieved a high PCE of 17.51%, a *V*_{oc} of 1.03 V, a *J*_{sc} of 20.46 mA cm⁻², and an FF of 82.52, significantly outperforming the device without the C₆₀ layer, which exhibited a PCE of 13.86%, a *V*_{oc} of 0.92 V, a *J*_{sc} of 19.29 mA cm⁻², and an FF of 88.00. The 20 nm C₆₀ layer improved PCE by ~4%. To evaluate the hysteresis behavior of the devices, forward and reverse *J*-*V* scans were performed before bending. The device without the C₆₀ exhibited significant hysteresis, as evidenced by the large discrepancy between forward (dashed) and reverse (solid) scans. In contrast, the C₆₀-buffered device showed a markedly reduced hysteresis, indicating improved interfacial charge extraction and suppressed ion migration at the TiO₂/perovskite interface. Fig. 3e illustrates the EQE spectra in the wavelength range of 400–800 nm, showing higher EQE values for C₆₀-incorporated devices. Box plots in Fig. 3f–i summarize performance data from 16 devices with and without C₆₀. The 20 nm C₆₀ layer

slightly improved and stabilized *V*_{oc} and *J*_{sc}, due to reduced interfacial recombination and enhanced charge transport.⁴¹ These trends align with PL spectra results (Fig. 2g). The most notable improvement was in PCE, mainly from stabilized FF along with slight *V*_{oc} and *J*_{sc} increases. These results confirm that C₆₀ improves both the interfacial quality and the overall photovoltaic performance.⁴² To investigate the reasons behind the improved photovoltaic performance, SEM measurements were conducted (Fig. S9, ESI†). Perovskite grains grown on the C₆₀/TiO₂ composite layer were significantly larger than those grown directly on the TiO₂ substrate. This is attributed to the C₆₀ buffer layer, which lowers interfacial energy between TiO₂ and the perovskite precursor solution. This reduction in interfacial energy improves wetting properties during the crystallization process, facilitating the formation of larger grains. Furthermore, the C₆₀ layer mitigates the surface roughness and defects of the TiO₂ substrate, providing a smoother surface that promotes unobstructed grain growth.⁴³ Additionally, the fullerene-based C₆₀ buffer layer serves as a passivation layer, effectively suppressing interfacial trap states^{44,45} Besides electron transport, the C₆₀ layer passivated interfacial trap states and blocked I⁻ ion migration, suppressing PbI₂ formation from reactions between I⁻ and TiO₂ oxygen vacancies.⁴⁶

To evaluate the potential application of C₆₀-incorporated SS-based PSCs in BIPV and VIPV systems, the efficiency change under bending conditions was analyzed. Fig. 4a presents a schematic diagram of the fabricated SS-based PSCs, while Fig. 4b (left image) shows the fabricated SS-based PSCs and the right image illustrates the cell bent to a diameter of 10 mm. As shown in Fig. 4c, the SS-based PSC without C₆₀ incorporation, bent to a diameter of 10 mm, exhibited a *V*_{oc} of 0.77 V, a *J*_{sc} of 17.20 mA cm⁻², a FF of 50.00, and a PCE of 6.70%. Compared to the unbent condition, the PCE decreased by approximately 7.16% after bending, indicating that the device is unsuitable for applications requiring various curved forms, such as those in BIPV and VIPV systems. In contrast, as shown in Fig. 4b, the C₆₀-incorporated SS-based PSCs, bent to a diameter of 10 mm, achieved a *V*_{oc} of 1.01 V, a *J*_{sc} of 17.82 mA cm⁻², a FF of 71.69, and a PCE of 12.92%. Compared to the unbent condition, the PCE exhibited a reduction of only 4.59%, which is significantly lower than the 7.16% reduction observed in devices without C₆₀ incorporation. Moreover, the PCE improved by 6.22% compared to devices prior to the introduction of C₆₀. After bending, the difference in hysteresis became even more pronounced. As shown in Fig. 4c, the device without the C₆₀ buffer layer exhibited aggravated hysteresis behavior due to mechanical damage in the TiO₂ layer, whereas the device incorporating the C₆₀ buffer layer maintained superior mechanical and electrical stability. Fig. 4d illustrates the EQE values of cells with and without C₆₀ incorporation after bending to a diameter of 10 mm. It is evident that the EQE values of the cells without C₆₀ are significantly lower than those of the cells with C₆₀. This finding suggests that C₆₀ not only enhances charge extraction through surface modification but also partially prevents degradation of the TiO₂ layer during bending. Fig. 4e–h show box plots comparing the *V*_{oc}, *J*_{sc}, FF, and PCE values of 16 SS-based PSCs with and without C₆₀ incorporation after bending to a diameter of 10 mm. When a 20 nm thick



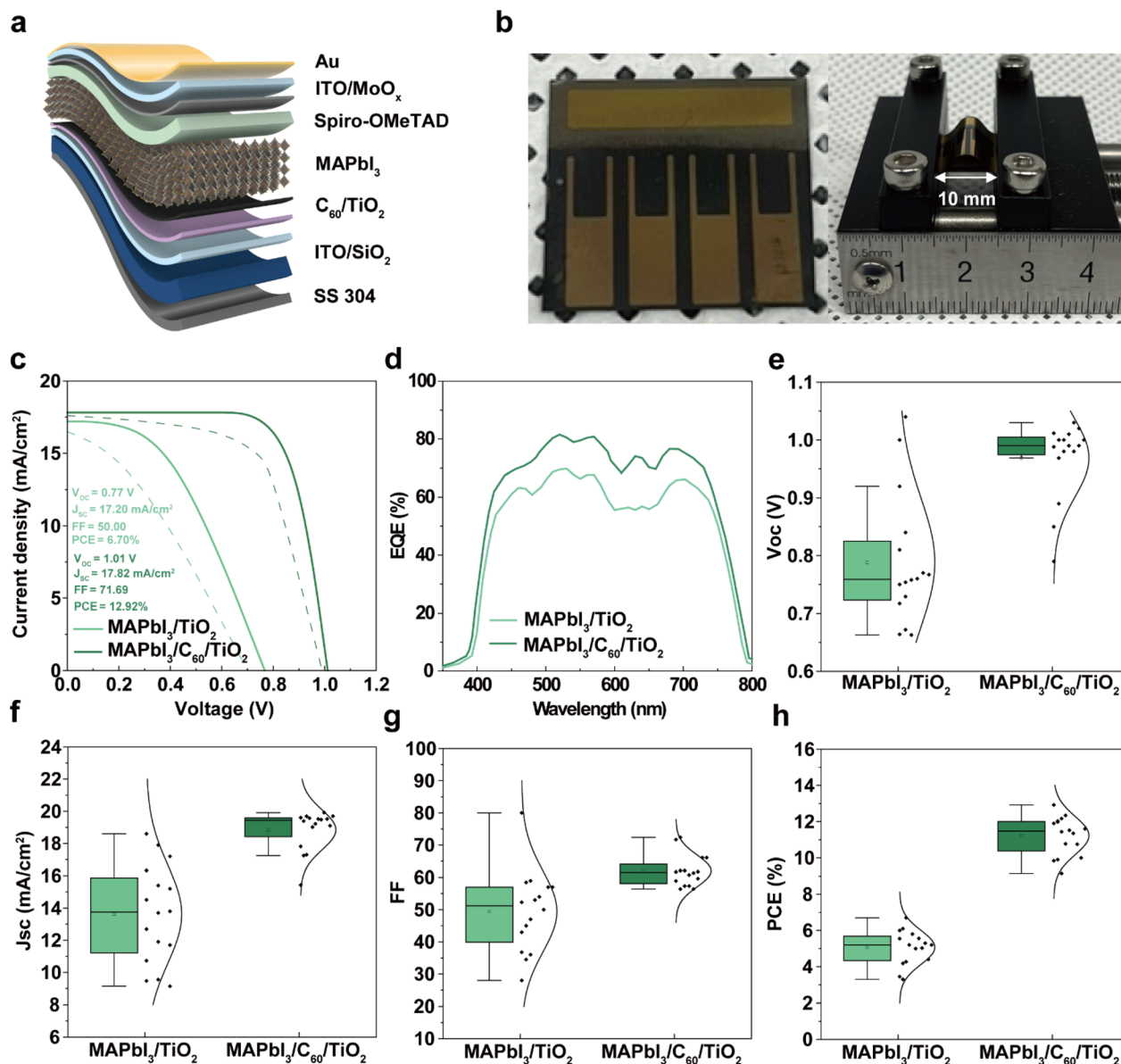


Fig. 4 Performance of SS-based flexible PSCs after bending: (a) schematic illustration of the SS-based flexible PSCs. (b) Images of SS-based flexible PSCs before and after bending. (c) J - V characteristics of the most efficient devices after bending with and without the C₆₀ layer (solid: reverse, dash: forward). (d) EQE plots of devices after bending with and without the C₆₀ layer. (e–h) Statistical deviation of photovoltaic parameters of the SS-based PSCs after bending with and without the C₆₀ layer in the reverse scanning direction. (The error bar represents standard deviation from 16 devices).

C₆₀ layer was incorporated into SS-based PSCs, post-bending performance significantly improved compared to devices without the C₆₀ layer. While the FF showed a slight increase, noticeable enhancements were observed in the V_{oc} , J_{sc} , and PCE. This improvement is attributed to the ability of C₆₀ to reduce defects at the TiO₂ interface, suppress interfacial recombination, and mitigate structural damage to the TiO₂ layer during bending. These properties allow the device to maintain high performance under mechanical stress. The incorporation of C₆₀ demonstrates significant potential for enabling the application of SS-based PSCs in BIPV and VIPV systems. The performance of previously reported SS-based PSCs has been summarized in Table S3, ESI.†

To understand why the incorporation of C₆₀ prevents performance degradation in SS-based PSCs after bending, the stress concentration factor (K) was analyzed.⁴⁷ K quantifies the concentration of stress due to load transfer obstruction at specific points, such as notches and tips. The value of K is governed by the following equation:^{48,49}

$$K = \frac{\sigma_{\max}}{\sigma_{\text{nom}}}, \quad K = 1 + \beta \cdot \left(\frac{R_p}{\lambda} \right) \quad (4)$$

$$\sigma_{\max} = \left(1 + \beta \cdot \left(\frac{R_p}{\lambda} \right) \right) \cdot \sigma_{\text{nom}} \quad (5)$$

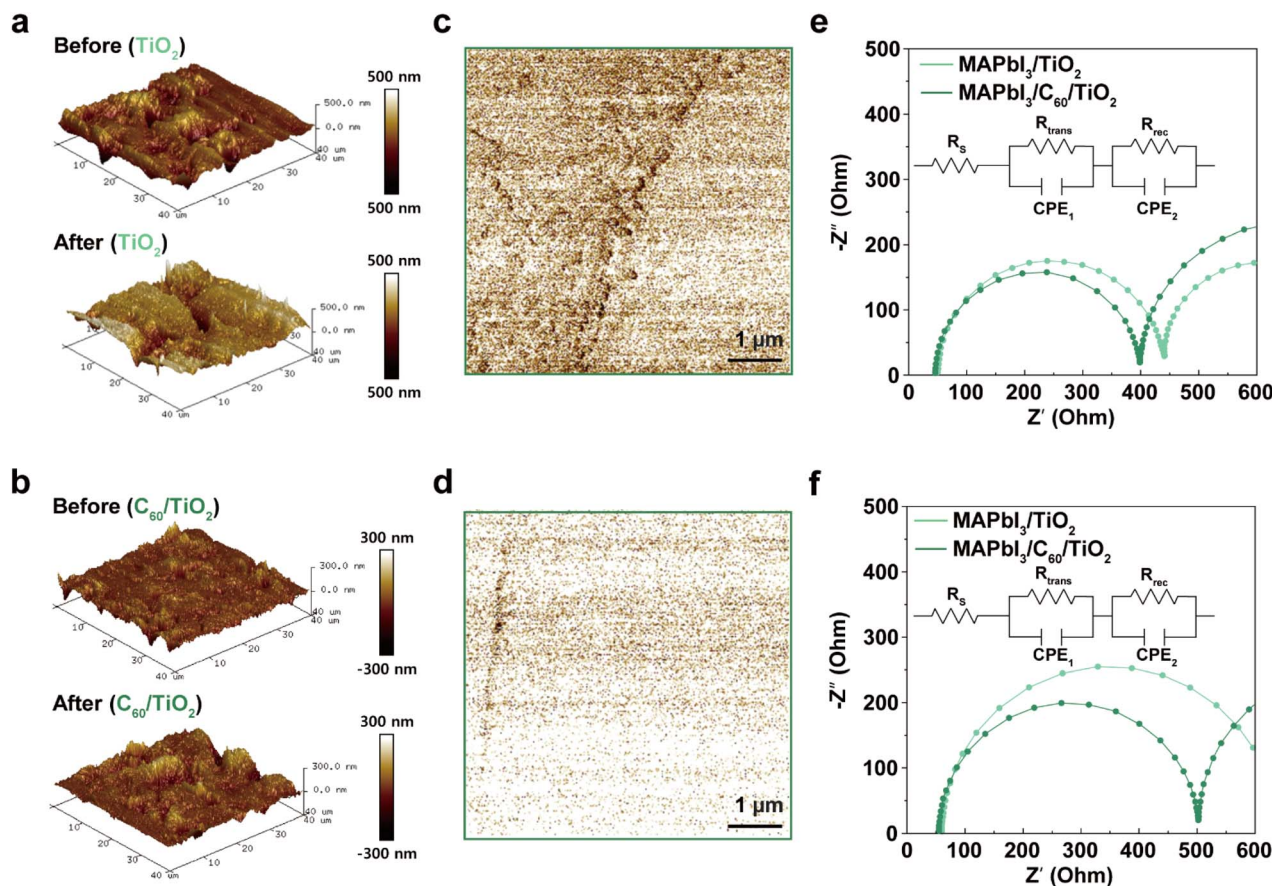


Fig. 5 Structural and electrical properties before and after bending: AFM 3D image of the device before and after bending (a) without (before RMS: 49.44 nm, R_a : 87.37 nm, R_p : 677.40 nm) (after RMS: 144.21 nm, R_a : 130.83 nm, R_p : 818.20 nm) (height range: -500 to $+500$ nm) and (b) with (before RMS: 15.92 nm, R_a : 10.71 nm, R_p : 293.00 nm) (after RMS: 44.23 nm, R_a : 30.02 nm, R_p : 386.90 nm) (height range: -300 to $+300$ nm) C_{60} . C-AFM image of the device after bending (c) without (min: 0.02 nA, max: 6.72 nA, mean: 2.38 nA) and (d) with (min: 0.19 nA, max: 10.43 nA, mean: 6.54 nA) C_{60} . Nyquist plot of SS-based PSCs without and with C_{60} (e) before and (f) after bending.

where R_p is the roughness peak-to-valley distance, σ_{max} is the maximum stress, σ_{nom} is nominal stress, β is the geometric influence coefficient and λ is a parameter related to surface characteristics. When R_p increases due to greater surface discontinuities or the formation of additional peaks and notches, the value of K also increases, as described by the equations. Therefore, reducing R_p is essential to minimize the stress applied to the TiO_2 layers. Fig. 5a and b investigate the R_p values before and after bending, both with and without the incorporation of C_{60} . For devices without C_{60} , the R_p values were 677.40 nm and 818.20 nm before and after bending, respectively. However, with the introduction of C_{60} , the R_p values were significantly reduced to 293.00 nm before bending and 386.90 nm after bending, corresponding to reductions of 56.75% and 52.71%, respectively. This improvement in R_p effectively reduces the stress applied to the TiO_2 layer, thereby preventing fractures during bending. These results underscore the critical role of C_{60} in enhancing the mechanical stability of SS-based PSCs under bending conditions. However, although these expressions provide a simplified estimation of local stress amplification due to surface features, they do not fully account for the complex interplay of interfacial adhesion, material

compliance, and multilayer coupling in the real device. The mechanical benefits of the C_{60} layer are not solely attributed to morphology smoothing. Rather, the C_{60} buffer is believed to act as a compliant interfacial layer that enhances mechanical coupling and accommodates local strain, while also passivating surface defects that may act as crack initiation sites.

To evaluate the impact of TiO_2 substrate fracture on conductivity, C-AFM measurements were conducted. Fig. 5c presents the results for the device without C_{60} after bending. The dark regions represent non-conductive areas, while the bright regions indicate conductive areas.^{50,51} The film without C_{60} exhibited an average current level of 2.38 nA. In contrast, when C_{60} was incorporated, the film displayed significantly higher conductivity, as shown in Fig. 5d.^{52,53} The average current level increased to 6.54 nA. This observation aligns with the previously reported efficiency data for SS-based PSCs, demonstrating a similar trend. These findings indicate that the incorporation of C_{60} effectively reduces stress on the TiO_2 layer during bending, contributing to the maintenance of the device's efficiency under mechanical stress. To further investigate the effects of the C_{60} layer on charge extraction and device stability under bending conditions, electrochemical impedance



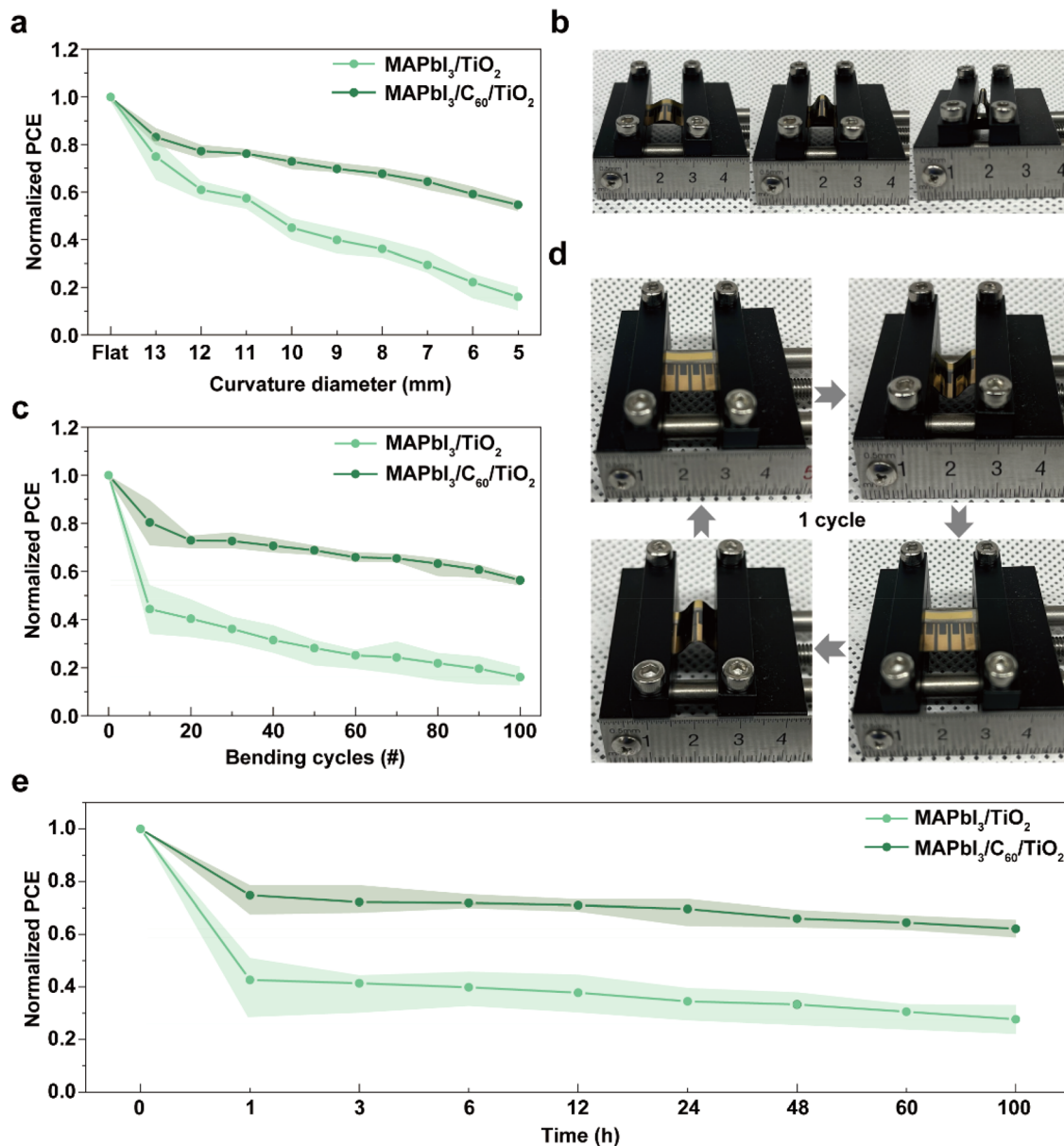


Fig. 6 Stability test of SS-based flexible PSCs after bending: (a) PCE measured after bending the substrate to diameters ranging from flat to 5 mm. (b) Images of devices bent to diameters of 12 mm, 9 mm, and 5 mm. (c) PCE measured over bending cycles ranging from 0 to 100. (d) Images of the devices after 1 bending cycle. (e) PCE measured after bending the substrate within a specified bending time of 0 to 100 h.

spectroscopy (EIS) measurements were performed. The Nyquist plots in Fig. 5e compare the EIS data of devices with and without the C₆₀ layer before bending. The device with C₆₀ exhibits a significantly smaller semicircle in the high-frequency region, indicating a reduced charge transfer resistance (R_{trans}). This improvement is attributed to the C₆₀ layer's ability to enhance charge extraction at the MAPbI₃/TiO₂ interface by reducing interfacial defects and facilitating efficient electron transport. Furthermore, the semicircle in the low-frequency region, representing recombination resistance (R_{rec}), is notably larger in the device with C₆₀. The increased R_{rec} demonstrates effective suppression of charge recombination at the interface, contributing to the enhanced performance of the device.⁵⁴ Fig. 5f

illustrates the EIS data for devices with and without the C₆₀ layer after bending. Bending introduces mechanical stress that degrades the TiO₂ layer and increases interfacial defects. For the device without C₆₀, R_{trans} increases significantly, as evidenced by the enlarged high-frequency semicircle. In contrast, the device with C₆₀ maintains a relatively smaller R_{trans} , emphasizing the protective role of C₆₀ in preserving charge transport pathways. Additionally, while the low-frequency semicircle (R_{rec}) shrinks for both devices due to increased defect density caused by bending, the reduction in R_{rec} is less pronounced in the device with C₆₀. This indicates that the C₆₀ layer mitigates recombination losses even under mechanical stress. These findings confirm that the incorporation of C₆₀ not only

enhances charge extraction efficiency but also provides improved structural stability to the device under bending conditions. These improvements reflect not only reduced surface stress but also enhanced interfacial integrity and defect tolerance enabled by the C_{60} layer. By reducing stress concentration factors, facilitating efficient electron transport, and suppressing charge recombination, the C_{60} layer significantly contributes to the mechanical and operational stability of SS-based PSCs.⁵⁴

To evaluate the morphological and functional stability of C_{60} -incorporated SS-based PSCs under mechanical deformation, PCE measurements were conducted under various static and dynamic bending conditions. Rather than aiming to extract classical mechanical parameters, this experiment was designed to assess the device performance and interface durability under realistic bending stress. Fig. 6a presents the results of PCE measurements as the bending diameter was adjusted from a flat state to a diameter of 5 mm. The PCE degradation rate was significantly lower in devices with C_{60} incorporation compared to those without, suggesting enhanced tolerance to bending-induced morphological disruption. Fig. 6b displays images of the devices at bending diameters of 12 mm, 9 mm, and 5 mm, illustrating their structural flexibility under increasing mechanical strain. In the second evaluation, dynamic mechanical stress was applied *via* repeated bending cycles. As shown in Fig. 6c, when the number of bending cycles increased from 0 to 100, devices with C_{60} incorporation exhibited a markedly lower PCE degradation rate compared to the control. Fig. 6d shows representative images during cyclic deformation. Finally, Fig. 6e illustrates the long-term PCE stability under sustained static bending (10 mm diameter) over 100 hours. Devices with C_{60} maintained significantly higher PCE values compared to those without C_{60} , indicating suppressed degradation under prolonged mechanical stress. These results demonstrate that C_{60} incorporation improves the mechanical reliability of SS-based PSCs not by altering classical stress distributions, but by mitigating localized morphological damage and enhancing interfacial durability under bending.

Conclusions

This work highlights the dual role of a 20 nm C_{60} interlayer in SS-based PSCs, demonstrating its contribution to both enhanced mechanical durability and photovoltaic performance under bending stress. The incorporation of C_{60} shifted the neutral axis closer to the brittle TiO_2 layer and reduced the effective strain and stress by $\sim 20\%$, as supported by theoretical and experimental analysis. In addition, the C_{60} layer reduced R_p , mitigated the K , and improved charge extraction efficiency. Importantly, C_{60} provided structural protection to the electron transport layer while simultaneously enhancing the crystallinity of the active perovskite layer, resulting in greater resilience to mechanical deformation. As a result, C_{60} -incorporated devices retained 6.2% higher PCE after bending compared to controls. These findings support the use of compliant interfacial layers such as C_{60} to simultaneously enhance the mechanical

robustness and operational stability of PSCs, which is particularly relevant for emerging applications in BIPV and VIPV.

Methods

Materials

SS 304 substrates with a thickness of 0.05T were used. Dimethyl sulfoxide (anhydrous, 99.9%) (DMSO), chlorobenzene (anhydrous, 99.9%), *N,N*-dimethylformamide (anhydrous, 99.8%) (DMF), acetonitrile (anhydrous, 99.8%), fullerene- C_{60} , lead(II) iodide (PbI_2), diethyl ether, 4-*tert*-butylpyridine (96%), and lithium bis(trifluoromethanesulfonyl)imide (Li-TFSI) were purchased from Sigma-Aldrich. Methylammonium iodide (MAI) was procured from dyesol, and 2,2',7,7'-tetrakis [*N,N*-di(4-methoxyphenyl)amino]-9,9'-spirobifluorene (spiro-OMeTAD) was obtained from Lumtec.

Fabrication of perovskite solar cell

The SS substrates were sequentially cleaned by sonication in acetone, ethanol, and isopropanol for 15 minutes each. Subsequently, the substrates were treated with ultraviolet (UV)-ozone for 30 minutes. To serve as a diffusion barrier, a 1 μm layer of SiO_2 was deposited onto the SS substrates *via* plasma-enhanced chemical vapor deposition (PECVD). The TiO_2 layer, with a target thickness of 50 nm, was fabricated through RF magnetron sputtering at a chamber pressure below 7×10^{-7} mTorr. C_{60} layers were deposited by thermal evaporation at varying thicknesses of 5, 10, 20, and 30 nm. A 1 M perovskite precursor solution was prepared by dissolving stoichiometric amounts of PbI_2 and MAI in a 1 : 1 (v/v) mixture of DMSO and γ -butyrolactone (GBL). The solution was stirred at 70 °C for 2 hours and filtered using a 0.2 μm PTFE syringe filter. Subsequently, the solution was deposited onto the substrate using a two-step spin-coating process: 1000 rpm for 10 seconds, followed by 5000 rpm for 60 seconds. During the second step, 1000 μL of chlorobenzene was dropped onto the center of the perovskite film as an antisolvent to facilitate the crystallization of perovskite grains. The substrate was annealed at 100 °C for 1 hour to complete the crystallization of the perovskite layer. For the hole transport layer (HTL), spiro-OMeTAD powder was dissolved in a solution containing 28.8 μL of 4-*tert*-butylpyridine, 520 mg of Li-TFSI in 1 mL of acetonitrile, and 1 mL of chlorobenzene. The prepared solution was applied onto the substrate and spin-coated to form a thin layer. A 10 nm thick MoO_x buffer layer was then thermally evaporated, followed by the deposition of a 160 nm thick ITO transparent electrode using RF magnetron sputtering. Finally, a 100 nm thick Au electrode was deposited through thermal evaporation.

Materials characterization

Scanning electron microscopy (SEM) was performed using a Quanta 250 FEG microscope (FEI). X-ray diffraction (XRD) patterns were obtained using an X-ray diffractometer (Rigaku) with Cu-K α radiation ($\lambda = 1.54 \text{ \AA}$). X-ray photoelectron spectroscopy (XPS) measurements were conducted with a Thermo Scientific K-Alpha system equipped with a monochromated Al



K α X-ray source. Photoluminescence (PL) spectra were measured on a JASCO FP-8500 spectrofluorometer. Lifetime measurements were carried out using a 470 nm picosecond laser (PicoQuant, Germany) as the excitation source. Atomic force microscopy measurements were performed using a Dimension 3 Edge AFM system (Bruker). Conductive atomic force microscopy (C-AFM) was employed to measure conductivity using the Dimension Edge C-AFM system.

Device characterization

A class AAA solar simulator was used to measure the J - V characteristics of the devices at a scanning rate of 0.05 V s^{-1} , using a Keithley 2400 instrument. The AM 1.5G (1 sun, 100 mW cm^{-2}) solar power was calibrated using a silicon reference solar cell. All J - V measurements were performed with a 0.075 cm^2 mask, and the scan voltage setting time was 200 ms. The incident photon-to-current conversion efficiency (IPCE) was measured using equipment from HS Technology Inc. Electrochemical impedance spectroscopy measurements were conducted under simulated AM 1.5G illumination at an intensity of 1 mA cm^{-2} using an electrochemical measurement system (InViumStat.XR, InVium Technologies). EIS measurements were performed over a frequency range of 1 Hz to 1 MHz.

Data availability

The data supporting this article have been included as part of the ESI.†

Author contributions

H.-S. Lee and D. H. Kim supervised the overall project. H. J. Lee and K. Kim were responsible for developing concrete strategies, data curation, formal analysis, investigation, and writing the original draft and editing. S. Lee and D. Pyun performed data curation and formal analysis. J.-S. Hwang, J. Nam, S. Cho, and S.-H. Jeong performed formal analysis. D. Kim and Y. Kang performed project administration. All authors have read and approved the manuscript.

Conflicts of interest

There are no conflicts to declare.

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