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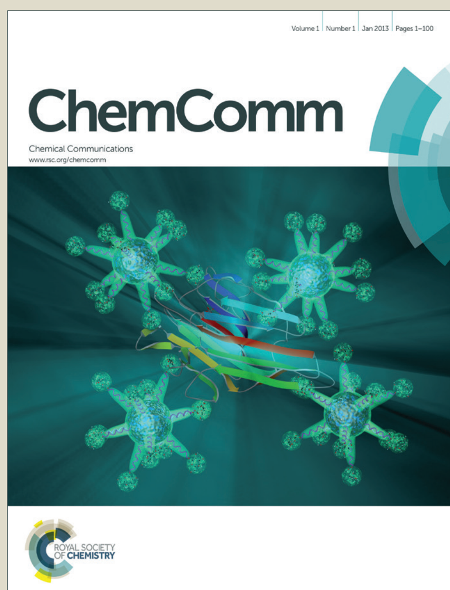

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A Novel Method to Prepare Photolithographic Polymer Shadow Masking: Toward High-Resolution High-Performance Top-Contact Organic Field Effect Transistors†

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A novel and universal method, based on water-solubility poly (4-styrene sulfonate), was introduced into the preparation of a polymer mask. Using this mask, high-resolution, high-performance, bottom-gate, top-contact (OFETs) can be achieved. There is no intervention of the solvent in the process of manufacturing these OFETs and the mask can be recycled.

For small molecular semiconductors, the universal existence of grain boundaries in their deposited films will trap the charge carrier when they are applied in organic field-effect transistors (OFETs), [1-3] further leading to cannot represent the intrinsic properties of materials. To this end, small-channel-length electrodes provide an effective pathway to decrease the grain boundary. It is well known that high-resolution, bottom-gate, bottom-contact (BGBC) configuration OFETs can be easily processed by traditional photolithography [4-7] and improved photolithography [8] directly patterning electrodes on the dielectric layer. However, top-contact devices possess larger injection areas and more favourable injection paths compared with bottom-contact devices. [9] These benefits result in lower contact resistance and better performance. Therefore, it is more reasonable to prepare high-resolution, top-contact OFETs. Unfortunately, the metal mask has a limited resolution of 30 μm and the rigid texture does damage to the surface of semiconductor. Therefore, it is still a big challenge to create high-resolution, bottom-gate, top-contact (BGTC) configuration OFETs. So far, there are two ways to realize this objective. One is orthogonal photolithography [10-11] and another is the high-resolution mask method [12-15]. Although the former minimizes any possible damage to the organic semiconductor film associated with processing the photoresist, the solution-effect is still non-ignorable. By contrast, the latter attracts more attention because it doesn't involve any solvent in the process of fabricating devices. Among the masks, a full-wafer stencil [14-15] can be used to obtain high-resolution, top-contact OFETs, but the cost of raw and processed materials, including silicon nitride (SiN) membranes and the bulk silicon (Si) supporting layer, is too high, not to speak of the poor performance. Besides, polymer-based masks were also introduced to pattern nanostructures in the previous reports, [12-13] but the tiring preparation technology, including a multi-step deposition and etch, led to high cost. In our work, by means of photolithography and water-solubility poly (4-styrene sulfonate) (PSS), a new polymer shadow masking is effortlessly prepared, which is not only based on low-cost and low processing temperature (80 ^{o}C) for polystyrene (PS) and polymethyl methacrylate (PMMA), but also based on high processing temperature for polyacrylonitrile (PAN) (150 ^{o}C) and polyimide (PI, 300 ^{o}C). With this polymer mask, high-resolution (3 μm), top-contact OFETs with pentacene as the active layer are achieved. It is to be highlighted that there is no intervention of the solvent in the process of manufacturing top-contact OFETs and the mask can be recycled. It is exhilarating to realize that mobility is improved when compared with ordinary shadow masking (30 μm). We believe this method will provide a good stage to further process top-contact, highly-integrated organic circuits.

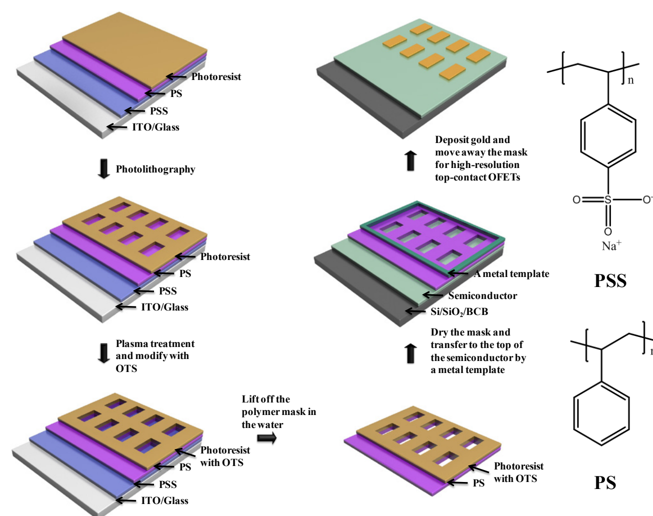

Fig. 1 The schematic diagram of manufacturing the polymer mask based on PS with the chemical structures of PSS and PS in the inset of this figure.

Polystyrene (PS) was used as an example to illustrate the whole process. The detailed procedure used to manufacture the polymer mask, included the following steps as shown in Fig. 1: i)

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poly (sodium-4-styrene sulfonate) (PSS), polystyrene (PS) (the chemical structures of PSS and PS shown in the inset of Fig.1) and photoresist were orderly spin coated onto Indium Tin Oxide (ITO)/glass substrate and then annealed at 150 °C, 80 °C and 95 °C in sequence; ii) the substrate was exposed under UV irradiation for 15 s and then developed to pattern the source/drain electrodes; iii) plasma treatment (200W, 10min) was performed on this substrate to remove the uncovering PS; iv) after plasma treatment, the surface of the residual photoresist was hydrophilic (Fig. S1a, ESI†), which was unfavourable for the polymer mask lifting from the Indium Tin Oxide (ITO)/glass substrate in the water. Therefore, octadecylsilane (OTS) was modified on the surface of residual photoresist to insure its hydrophobicity (Fig. S1b, ESI†); v) the substrate was gradually immersed into the deionized water and the water would enter into the PSS layer (Fig. S2a, ESI†) to make the upper film (polystyrene (PS) and photoresist) float on the surface of the water to finish the key step of this polymer mask; vi) the polymer mask was transferred to the top of the semiconductor on the surface of pentacene/silicon dioxide with divinyltetramethyldisiloxane-bis (benzocyclobutene) (BCB) modified using a metal supporting plate (Fig. S2b, ESI†) with the visible electrodes mask shown in Fig. 2a; vii) depositing gold (20 nm) and then the mask was moved away to finish the final high-resolution, top-contact OFETs with channel length of 3 μm, 4 μm and 5 μm (Fig. 2b).

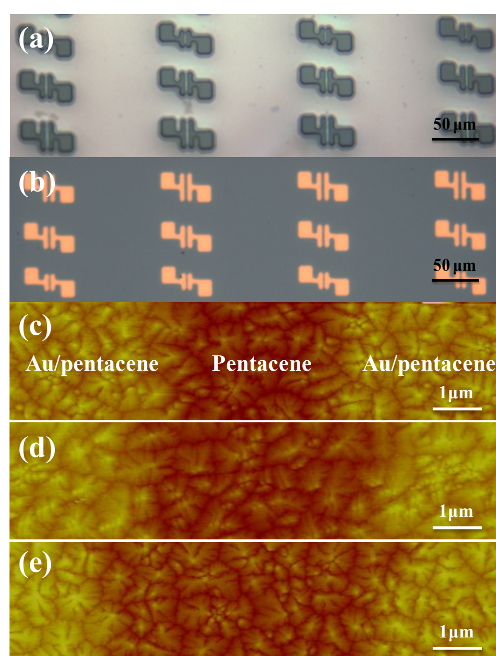

Fig. 2 (a) Physical presentation diagram of the masks with different channel size. (b) Device arrays on the substrate. Different channel size (c) 3 μm, (d) 4 μm and (e) 5 μm of gold electrodes on the Pentacene/BCB/SiO_2/Si substrate.

In order to complete the polymer mask successfully, the PSS layer was considered first. The selection of this material considered two main points: 1) it was water-soluble [16-17] and could easily form a flat membrane on the ITO surface; 2) it did not dissolve in the organic reagents (acetone, toluene, and chloroform). Secondly, the thickness of PS and photoresist was also a significant consideration. Because of the frangibility of extremely thin PS film and the time-consuming nature of plasma treatment with thick PS film, 500 ± 50 nm PS film was selected for the mask preparation. Simultaneously, 2 μm photoresist was spin coated on the PS to act as the protecting layer, which, on the one hand, protected PS layer not completely being eliminated and on the other hand reinforced PS through the residual layer. It is worth mentioning that the polymer mask could be easily supported by the metal supporting plate and the deionized water on it could rapidly evaporate. Besides the strip-structure electrodes mentioned in Fig. 2b, other structures (Fig. S3, ESI†) of gold electrodes on the silicon oxide with OTS modified are also manufactured using this mask. It needed to be stressed that other polymer materials (PMMA, PAN and PI) could also be applied into the process of fabricating the mask using the same method (Fig. S4, ESI†). It had been acknowledged that good physical contact between the mask and the semiconductor was another main issue. In view of suppleness of the polymer mask, downward deposition method was adopted to prepare the source/drain electrodes on these two surfaces. It was believed that gravity would enhance the adhesion of the mask to the surface adding the downward pressure of the metal supporting plate itself. The results proved that our approach did work. Different channel size (3 μm, 4 μm and 5 μm) of electrode arrays (Fig. 2b) were successfully obtained on pentacene/silicon dioxide with BCB modified. Atomic force microscope (AFM) was measured to further indicate that there was very clean inside the triumphant channel (3 μm, 4 μm and 5 μm) (Fig. 2c-e).

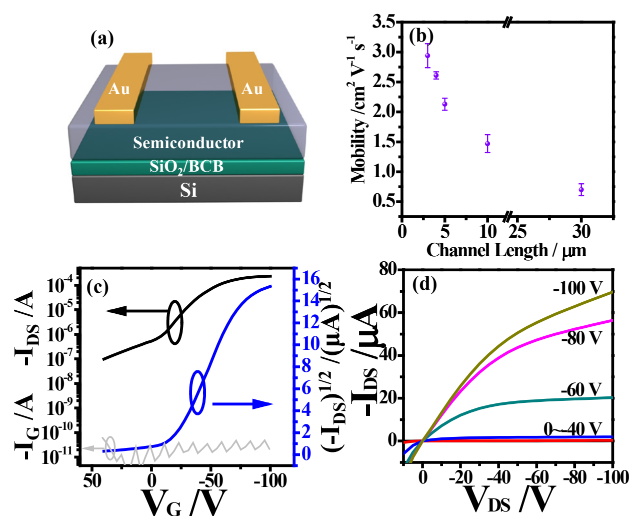

Fig. 3. (a) The structure of top-contact OFET. (b) The mobility as a function of channel length. (c) Typical transfer characteristic of the transistor based on pentacene with 3 μm channel length. (d) Typical output characteristic of the transistor based on pentacene with 3 μm channel length.

Grain boundary was an important feature of morphology that affected the performance of the OFETs. Under normal circumstances, deep and dense grain boundaries led to lower mobility because the grain boundaries resembled defects blocking the transmission of the carrier. As shown in Fig. S5 in the ESI†, when big-channel-length electrodes (such as 30 μm or even bigger) were adopted, it was obvious that a large number of grain boundaries were observed in the film and that there was a

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corresponding increase in the number of holes that were trapped. With the decrease in channel length, fewer holes were trapped and therefore the material will achieve a higher performance level. Furthermore, BGTC OFETs (Fig. 3a) were fabricated using this polymer mask. Devices with different small-channel lengths (3 µm, 4 µm, 5 µm and 10µm) based on pentacene through polymer mask and 30 µm channel lengths by copper mask functioning as contradistinctive electrodes are shown in Fig. 3b. The mobility of the devices prepared by the polymer mask was better than those prepared by the copper mask. The mobility increased from 0.84 $cm^2 V^{-1} s^{-1}$ (30 µm) to 3.2 $cm^2 V^{-1} s^{-1}$ (3 µm). The representative transfer characteristics of the best transistor (based on 3 µm channel length) are shown in Fig. 3c with negligible leakage current and their corresponding output curve is shown in Fig. 3d. What's more, it was evident that the threshold voltage decreased with the channel length decreasing (especially below 5µm), which was ascribed to the short-channel effect and also excluded the idea that high performance resulted from the high threshold voltage (Fig. S6, ESI†). This excellent result was ascribed to the small channel length, which decreased the number of trapped holes in the grain boundaries and then further improved the performance. It is noted that the mask could be recycled and applied without any changes at least ten times on different substrates (Fig. 4), which was much cheaper than the commercial copper-net electrode template. This polymer mask could be continued to be used in the following fabrication after ten times employment (Fig. S7, ESI†).

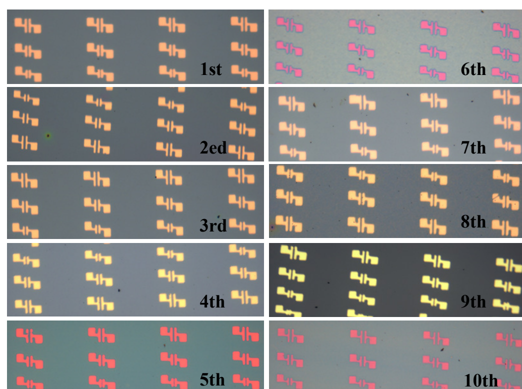

Fig. 4. The situation of this polymer mask repeatedly used on different substrate (at least for ten times).

In summary, a polymer mask based on PS and other polymers, such as PMMA, PAN and PI, was fabricated by photolithography. By means of this polymer mask, high-resolution, top-contact OFETs were prepared without the intervention of the solvent and the mask can be recycled. The introduction of small channel had reduced grain boundaries and accordingly improved the performance of the devices. We believe that this polymer mask could be further applied in patterning the semiconductor and would provide a good stage to further process top-contact, highly- integrated organic circuits.

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