PCCP

Accepted Manuscript

ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/pccp

Solution-processed N-type Fullerene Field-Effect Transistors Prepared Using CVD-grown Graphene Electrodes: Improving Performance with Thermal Annealing

Yong Jin Jeong,[a] Dong-Jin Yun,[b] Jaeyoung Jang,[a] Seonuk Park,[a] Tae Kyu An,[a] Lae Ho Kim,[a] Se Hyun Kim,[c,] and Chan Eon Park,[a,*]*

[a] Polymer Research Institute, Department of Chemical Engineering, Pohang University of Science and Technology, Pohang, 790-784, Korea.

[b] Analytical Science Laboratory of Samsung Advanced Institute of Technology, SAIT, Yongin 446-712, Republic of Korea

[c] Department of Nano, Medical and Polymer Materials, Yeungnam University, Gyeongsan, North Gyeongsang 712-749, South Korea

ABSTRACT

Solution-processed organic field effect transistors (OFETs), which are amenable to facile large-area processing methods, have generated significant interest as key elements for use in all-organic electronic applications aimed at realizing low-cost, lightweight, and flexible devices. The low performance levels of *n*-type solution-processed bottom-contact OFETs unfortunately continue to pose a barrier to commercialization. In this study, we introduced a combination of CVD-grown graphene source/drain (S/D) electrodes and fullerene (C_{60}) in a solution-processable *n*-type semiconductor toward the fabrication of *n*-type bottom-contact OFETs. The C_{60} coating in the channel region was achieved by modifying the surface of the oxide gate dielectric layer with a phenyl group-terminated self-assembled monolayer (SAM). The graphene and phenyl group in the SAMs induced π-π interactions with C_{60}, which facilitated the formation of a C_{60} coating. We also investigated the effects of thermal annealing on the reorganization properties and field-effect performances of the overlaying solution-processed C_{60} semiconductors. We found that thermal annealing of the C_{60} layer on the graphene surface improved the crystallinity of the face-centered cubic (*fcc*) phase structure, which improved the OFET performance and yielded mobilities of 0.055 cm^2/Vs. This approach enables the realization of solution-processed C_{60}-based FETs using CVD-grown graphene S/D electrodes via inexpensive and solution-process techniques.

KEYWORDS: organic field effect transistor, graphene, chemical vapor deposition, *n*-type organic semiconductors, fullerene, solution process, thermal annealing

1. INTRODUCTION

Organic field-effect transistors (OFETs), which are compatible with low-temperature and solution processing methods, have received significant attention as key elements for realizing commercially viable all-organic electronics, including cheap, light, flexible, and large-area electronic products.[1-3] These advantages may be accessed primarily by depositing the organic semiconductors onto substrates using various solution processes including novel techniques (spin-coating, layer-by-layer, or Langmuir-Blodgett technique).[4-7] Numerous studies have attempted to rationally design solution-processable organic semiconductors composed of small molecules and polymers, such as triethylgermylethynyl-substituted anthradithiophene (diF-TEG ADT) or 2,7-dioctyl[1]benzothieno[3,2-b][1]benzothiophene (C8-BTBT), in an effort to achieve a high oxidation stability and good electrical performance.[8, 9] Pentacene, fullerene (C_{60}), and their derivatives have been extensively studied in small molecule semiconductors.[10-12] Among these, C_{60} and its derivatives have been most attractive because they are soluble in a variety of organic solvents.[13, 14] However, the studies on the solution-processable C_{60}-based FETs reported to date have focused only on the effects of surface modifications on the insulating layer and solvent dependence of the formation of a stable C_{60} thin film, and the electron transfer properties.[15-17] As the field progresses, understanding the characteristics of electrode/semiconductor interfaces has become important because the crystallinity of a semiconductor deposited on an electrode may depend on the surface properties of the electrodes in a bottom-contact configuration. Source/drain (S/D) electrodes are typically patterned prior to the deposition of an organic semiconductor layer.[18-20] This configuration avoids damaging the organic semiconductor films during certain patterning processes.[21] The development of appropriate S/D electrode materials is, therefore, vital. Metal S/D electrodes (e.g. gold, aluminum, and calcium) are typically used in

OFETs, even though these electrodes have hydrophilic surfaces that can hinder uniform C_{60} film formation via solution processing.[22, 23]

CVD-grown graphene films have recently been considered as potential alternative S/D electrodes for use in OFETs due to their thinness, high electrical conductivity, and good oxidation/thermal stabilities.[24-26] The two-dimensionally flat sp^2 carbon network of a graphene film can interact with the molecules of a carbon-based organic semiconductor including C_{60}.[26-28] This organic/organic interface between graphene and organic semiconductor could reduce the contact resistance compared to the metal/organic semiconductor interface having high contact resistance due to the formation of an unfavorable interface dipole layer.[20, 29, 30] To enlarge the benefits of graphene S/D electrodes, it is necessary to investigate the growth behavior of C_{60} molecules on graphene, and the ways to improve the crystalline morphology of C_{60} on the graphene, with a goal to enhance device performance.

Here, we prepared a C_{60} thin film deposited on graphene S/D electrodes using solution processing techniques toward the fabrication of bottom-contact OFETs for the first time. Moreover, we studied the effects of thermal annealing on the crystallinities, morphologies, and OFET performances of C_{60} thin films on graphene. Uniform C_{60} thin films may be obtained by treating the surfaces of the oxide dielectric layers with self-assembled monolayers (SAMs) that include terminal phenyl groups.[31] Higher annealing temperatures physicochemically reorganized the C_{60} molecules and yield their thin films on the graphene electrodes with better crystallinities and *fcc* structures. The resulting OFETs exhibited high performances with a maximum mobility of 0.055 cm^2/Vs using the graphene S/D electrodes. This study enables the realization of C_{60} bottom-contact FETs using CVD-grown graphene S/D electrodes via inexpensive and solution-process techniques.

2. EXPERMINTAL SECTION

The graphene was synthesized on a 25 μm thick copper foil using CVD methods at low pressures. The graphene layers were then transferred onto a pre-cleaned SiO_2/Si substrate, as described previously.[22, 32] The CVD-grown graphene was monolayer films with some existing bilayer island from the scanning electron microscopy image and Raman spectra, shown in Figure S1 in Supporting Information.[33, 34] The SiO_2/Si substrate was cleaned by piranha treatment, followed by multiple DI water rinses and then further cleaned by exposure to UV-ozone (UVO) for 20 min. After thermal annealing above 350 °C for 1h to obtain the cleaned graphene surface, the graphene was patterned by using standard photolithography. The device fabrication steps are briefly summarized in Figure 1. A negative-type photoresist (PR) was spin-coated onto the graphene films and then exposed to UV light through a photo-mask. The PR was then washed away using developer and DI water. All parts of the graphene films other than the part used as a S/D or contact electrode were not covered by the PR and were etched with the O_2 plasma. The phenyl group-terminated SAM treatment was accomplished by applying phenyltrimethoxysilane (PTS) ($C_6H_5Si(OCH_3)_3$, 97 %, Aldrich Co.) to the 300 nm thick SiO_2/Si substrates. The substrates were exposed to UVO for 10 min and then to PTS vapor at 140°C for 40 min. The substrates were then baked at 120°C for 20 min. After the PR had been removed in a warm acetone solution (Figure S2 shows the optical microscopy image of patterned graphene electrodes without contact pad), a 0.6% C_{60} solution in dichlorobenzene was spin-coated to cover the substrates with graphene S/D electrodes. The C_{60} thin film coatings were thermally annealed at 50, 90, or 130°C for 1 h and then were slowly cooled to room temperature in a vacuum chamber. The channel width (W) of the OFETs was 1000 μm, and the channel lengths (L) were

20, 50, 100, or 150 μm. The C_{60} was spin-coated onto the substrates in a N_2-rich glove box, and the other fabrication steps were performed in ambient air (RH: 40%±10%).

All electrical measurements were performed using a Keithley 4200 SCS in a N_2-rich glove box. The morphologies of the C_{60} films were investigated using atomic force microscopy (AFM, Multimode AFM, Digital Instruments), and their θ-2θ mode out-of-plane X-ray diffraction (XRD) patters and two-dimensional grazing incidence wide-angle XRD (2D-GIXD) patterns were collected using a synchrotron X-ray beam source at the 5A and 3C beamline of the Pohang Accelerator Laboratory (PAL). The work functions of the graphene electrodes and the energy level alignment of the C_{60}/graphene structures were investigated using ultraviolet photoelectron spectroscopy (UPS, beam diameter: 5 mm). The top-surface regions of the C_{60} layers were cleaned using an Ar gas cluster ion beam sputtering process prior to the UPS measurements in order to remove air contamination and any oxidized C_{60} layers. The optical band gap of C_{60} was studied using reflective electron energy loss spectroscopy (REELS, using an electron gun and a photodetector manufactured by PSP Vacuum Technology Ltd.). The water contact angles were measured using SEO300A.

3. RESULTS AND DISCUSSION

The water contact angles (θ_{water}) on the UVO-exposed and PTS-modified SiO_2/Si substrates (prepared using the vapor deposition method) were measured to confirm whether the substrates were effectively modified with PTS by the vapor deposition method. Figure 2a shows the optical images captured while the water droplets were seeded onto the UVO- and PTS-modified SiO_2/Si substrates. The values of θ_{water} on the pristine SiO_2/Si substrates were less than 1°, whereas those obtained from the PTS-modified SiO_2/Si substrates were found to be ~54±2°, which are smaller than the values reported for the PTS-modified SiO_2/Si substrates prepared using the solution dipping method.[35, 36] In addition, the contact angle of dichlorobenzene on PTS SAM modified substrates had the value of ~11±2° (Figure S3), in good agreement with the reported values.[37] These results suggested that the SiO_2/Si substrate surfaces were effectively modified with the PTS-SAM.

The wettability of C_{60} at the electrode and channel regions was examined by spin-casting 25 nm thick C_{60} films onto the substrates bearing graphene S/D electrodes. The channel areas were modified with the PTS-SAM or were left unmodified. C_{60} was only deposited onto the graphene electrodes in the substrate prepared without the PTS modification, and the C_{60} layer was fully dewetted from the SiO_2 (Figure 2b). By contrast, the PTS modification allowed C_{60} to form a wetted film on the channel, leading to the successful deposition of C_{60} films onto both the graphene and channel regions (Figure 2c). These results may have been facilitated by π-π interactions between the C_{60} molecules and the two-dimensional carbon sheet formed by a honeycomb lattice of graphene and phenyl groups in the PTS-SAM.[16, 31] In this way, it was possible to fabricate bottom-contact C_{60} FETs using spin-coating techniques if the graphene and PTS-SAM were organized as an S/D electrode and a channel modifying layer, respectively. On

the other hand, the metal electrodes prepared with aluminum could not be used in solution-processed C_{60} FETs with a bottom-contact geometry because C_{60} aggregated on the metal electrodes during the spin-coating process, as shown in Figure S4.

High OFET performances require a highly crystalline semiconductor thin films that favors effective charge transport and enhanced mobility.[38] Previous studies have used thermal treatment with heating around 100°C to enhance the crystallinity of C_{60} in a polymer gate dielectric, resulting in improved OFET performances.[15] In the present work, C_{60} thin films deposited onto graphene were annealed at a variety of temperatures. AFM, XRD, 2D-GIXD, and UPS analyses were performed to examine the effects of thermal annealing on the crystalline morphology and electronic structure of the C_{60} film on graphene, as well as to establish the optimal conditions (such as annealing temperature (T_A)) for achieving a high OFET performance.

Figures 3a–3c show the AFM topography images and height profiles of C_{60} thin films prepared on graphene S/D electrodes after thermal annealing at three different T_A values of 50, 90, or 130°C, respectively. The C_{60} molecules in the films deposited on graphene formed a miliary topology of small ellipsoidal balls. Some of the C_{60} molecular bunches formed aggregates on the graphene electrode in the films that were thermally annealed at 50°C, whereas the self-organized C_{60} molecules were present in the films deposited on graphene after thermal annealing at 90 or 130°C. The rms roughness (R_{ms}) of the C_{60} films annealed at 50°C was much higher than the value obtained after annealing at 90 or 130°C. The cross-sectional height profiles revealed that the C_{60} layer formed a flat and smooth film on graphene after thermal annealing at 90 or 130°C, whereas some C_{60} molecules were aggregated to form 20~40 nm thick bunches on graphene after thermal annealing at 50°C

In addition to the morphological studies conducted using AFM analysis, we also investigated

the X-ray diffraction patterns to analyze the crystalline structure of the C_{60}/graphene bilayer. Figure 4a shows the Θ-2Θ mode out-of-plane XRD patterns obtained from the thermally annealed C_{60} films deposited onto graphene at various T_A values. As shown in the XRD patterns, the out-of-plane XRD peak intensity obtained from the C_{60} film annealed at 130°C was much higher than the corresponding peaks in films annealed at 50°C or 90°C, suggesting better crystallinity along the out-of-plane direction as a result of thermal annealing at high T_A. The intense peak at $q_z = 0.75$ A^{-1} and the small peak at $q_z = 1.52$ A^{-1} in the out-of-plane XRD patterns obtained from a C_{60} thin film corresponded to the (111) and (311) reflections, respectively. Previous studies revealed that the C_{60} crystals formed a face-centered cubic (*fcc*) phase structure.[15, 17, 39]

The relationship between the crystallinity and T_A was further explored and an in-depth analysis of the crystalline structure of the C_{60} thin films prepared on graphene was conducted by collecting 2D-GIXD measurements. Figures S5a–S5c show the 2D-GIXD patterns obtained from a C_{60} layer annealed at various T_A. The 2D-GIXD patterns obtained from the C_{60} film annealed at 130°C displayed reflection spots with apparent intensities that were higher than those obtained from other patterns, strongly suggesting that the C_{60} molecules formed more extensive crystal structures as T_A increased, in good agreement with the XRD analysis.

The hypothesis described above, that the C_{60} crystals formed an *fcc* phase structure, was tested by indexing the 2D-GIXD patterns collected from C_{60} films deposited onto graphene and thermally annealed at 130°C. The measured patterns were compared with C_{60} *fcc* reference patterns reported in previous studies, as shown in Figure 4b.[40-42] The lower spectrum shown in Figure 4b reveals the integrated GIXD intensity in the in-plane direction. All structural information collected from the XRD and 2D-GIXD profiles indicated that the crystalline growth

in the C_{60} films formed an *fcc* phase structure on graphene. Some peaks were absent, and even the 2D-GIXD profile peaks observed in Figure 4b had lower intensities than the corresponding peaks obtained from reference *fcc* C_{60} structures. Because film formation via solution processing may be disrupted by the presence of solvent molecules, solution-deposited C_{60} molecules formed random crystalline domains more frequently than did C_{60} molecules deposited through vacuum evaporation processes.

The electron injection barrier at the C_{60}/graphene interface was examined by collecting UPS spectra and performing REELS analyses of the C_{60}/graphene structures annealed at different T_A. Figures 5a, 5b, and 5c show the UPS spectra (secondary cut-off and valence band region) and REELS spectra of C_{60}/graphene films annealed at different T_A. The graphene layers examined here were thermally treated at 350°C for 1 h to remove the polymer residue that remained after the transfer process. In general, thermal treatment of transferred graphene induced charge transfer between graphene and SiO_2, which resulted in *p*-type graphene doping.[26] Therefore, the work functions of the thermally annealed graphene films were found to be 4.81 eV based on the UPS data (Figure 5a). The vacuum level shift and electron injection barrier ($\Phi_{E.B}$) between C_{60} and graphene were calculated using the UPS and REELS spectra. $\Phi_{E.B}$ was calculated from the difference between the lowest unoccupied molecular orbital (LUMO) level of C_{60} and the Fermi energy level (E_f) of graphene. This value also corresponded to the difference between the band gap (E_g) and the hole injection barrier ($\Phi_{H.B} = E_{HOMO} - E_f$, where HOMO refers to the highest occupied molecular orbital). The band gap of the C_{60} film deposited onto each sample was measured directly from the electron energy level difference between the zero-energy loss position and the onset of the minimum energy loss peak in the REELS spectra.[43, 44] Although the band gap of an organic semiconductor measured using REELS data is generally lower than the

corresponding transport band gap due to the exciton binding energy difference,[43, 44] the band gap obtained using the REELS technique, which is relatively insensitive to the substrate-induced charge carrier concentration, was used to characterize the electron injection barrier at the C_{60}/graphene interface. Despite the crystallinity differences among the C_{60} films annealed at different T_A values, the UPS and REELS spectra, which queried the electronic structures of both the occupied and unoccupied states, gave nearly identical energy distributions. Highly crystalline organic semiconductor films can reduce the exciton binding energy by the scale at tens meV due to the weak intermolecular van der Waals interactions.[45] For these reasons, the C_{60} films prepared at different T_A have no distinction in the band gap energies.

The UPS and REELS spectra of the annealed C_{60} film coatings on graphene were used to generate a schematic diagram of the energy bands at the C_{60}/graphene interfaces, as shown in Figures 5d–5f. As T_A increased from 50°C to 130°C, the vacuum level shift increased from 0.16 eV to 0.23 eV, whereas $\Phi_{E.B}$ decreased slightly from 0.26 eV to 0.19 eV. The changes in the vacuum level shift and $\Phi_{E.B}$ with T_A were attributed to the crystalline morphologies of the C_{60} films deposited on graphene and annealed at different T_A values.[46] These results demonstrated that carrier injection could be facilitated in OFETs by reducing the electron injection barrier from graphene to C_{60} after thermal annealing at high T_A.

The CVD-grown graphene films were used as S/D electrodes and the SiO_2 surface was modified with a PTS-SAM to enable the fabrication of solution-processed C_{60} FETs prepared using a bottom-contact geometry, as shown in Figure 6a. The device characteristics, determined by measuring the electrical properties of the OFETs, were examined in three different C_{60} FETs prepared under various T_A values to investigate the effects of thermally annealing the spin-coated C_{60} films. Figures 6b and 6c show, respectively, the transfer and output characteristics of the

OFETs. The field-effect mobility (μ) in the saturation regime (drain voltage, V_D = 80 V) was calculated from the slope of the square root drain current ($I_D^{1/2}$) versus the gate voltage (V_G) using the following equation:

$$I_D = \frac{\mu C_i W}{2L}(V_G - V_{th})^2 \quad (1)$$

where C_i is the capacitance per unit area of the gate dielectric (≈10 nF/cm^2) and V_{th} is the threshold voltage. The electrical characteristics of the OFETs are summarized in Table 1. As T_A increased, the resulting C_{60} FETs showed higher mobilities and on-state currents, demonstrating that a high C_{60} crystallinity improved the OFET performance. The C_{60} FET devices that were thermally annealed at 130°C exhibited the highest electrical performances, with an average μ of 0.055 ± 0.004 cm^2/Vs and an on/off ratio of 10^6.

The origin of these field-effect mobility variations was investigated by calculating the contact resistance of each device using the transfer-line method.[21, 47] The total width-normalized resistances ($R_{total}W$) were determined from the inverse slope of the *I-V* curve for each device (W = 1000 μm and L = 20, 50, 100, 150 μm) in the linear regime at each gate voltage (Figure S6). The $R_{total}W$ value could be expressed as

$$R_{total}W = R_C W + \frac{L}{\mu C_i (V_G - V_{th})} \quad (2)$$

where $R_C W$, μ, and V_{th} are the width-normalized contact resistance, intrinsic field-effect mobility, and threshold voltage, respectively. Therefore, RcW could be approximated based on the *y*-intercept of the linear extrapolation of the plots of $R_{total}W$ versus channel length (L) ($R_{total}W$ was obtained from the inverse slope of each I-V curve in the linear regime). Figure 6d plots the width-normalized contact resistances (RcW) of these OFETs under various gate voltages. It should be noted that the C_{60} FET devices thermally annealed at 130°C showed the

smallest contact resistances between the electrode and the active layer. These results demonstrated that highly crystalline C_{60} films formed on the graphene S/D electrodes and a small charge injection barrier in C_{60}/graphene led to a small RcW, which enhanced the OFET performance. Because thermal annealing also increased the crystallinity of C_{60} in the channel area,[15] the channel resistance may also be reduced by thermal annealing. Therefore, we believed that reductions in both the contact and channel resistances contributed the high OFET performances in C_{60}-based FETs.

4. CONCLUSIONS

In conclusion, we realized solution-processable C_{60}-based bottom-contact OFETs for the first time by using CVD-grown graphene as the S/D electrodes. C_{60} was effectively spin-coated onto graphene, which formed stabilizing π-π interactions, whereas the film was not spin-coated onto the metal electrodes. In the channel region, the phenyl group of the SAM formed π-π interactions with the C_{60} molecules, which further stabilized the C_{60} coating and enabled OFET preparation. We found that the thermally annealed C_{60} films on graphene displayed surprisingly good crystallinities and low electron injection barriers between the graphene and C_{60}, leading to effective charge injection and transport. The resulting devices exhibited field effect mobility values up to 0.055 cm^2/Vs with high on/off ratios exceeding 10^6. These results constitute significant progress toward the realization of all-organic integrated devices based on CVD-grown graphene electrodes prepared using inexpensive and simple fabrication techniques.

ASSOCIATED CONTENT

Supporting Information. Optical microscopy images of the aggregated C_{60} on aluminum electrodes, 2D-GIXD patterns of the C_{60} films deposited onto graphene and thermally annealed at three different T_A values (50, 90, or 130°C), and width-normalized total resistance (R_{total} W) values obtained from the C_{60} FETs annealed at three different T_A values as a function of the gate voltages are provided in the Supporting Information. This material is available free of charge via the Internet at http://pubs.acs.org.

Author Information

Corresponding Author

*E-mail: cep@postech.ac.kr, Fax: +82-54-279-8298, Tel: +82-54-279-2269 (C. E. Park)

*E-mail: shkim97@yu.ac.kr (S. H. Kim)

Acknowledgements

This work was supported by a grant from the National Research Foundation of Korea (NRF), funded by the Korean Government (MSIP) (2014R1A2A1A05004993). The authors thank the Pohang Accelerator Laboratory for providing access to the 5A and 3C beamlines used in this study.

FIGURES

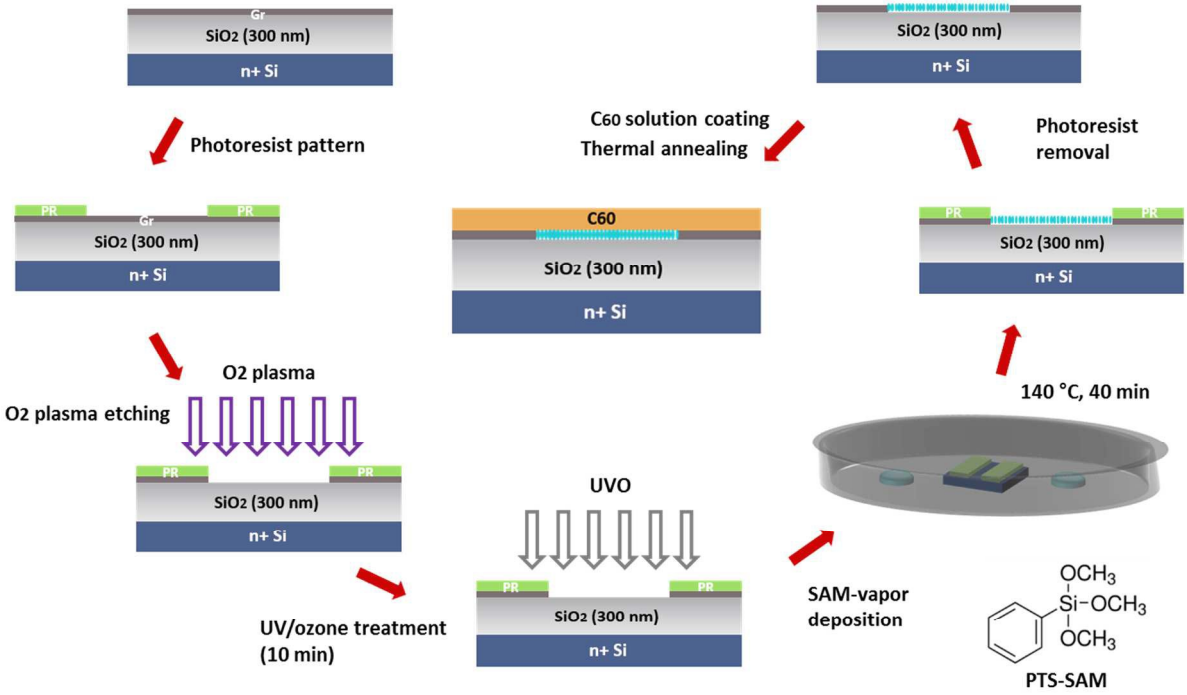


Figure 1. (a) Schematic illustration of the experimental procedure and sample structure used in this study. The lower right inset shows the chemical structures of phenyltrimethoxysilane (PTS).

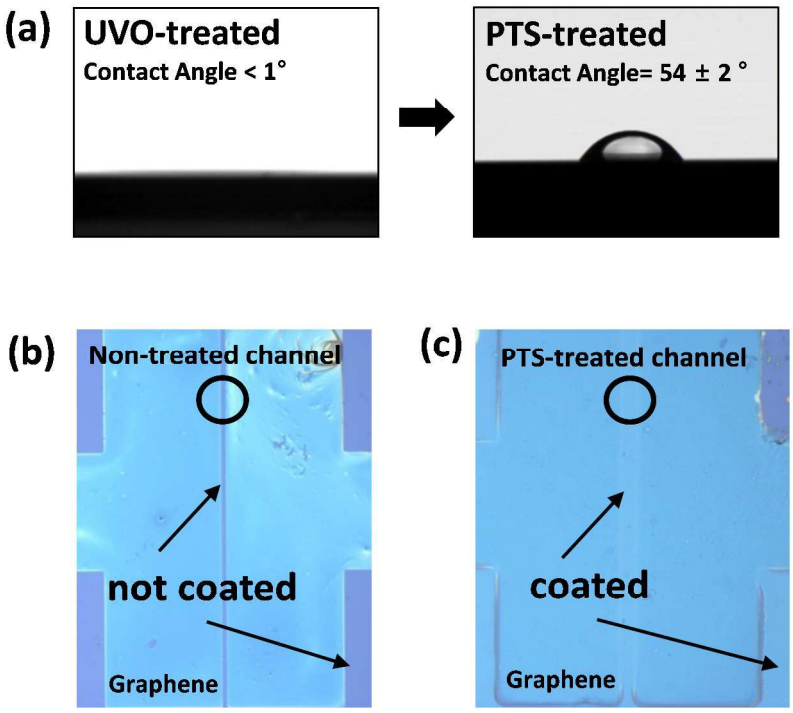


Figure 2. (a) Optical images of the seeding water droplet on the UVO- and PTS-treated SiO_2/Si substrates. Optical microscopy images of the C_{60} thin film coatings deposited onto the patterned graphene electrodes, with an untreated channel (b), or with a PTS-treated channel (c).

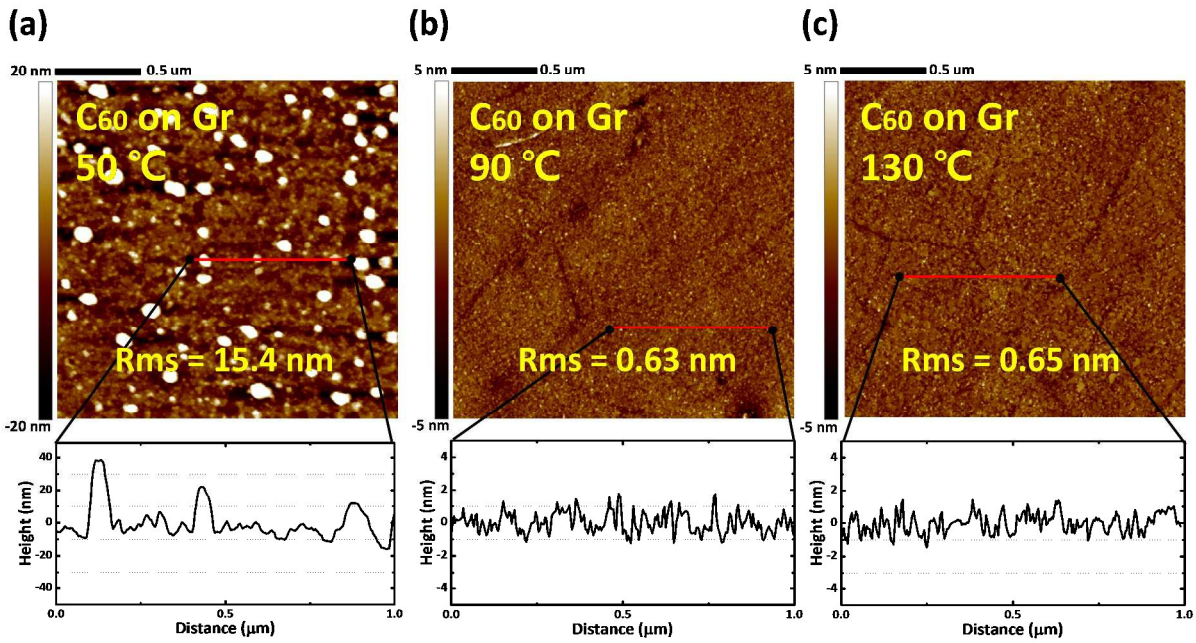


Figure 3. AFM topography images of thermally annealed C_{60} films deposited onto a graphene electrode at (a) 50°C, (b) 90°C, or (c) 130°C. The bottom graphs display the corresponding AFM cross-sectional height profiles of the C_{60} films.

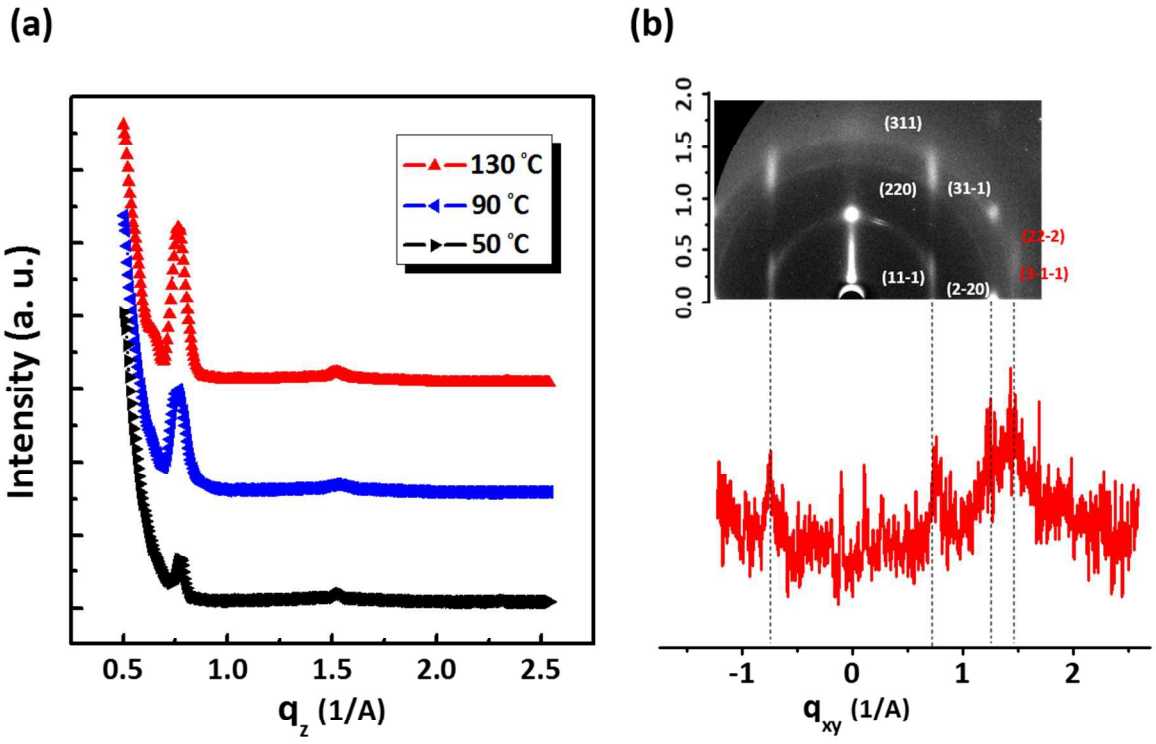
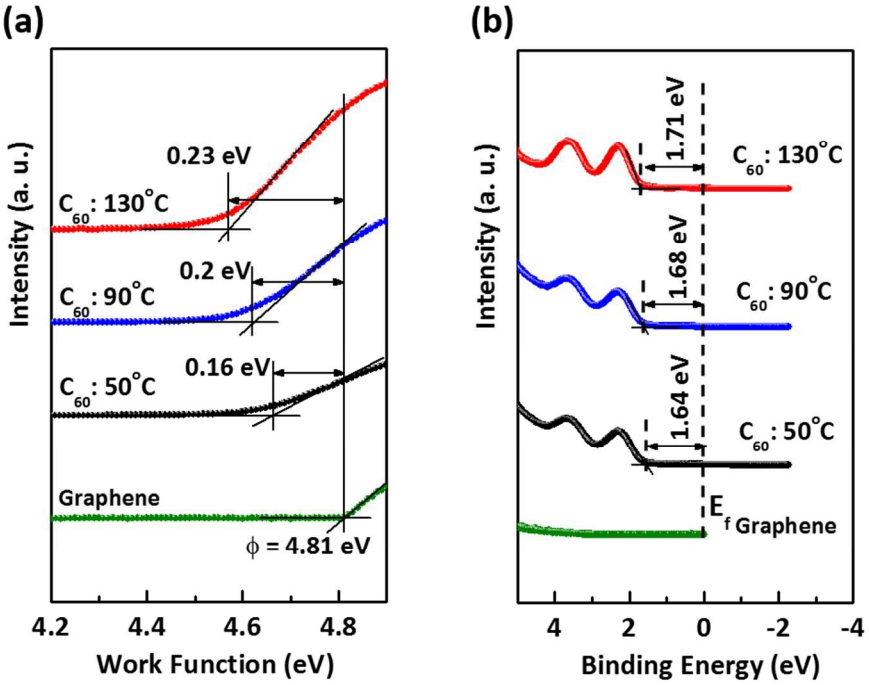
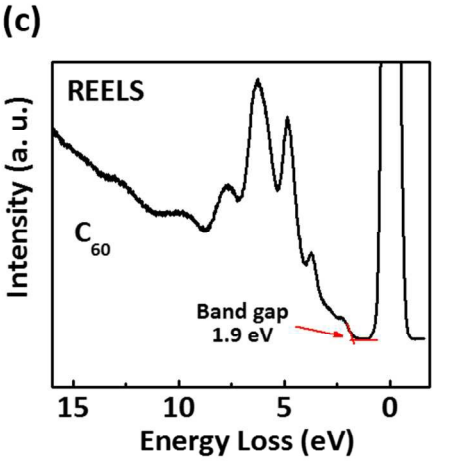
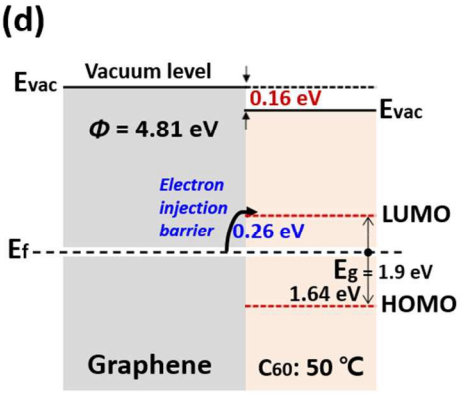
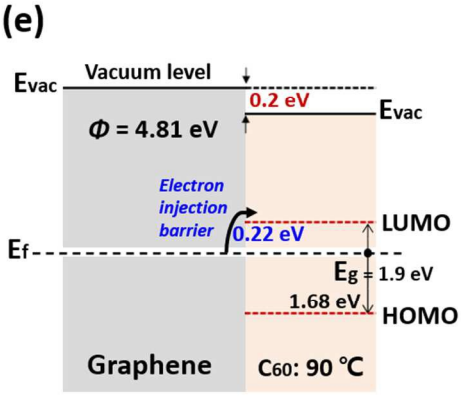


Figure 4. (a) *Θ-2Θ* mode out-of-plane XRD profiles of thermally annealed C_{60} films deposited onto graphene electrodes at different T_A (λ=1.07 Å). (b) 2D-GIXD patterns of the C_{60} films deposited onto graphene and thermally annealed at 130°C, indexed according to the C_{60} *fcc* phase structure. The bottom graph displays the corresponding in-plane profiles extracted from the 2D-GIXD pattern obtained from a C_{60} film.









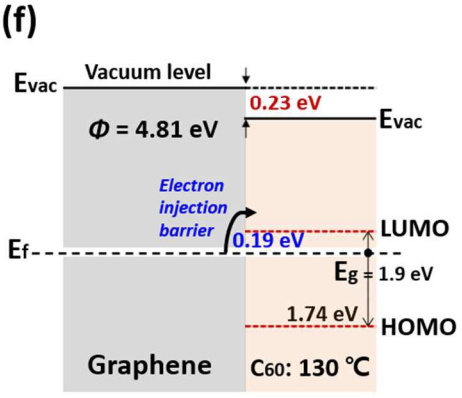


Figure 5. Comparative UPS spectra showing the secondary cutoff region (a) and valence regions (b) of C_{60}/graphene films annealed at different T_A (50, 90, or 130°C). (c) REELS spectrum of a C_{60}/graphene film. Schematic energy diagram of the C_{60}/graphene film interface after annealing at (d) 50°C, (e) 90°C, or (f) 130°C, including the work function of the graphene films, the HOMO and the LUMO levels, the electron injection barriers, and the vacuum level shift. The electron injection barriers between graphene and the thermally annealed C_{60} films were calculated from the UPS and REELS spectra.

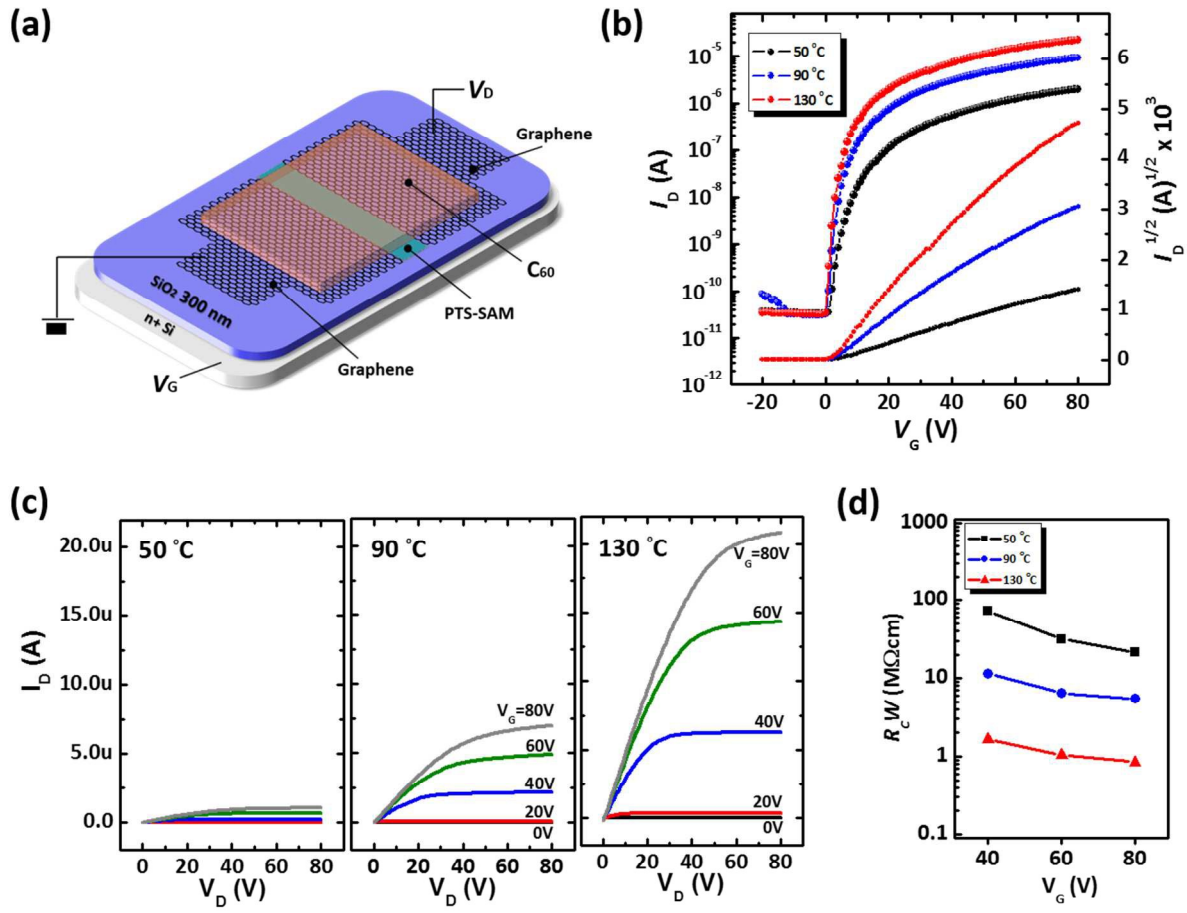


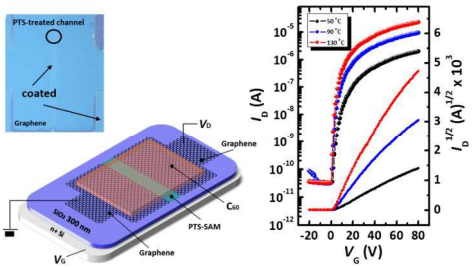
Figure 6. (a) Schematic illustration of a bottom-contact C_{60} FET prepared using graphene S/D electrodes in this study. (b) Transfer characteristics in the saturation regime (V_D = 80 V), and (c) output characteristics of three types of C_{60} FETs prepared using graphene S/D electrodes and thermally annealed at various T_A values (50, 90, or 130°C). The channel lengths (L) and widths (W) of the OFETs were 100 and 1000 μm, respectively. (d) The RcW values for three types of C_{60} FETs prepared using graphene S/D electrodes, as a function of the V_G values.

TABLES.

Table I. Electrical characteristics of the C_{60} FETs prepared using graphene S/D electrodes and thermally annealed at various T_A values (50, 90, and 130°C).

T_A [°C]	μ [cm^2/Vs]	V_{th} [V]	$I_{on/off}$	SS [V/dec]
50	0.002 ± 0.001	2.93	~ 10^4	–3.45
90	0.027 ± 0.002	3.20	~ 10^5	–3.88
130	0.055 ± 0.004	2.39	~ 10^6	–3.28

Table of Contents



REFERENCES

1. H. T. Yi, M. M. Payne, J. E. Anthony and V. Podzorov, *Nature communications*, 2012, **3**, 1259.
2. Y. Diao, B. C. Tee, G. Giri, J. Xu, H. Kim do, H. A. Becerril, R. M. Stoltenberg, T. H. Lee, G. Xue, S. C. Mannsfeld and Z. Bao, *Nature materials*, 2013, **12**, 665-671.
3. M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokota, K. Kuribara, T. Tokuhara, M. Drack, R. Schwödiauer, I. Graz, S. Bauer-Gogonea, S. Bauer and T. Someya, *Nature*, 2013, **499**, 458-463.
4. T. K. An, I. Kang, H. J. Yun, H. Cha, J. Hwang, S. Park, J. Kim, Y. J. Kim, D. S. Chung, S. K. Kwon, Y. H. Kim and C. E. Park, *Adv Mater*, 2013, **25**, 7003-7009.
5. Y. J. Jeong, H. Lee, B. S. Lee, S. Park, H. T. Yudistira, C. L. Choong, J. J. Park, C. E. Park and D. Byun, *ACS applied materials & interfaces*, 2014, **6**, 10736-10743.
6. K. Ariga, Y. Yamauchi, T. Mori and J. P. Hill, *Adv Mater*, 2013, **25**, 6477-6512.
7. K. Ariga, Y. Yamauchi, G. Rydzek, Q. Ji, Y. Yonamine, K. C. W. Wu and J. P. Hill, *Chemistry Letters*, 2014, **43**, 36-68.
8. Y. Yuan, G. Giri, A. L. Ayzner, A. P. Zoombelt, S. C. Mannsfeld, J. Chen, D. Nordlund, M. F. Toney, J. Huang and Z. Bao, *Nature communications*, 2014, **5**, 3005.
9. Y. Mei, M. A. Loth, M. Payne, W. Zhang, J. Smith, C. S. Day, S. R. Parkin, M. Heeney, I. McCulloch, T. D. Anthopoulos, J. E. Anthony and O. D. Jurchescu, *Adv Mater*, 2013, **25**, 4352-4357.
10. B. Kang, M. Jang, Y. Chung, H. Kim, S. K. Kwak, J. H. Oh and K. Cho, *Nature communications*, 2014, **5**, 4752.
11. Y. Zhou, S. T. Han, Z. X. Xu and V. A. Roy, *Adv Mater*, 2012, **24**, 1247-1251.
12. R. Ahmed, A. Kadashchuk, C. Simbrunner, G. Schwabegger, M. A. Baig and H. Sitter, *ACS applied materials & interfaces*, 2014.
13. M. Chikamatsu, S. Nagamatsu, Y. Yoshida, K. Saito, K. Yase and K. Kikuchi, *Applied Physics Letters*, 2005, **87**, 203504.
14. R. D. N. Sivaraman, I. Kaliappan, and P. R. V. R. T. G. Srinivasan, and C. K. Mathewsl, *J. Org. Chem.*, 1992, **57**, 6077-6079.
15. C. F. Sung, D. Kekuda, L. F. Chu, Y. Z. Lee, F. C. Chen, M. C. Wu and C. W. Chu, *Adv Mater*, 2009, **21**, 4845-4849.
16. W. Kang, M. Kitamura, M. Kamura, S. Aomori and Y. Arakawa, *Japanese Journal of Applied Physics*, 2012, **51**, 02BK10.
17. W. Kang, M. Kitamura and Y. Arakawa, *Applied Physics Express*, 2011, **4**, 121602.
18. D. J. Yun, H. Ra, J. Kim, I. Hwang, J. Lee, S. W. Rhee and J. Chung, *ECS Journal of Solid State Science and Technology*, 2012, **1**, M10-M14.
19. D.-J. Yun, J.-M. Kim, H. Ra, S. Byun, H. Kim, G.-S. Park, S. Park and S.-W. Rhee, *Organic Electronics*, 2013, **14**, 2962-2972.
20. K. Hong, S. H. Kim, C. Yang, J. Jang, H. Cha and C. E. Park, *Applied Physics Letters*, 2010, **97**, 103304.
21. K. Hong, S. H. Kim, C. Yang, T. K. An, H. Cha, C. Park and C. E. Park, *Organic Electronics*, 2011, **12**, 516-519.
22. Y. J. Jeong, J. Jang, S. Nam, K. Kim, L. H. Kim, S. Park, T. K. An and C. E. Park, *ACS applied materials & interfaces*, 2014, **6**, 6816-6824.

23. K. Hong, S. H. Kim, C. Yang, W. M. Yun, S. Nam, J. Jang, C. Park and C. E. Park, *ACS applied materials & interfaces*, 2011, **3**, 74-79.
24. S. Lee, S.-J. Kang, G. Jo, M. Choe, W. Park, J. Yoon, T. Kwon, Y. Ho Kahng, D.-Y. Kim, B. Hun Lee and T. Lee, *Applied Physics Letters*, 2011, **99**, 083306.
25. S. Lee, G. Jo, S. J. Kang, G. Wang, M. Choe, W. Park, D. Y. Kim, Y. H. Kahng and T. Lee, *Adv Mater*, 2011, **23**, 100-105.
26. W. H. Lee, J. Park, S. H. Sim, S. Lim, K. S. Kim, B. H. Hong and K. Cho, *J Am Chem Soc*, 2011, **133**, 4447-4454.
27. J. Cho, J. Smerdon, L. Gao, O. Suzer, J. R. Guest and N. P. Guisinger, *Nano letters*, 2012, **12**, 3018-3024.
28. J. Jang, J. Park, S. Nam, J. E. Anthony, Y. Kim, K. S. Kim, K. S. Kim, B. H. Hong and C. E. Park, *Nanoscale*, 2013, **5**, 11094-11101.
29. K. Hong, S. Y. Yang, C. Yang, S. H. Kim, D. Choi and C. E. Park, *Organic Electronics*, 2008, **9**, 864-868.
30. F. Amy, C. Chan and A. Kahn, *Organic Electronics*, 2005, **6**, 85-91.
31. T. Minari, M. Kano, T. Miyadera, S.-D. Wang, Y. Aoyagi, M. Seto, T. Nemoto, S. Isoda and K. Tsukagoshi, *Applied Physics Letters*, 2008, **92**, 173301.
32. X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, *Science*, 2009, **324**, 1312-1314.
33. K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J. H. Ahn, P. Kim, J. Y. Choi and B. H. Hong, *Nature*, 2009, **457**, 706-710.
34. W. Wu, Q. Yu, P. Peng, Z. Liu, J. Bao and S. S. Pei, *Nanotechnology*, 2012, **23**, 035603.
35. J. Moineau, M. Granier and G. F. Lanneau, *Langmuir*, 2004, **20**, 3202-3207.
36. C. Huang, H. E. Katz and J. E. West, *Langmuir*, 2007, **23**, 13223-13231.
37. D. Janssen, R. De Palma, S. Verlaak, P. Heremans and W. Dehaen, *Thin Solid Films*, 2006, **515**, 1433-1438.
38. H. Klauk, *Chemical Society reviews*, 2010, **39**, 2643-2666.
39. F. Li, *ACS applied materials & interfaces*, 2013, **5**, 8099-8104.
40. A. Hinderhofer, A. Gerlach, K. Broch, T. Hosokai, K. Yonezawa, K. Kato, S. Kera, N. Ueno and F. Schreiber, *The Journal of Physical Chemistry C*, 2013, **117**, 1053-1058.
41. J. L. de Boer, S. van Smaalen, V. Petricek, M. DusekP, M. A. Verheijen and G. Meijer, *Chemical Physics Letters*, 1994, **219**, 469-472.
42. S. J. Noever, S. Fischer and B. Nickel, *Adv Mater*, 2013, **25**, 2147-2151.
43. H. Jin, S. K. Oh, H. J. Kang and M. H. Cho, *Applied Physics Letters*, 2006, **89**, 122901.
44. R. F. Egerton, *Reports on Progress in Physics*, 2009, **72**, 016502.
45. P. K. Nayak, *Synthetic Metals*, 2013, **174**, 42-45.
46. D. J. Yun, J. Chung, C. Jung, H. S. Han, J. Lee, B. Anass, S. Lee, Y. Kyung and S. H. Park, *Journal of the Electrochemical Society*, 2013, **160**, H436-H442.
47. D. B. Gamota, P.; Kalyanasundaram, K.; Zhang, J., *Printed Organic and Molecular Electronics*, Kluwer Academic Publishers, 2004.