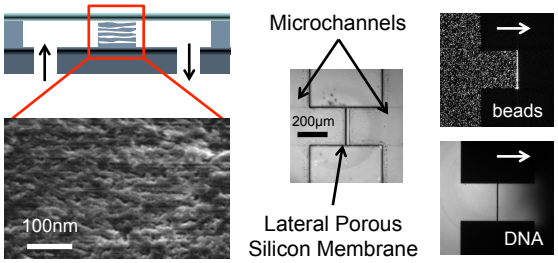
Lab on a Chip

Accepted Manuscript

ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/loc

Graphical and Textual Abstract for the Contents Page:



A unique fabrication process was developed to integrate lateral porous silicon membranes into planar microfluidic channels. These mesoporous membranes were demonstrated to be suitable for on-chip dead-end microfiltration.

Lab on a Chip

RSCPublishing

PAPER

Integration of lateral porous silicon membranes into planar microfluidics

Cite this: DOI: 10.1039/xoxxoooooox

Thierry Leichlé*[ab] and David Bourrier[ab]

Received ooth January 2012,
Accepted ooth January 2012

DOI: 10.1039/xoxxoooooox

www.rsc.org/

In this work, we present a novel fabrication process that enables the monolithic integration of lateral porous silicon membranes into single-layer planar microchannels. This fabrication technique relies on the patterning of local electrodes to guide pore formation horizontally within the membrane, and on the use of silicon-on-insulator substrates to spatially localize porous silicon within the channel depth. The feasibility of our approach is studied by current flow analysis using finite element method and supported by creating 10 µm long mesoporous membranes within 20 µm deep microchannels. The fabricated membranes are demonstrated to be potentially useful for dead-end microfiltration by adequately retaining 300 nm diameter beads while macromolecules such as single-stranded DNA and immunoglobulin G permeate the membrane. The experimentally determined fluidic resistance is in accordance with the theoretical value expected from the estimated pore size and porosity. The work presented here is expected to greatly simplify the integration of membranes capable of size-exclusion based separation into fluidic devices and opens doors to the use of porous silicon in planar lab on a chip devices.

Introduction

Lab on a chip devices aim at integrating functions routinely used in medical laboratories into miniaturized chips to target health care applications with a promising impact foreseen in point-of-care testing.[1] Among these fundamental operations, sample preparation, which is to be performed prior to sample analysis, involves many steps to result in a purified sample. While several techniques have been recently developed to carry out this task on-chip,[2,3] the use of porous membranes is an evident choice given their long history in separation science.

Lately, there has been a growing interest in integrating porous membranes into microfluidics for various purposes especially some related to sample pre-treatment, *e.g.* sample filtration[4-6] and sample concentration.[7-9] As a result, there are now many methods and materials available to create membranes from porous elements and integrate them onto chips.[10] The various strategies that have been developed for membrane integration include the direct incorporation of membranes into channels during chip assembly,[11,12] the in-situ fabrication of membranes within already existing enclosed channels,[13,14] the realization of membranes during the chip fabrication process,[15,16] and the direct use of membrane properties of the bulk-chip material.[17,18] In addition to the diversity in integration methods, the range of materials constituting membranes is wide, spanning from polymers, hydrogels, to ceramics and silicon.

Among the materials used as membrane constituents, porous silicon is of special interest because of the specific advantages it offers in addition to the obvious size exclusion-based filtering capability. Indeed, charge effects contribute to the ion selectivity property of nanoporous silicon,[19] and selective mass-transport of reagents can be achieved by tuning the surface chemistry of the membrane pores.[20] Moreover, if properly functionalized with biological probes, porous silicon can serve as a biosensing layer due its unique optical properties,[21,22] thus allowing sample preparation and analysis to be carried out by a single element.[23] However, in dead-end configuration (*vs.* cross-flow), integration of porous silicon membranes is currently achieved by sandwiching the membrane between two micromachined layers bearing fluidic channels (Fig. 1a), because silicon pores are created through the substrate.[24] This results in three-dimensional (3D) fluidic networks that lack the simplicity of operation and direct observation accessibility of planar microfluidic devices. Besides, these hybrid processes do not offer design flexibility and clearly limit membrane integration into lab on a chip.

To tackle this constraint, we propose a fabrication method enabling the monolithic integration of porous silicon membranes into planar, two-dimensional (2D) microfluidics. Feasibility of our approach relies on pores created parallel to the substrate surface so that they run laterally within the membrane and bridge microchannels lying in the same plane, as depicted in Fig. 1b. Pores are grown in a lateral fashion by controlling the position of the current source and the direction of the current flow during silicon anodization, in a configuration similar to the one reported for the fabrication of lateral porous alumina membranes.[25,26] Technically, in our case, this is achieved by injecting charges through electrodes that are

locally patterned within microchannels etched into the top layer of a silicon-on-insulator (SOI) wafer. Our proposed fabrication process was used to create 10 µm long mesoporous membranes within 20 µm deep microchannels. We show preliminary experiments demonstrating the capability of the porous membrane to remove unwanted components from a solution in a dead-end filter configuration. The permeation of small molecules and the retention of polymer microspheres mimicking larger biological species are in accordance with the measured average pore size of the fabricated membranes.

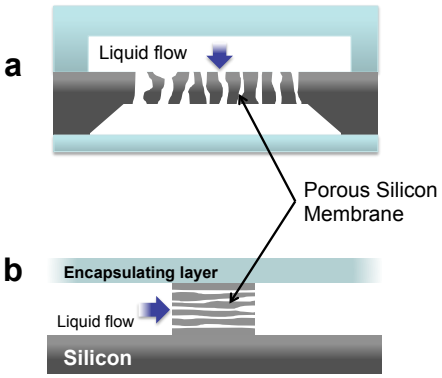


Fig. 1 Schematics showing the difference between (a) transverse and (b) lateral porous membranes integrated into 3D and 2D fluidic systems, respectively.

Concept – Finite Element Simulation

The most common method used to fabricate porous silicon is the electrochemical anodization of a silicon substrate in a hydrogen fluoride (HF) electrolyte. The mechanism leading to the dissolution of silicon and the formation of pores relies on the local oxidation of silicon due to the injected current (holes) that is subsequently etched in HF.[27] The propagation of pores is dictated by various mechanisms, but always follows the electrical current lines.

In a classical etch cell set up, the current is injected via the backside of (*i.e.* through) a silicon wafer so that the current flows in a direction perpendicular to the silicon surface, leading to the formation of vertical pores (with respect to the surface of the wafer). However, for porous silicon membranes to be used as dead-end filters into planar microfluidics, pores have to be horizontally distributed in the membrane in order to connect inlet and outlet microchannels. In order to do so, our approach relies on the use of electrodes patterned on one of the sidewalls of a step bridging two microchannels in order to inject the current on one side of that step while the electrochemical reaction occurs on the other sidewall. This configuration leads to the current flowing horizontally to the silicon surface through the step so that the pores propagate in a lateral fashion until the step is fully converted into a porous membrane.

In order to investigate the feasibility of our approach, we have first studied the orientation of the current flowing within silicon by means of finite element analysis (FEA, COMSOL Multiphysics 4.0a) in two etching configurations. The electrochemical cell was simplified to a 2D model and the Electric Currents physics interface was used to compute electrical currents and potentials. The steady-state solutions were obtained for a 1V potential difference applied between the electrodes located on the silicon and in the electrolyte, and for electrical conductivity and relative permittivity values found in the literature[28] and in the COMSOL material library (Si: $\sigma = 10^5$ S/m, ε_r = 12.1; Electrolyte: σ = 10^4 S/m, ε_r = 80.1). Fig. 2 presents simulation results, displaying the current flow (white arrows) and potential (color scale) within the bulk silicon and the electrolyte in the case of classically fabricated vertical pores (Fig. 2a, upon current injection at the bottom of the silicon substrate) and in the case of pore formation within the membrane (Fig. 2b, upon current injection within the sidewall electrode). As expected, while the current flows vertically in the former case, leading to the formation of classically reported vertical pores, the use of local electrodes patterned onto the membrane wall forces the current to flow through the silicon membrane. From the simulation results of Fig. 2b, we can point out that in order to confine the current flow lines to the step/membrane, it has to be electrically isolated from the silicon substrate. In this case, the electrode patterned at the surface of the silicon wafer does not inject any charges into the substrate. Thus, our proposed method relies on using electrodes patterned onto the membrane in combination with the use of silicon-on-insulator substrates. This method should lead to pore propagation solely into the membrane in a lateral fashion while preventing pore propagation in the substrate, hence resulting in a confined porous membrane within the channel.

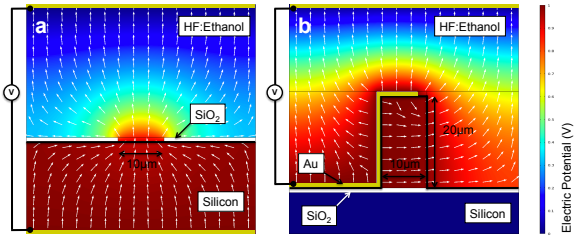


Fig. 2 Finite element analysis 2D models of the fabrication of porous silicon via: (a) the classical approach, where current injected at the backside of the silicon wafer flows in perpendicular to the surface of the substrate and thus leads to the formation of vertical pores; (b) the proposed approach, where current injected via a locally patterned electrode through a step formed within the top layer of a silicon-on-insulator wafer flows horizontally and thus leads to the formation of lateral pores. The white arrows represent the direction of current flow and the color scale indicates the local potential.

Device fabrication

To demonstrate the feasibility of our approach, microfluidic chips with integrated lateral porous silicon membranes were fabricated following the process shown in Fig. 3. The key steps of this process are first the fabrication of a solid membrane bridging two etched microchannels and secondly, in a single step, the protection of the silicon surface except that of the membrane sidewall where pores are to be created and the patterning of an electrode to provide charges on the opposite membrane sidewall.

Confinement of the porous membrane within the microchannel depth was achieved using a silicon-on-insulator wafer as a starting substrate (P-type, d = 100 mm, t = 20/2/450 µm, ρ = 0.01-0.02/0.015 Ω.cm, Shin-Etsu). The dopant type and concentration of the top silicon layer were selected to allow mesoporous silicon formation upon anodization of the

membrane without the use of external illumination. The large thickness of that top silicon layer was desired for channels to be deep enough to permit the generation of reasonable volumetric flow rates by means of a conventional pressure source routinely used in microfluidics (*i.e.* providing a 1 bar maximum applied pressure).

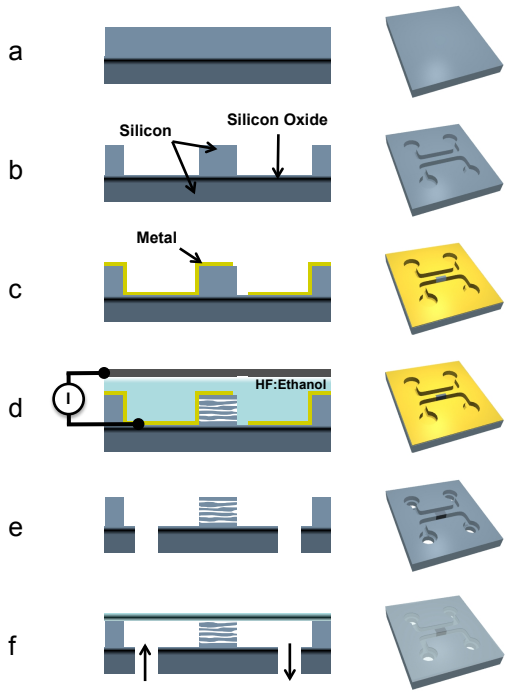


Fig. 3 Fabrication process of fluidic chip with an integrated lateral porous silicon membrane (Left: section view; Right: three-dimensional representation). (a) The starting substrate consists of a SOI wafer. (b) Dry etching of top the silicon layer down to the buried oxide is used to create microchannels. (c) A metal layer, used as the working electrode, is deposited in a conformal way and etched where anodization of silicon is to be initiated. (d) Silicon anodization is carried out in a HF:ethanol bath. (e) Fluidc inlets and outlets are realized by means of sandblasting. (f) The channels are sealed by anodic bonding.

The process started by deep reactive ion etching the inlet and outlet microchannels using the buried oxide as an etch stop layer (Fig. 3b). Integration of the lateral porous silicon membrane was then carried out by anodizing a portion of the bulk silicon lying in between the two channels. For this purpose, an electrode was created by first sputtering 100 nm/500 nm Cr/Au layers in a conformal way to ensure the presence of metal on the sidewalls of the bulk silicon part to permeate. After proper annealing (250 °C, 20 min), the metal was then patterned by means of photolithography using a thick photoresist (AZ 40XT), followed by wet etching in appropriate baths in order to access the opposite silicon membrane sidewall, where pore formation was to be initiated (Fig. 3c): this metal layer was not only used as an electrode to bring charges within the doped silicon for anodization but it also acted as a protective layer for the remaining area where porous silicon was undesired. Finally, the formation of pores within the membranes was achieved by anodic dissolution of silicon in a 1:1 ethanol:48% aqueous HF solution for 2 min at a current density of 200 mA/cm^2 (Fig. 3d). The electric current was injected to the patterned electrodes (used as the anode) on the front side of the wafer, while the cathode consisted of a platinum disk immersed in the solution and facing the wafer in the electrolyte bath. It is important to note here that since silicon oxide was etched by the electrolyte, the anodization time could not exceed the time it takes to fully etch the buried layer because of possible device failure. This restriction thus limited the maximum thickness of the porous membrane. Following the anodization step, both Cr/Au metal layers were removed in wet etch baths. In order to create fluidic inlet/outlets and connect the fluidic chip to reservoirs, holes were drilled through the silicon wafer by sandblasting (Fig. 3e). The channels were then encapsulated by anodic bonding the silicon chips bearing the fluidic channels to a 150 µm thick transparent borofloat 33 wafer (Schott) at 370 °C, 5×10^{-5} mBar, 600 V for 10 min. Finally, individual chips were obtained by dicing the borofloat substrate.

A typical 1.6 cm×1.6 cm fabricated chip is shown in Fig. 4a. The microfluidics chip bears two 20 µm deep microchannels, each having two inlet/outlet holes, that are separated by a 10 µm thick porous silicon membrane (Fig. 4b). Fig. 4c and 4d display cross-section SEM images of the fabricated mesoporous membrane. The formation of pores is initiated on one side of the membrane sidewall and they propagate through the membrane by following the current density lines until they reach the electrode placed on the opposite sidewall, *i.e.* where holes are injected. Thus, as expected, silicon anodization results in the creation of a membrane displaying horizontal/lateral pores bridging the two microchannels.

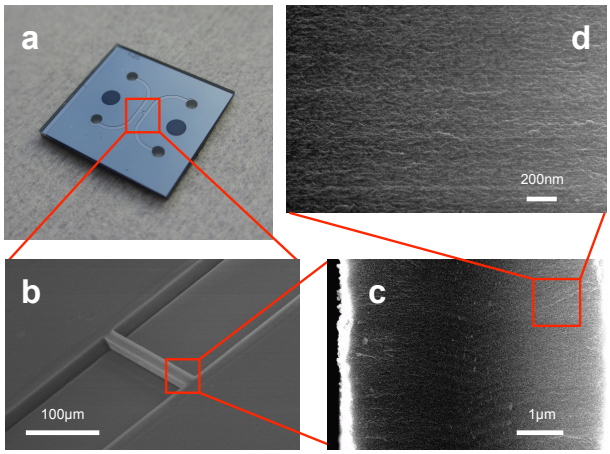


Fig. 4 (a) Optical photograph of a fabricated fluidic chip integrating a lateral porous silicon membrane. (b) SEM picture of the lateral porous silicon membrane bridging two fluidic microchannels. (c), (d) SEM section views of the fabricated membrane. The membrane is 20 µm thick and 10 µm long.

Filtering experiments

Experiments were carried out to demonstrate that the fabricated pores are open-ended pipes that adequately connect the microchannels situated on both sides of the membrane. The use of various size objects (300 nm diameter beads, 40-mers single-stranded DNA and immunoglobulin G (IgG) molecules) was used to prove the dead-end filtration capability of the porous membranes.

Initial chip loading was achieved by injecting DI (deionized) water in the fluidic inlets of the two microchannels. Then, the

test solutions were sequentially flown through the membrane by loading the left side microchannel and applying various pressures between both microchannels, *i.e.* across the membrane, by means of a pressure generator (MFCS-8C, Fluigent). All solutions were properly degased before loading. The test solutions consisted of 300 nm diameter green fluorescent polystyrene microspheres (Duke Scientific) diluted in DI water at a final concentration of 7.4×10^7 beads/mL, Cy3-lablelled 40-mer single-stranded DNA (5'-CY3-GTC TAT AAA CAA AGT CTT CCT GGA AGT AAT TGT AAG CAT C-3', Unimed Healthcare Inc.) at 1 µM in DI water, and Alexa Fluor 660 donkey anti-goat IgG (Invitrogen) diluted at 100 µg/mL in phosphate buffered saline (PBS) 1×. Fluorescence images were obtained during the experiments by means of a IX70 Olympus inverted epifluorescence microscope equipped with 10× and 20× objectives and appropriate filters (UMWIB3 from Olympus, U-M41007 and U-M41008 from Chroma), and an Andor iXon 885 EMCCD camera (with acquisition time/kinetic cycle time in the range of 0.1-0.5 s/0.5-1 s).

Fig. 5 presents sequential images recorded while flowing solutions back and forth through the membrane for the cases of the three different dissolved species. First, loaded 300 nm diameter microspheres did quickly accumulate at the microchannel/membrane interface when positive pressure was applied between the left-hand side and the right-hand side microchannels filled with bead solution and DI water, respectively (Fig. 5b). Reversing the pressure resulted in the majority of beads flowing outward the membrane surface into the left microchannel, while few beads remained stuck to the membrane surface due to non-specific adsorption. Observation of this pressure-driven flow indicated that the pores were open-ended pipes. After loading the left microchannel with the 40-mer single-stranded DNA sample (Fig. 5c), a rise of fluorescence level was observed in the right-hand side of the membrane upon pressure increase, thus demonstrating that DNA strands flowed through the membrane. This situation was reversible since applying the positive pressure on the right-hand side channel led to a florescence decrease in both microchannels, showing that the DNA molecules could flow backwards into the feeding channel. Fig. 5d illustrates that the exact same behavior was obtained when flowing IgG molecules in the porous silicon chip.

The outcome of these experiments is that full retention is achieved for 300 nm size beads, while small molecules permeate the porous membrane. It can be concluded that size exclusion based separation can be accomplished with the presented fluidic chip integrating a lateral porous silicon membrane. The experimental results indicate that the cut-off size of the fabricated membrane is larger than ~10 nm (40-mer single-stranded DNA display a 4 nm minimum radius of gyration,[29] and IgG molecules have a 5.29 nm hydrodynamic radius[30]), but much smaller that the 300 nm diameter of the beads. This range is consistent with the ~25 nm average pore size of the fabricated membrane estimated from the SEM picture shown in Fig. 6.

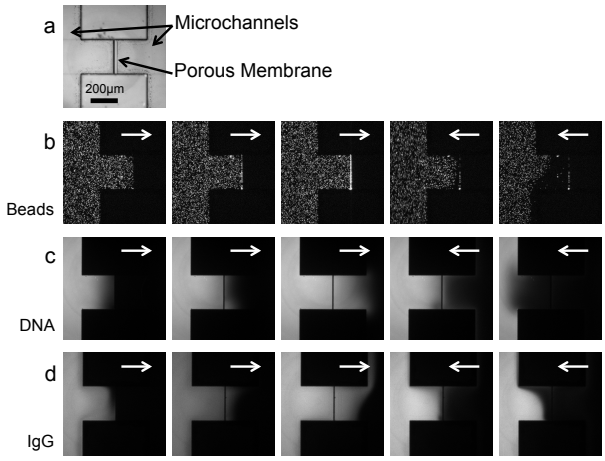


Fig. 5 Filtering capability of the fabricated membrane tested by flowing fluorescent beads and macromolecules. (a) Bright field optical picture of the microchannels with integrated membrane. (b) Test flow of 300 nm beads retained by the membrane. (c), (d) 40-mer single-stranded DNA and IgG molecules flowing back and forth through the membrane. The pictures are presented sequentially from left to right and the white arrows indicate the direction of the fluid flow that is inverted during the experiment.

Measurement of the hydrodynamic resistance

Finally, the hydrodynamic resistance of the fabricated membrane, which is an essential characteristic used in the design consideration of fluidic and lab on a chip devices, was experimentally estimated. To this aim, the pressure-driven flow velocity induced in the microchannels was measured by manually tracking the position of 300 nm fluorescein polymer microspheres for applied pressures ranging from 0.1 bar to 1 bar.

In brief, following the experimental protocol described in the previous section, where beads were introduced into the left side microchannel, a constant pressure was generated at the inputs of the right hand side microchannel causing the particles to flow inward the left microchannel. This was conducted after ensuring that pressure was equilibrated between the various inlets/outlets (*i.e.* upon observation of a net null flow velocity with beads only experiencing Brownian motion). The particle velocity was measured in the straight channel and in the vicinity of the membrane by averaging the displacement of 5 nanobeads over time, where each particle position (pixel location) was directly extracted from the recorded images using ImageJ. To ensure that the measurements reflect the maximum flow velocity as adequately as possible, care was taken to position the focus plane in the middle of the channel depth and only beads in focus were tracked. Finally, giving the fact that particle velocity increases with applied pressure, measurements were carried out over 3 s at 1 bar applied pressure and up to 25 s at 100 mbar (respectively corresponding to the analysis of 7 and 51 acquired frames). The resulting increase of measured velocity with applied pressure is in shown in Fig. 6.

The hydrodynamic resistance of a fluidic network linearly relates the fluid flow, Q, to the applied pressure ΔP. The resistance of the fabricated membrane, R_h, was thus extracted

from the linear fit of the experimental data, by neglecting the resistance contribution of the microfluidic channels. This resulted in a value of 2.9×10^{-1} Pa.s/μm^3 for the 10 μm thick porous membrane. Theoretically, the hydrodynamic resistance of an idealized membrane of cylindrical pores with the same radius can be obtained from the Hagen-Poiseuille equation, providing transport mechanisms other than laminar flow are neglected:[31]

$$R_h = \frac{\Delta P}{Q} = \frac{8\eta l}{r_p{}^2 wh\phi} \quad (1)$$

where, η is the fluid dynamic viscosity, l, w, h, and ϕ are the membrane length (i.e. thickness), width, height and porosity, respectively and r_p is the pore radius. Neglecting the tortuosity of the pores and using the geometrical values for the fabricated membranes (where ~25 nm pore diameter and ~50 % porosity were estimated from the SEM images shown in the inset of Fig. 6), leads to a theoretical hydrodynamic resistance of 2×10^{-1} Pa.s/μm^3. This value, which is more than 6 orders of magnitude higher than the resistance of a similar size microchannel without integrated membrane, is in accordance with the value obtained from flow velocity measurements and thus demonstrates that injected fluid indeed flows through the fabricated porous layer across the entire section of the microchannel.

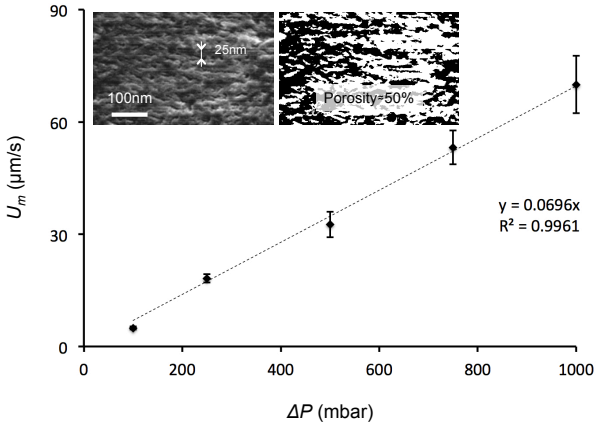


Fig. 6 Graph showing the measured flow velocity as a function of the pressure applied across a membrane. From the linear relationship, we can deduce the hydrodynamic resistance of the membrane. The two insets show SEM pictures of the porous membrane used to estimate the mean pore size and the layer porosity (the right inset shows a binary image after threshold conversion of the left inset image).

Conclusions

We have demonstrated the integration of lateral porous silicon membranes into planar microfluidic channels using a specifically dedicated fabrication process. The key ideas of this process are to guide pore formation horizontally during anodization by means of electrodes patterned onto the silicon surface and to spatially localize porous silicon growth within a controlled depth through the use of silicon-on-insulator substrates. To demonstrate the feasibility of our approach, 10 μm thick mesoporous membranes with ~25 nm diameter pores bridging 20 μm deep microchannels were prepared as part of the chip fabrication process. Preliminary experiments have shown that while 300 nm diameter polymer microspheres are retained from flowing through the membrane, macromolecules such as 40-mer single-stranded DNA and IgG do permeate, thus illustrating the potential of lateral porous membranes for dead-end filtration. While obvious applications include on-chip sample preparation through size-based separation, such membranes could also be used for other purposes, *e.g.* sample concentration. The method presented here constitutes a new technical solution for the integration of membranes into planar single-layer microfluidic devices with the advantages inherent to the use of porous silicon.

Acknowledgements

This work was partly supported by the French RENATECH network.

Notes and references

[a] CNRS, LAAS, 7 avenue du colonel Roche, F-31400 Toulouse, France.
[b] Univ de Toulouse, LAAS, F-31400 Toulouse, France.

1 P. Yager, T. Edwards, E. Fu, K. Helton, K. Nelson, M.R. Tam and B.H. Weigl, *Nature*, 2006, **442**, 412-418.
2 J. Lichtenberg, N. F. de Rooij and E. Verpoorte, *Talanta*, 2002, **56(2)**, 233–266.
3 J. Kim, M. Johnson, P. Hill and B.K. Gale, *Integr. Biol.*, 2009, **1**, 574-586.
4 J. E. Kim, J. H. Cho and S. H. Paek, *Anal. Chem.*, 2005, **77(24)**, 7901–7907.
5 C. C. Striemer, T. R. Gaborski, J. L. McGrath and P. M. Fauchet, *Nature*, 2007, **445**, 749-753.
6 H. Wei, B. H. Chueh, H. Wu, E. W. Hall, C. W. Li, R. Schirhagl, J. M. Lin and R. N. Zare, *Lab Chip*, 2011, **11**, 238-245.
7 R. S. Foote, J. Khandurina, S. C. Jacobson and J. M. Ramsey, *Anal. Chem.*, 2005, **77**, 57–63.
8 R. T. Kelly, Y. Li and A. T. Woolley, *Anal. Chem.*, 2006, **78(8)**, 2565–2570.
9 J. H. Lee, Y. A. Song and J. Han, *Lab Chip*, 2008, **8**, 596-601.
10 J. de Jong, R. G. H. Lammertink and M. Wessling, *Lab Chip*, 2006, **6**, 1125-1139.
11 B. -H. Chueh, D. Huh, C. R. Kyrtsos, T. Houssin, N. Futai and S. Takayama, *Anal. Chem.*, 2007, **79**, 3504-3508.
12 J. Ou, T. Glawdel, R. Samy, S. Wang, Z. Liu, C. L. Ren and J. Pawliszyn, *Anal. Chem.*, 2008, **80**, 7401-7407.
13 J. Moorthy and D. J. Beebe, *Lab Chip*, 2003, **3(2)**, 62-6.
14 S. Song, A. K. Singh and B. J. Kirby, *Anal. Chem.*, 2004, **76**, 4589–4592.
15 R. W. Tjerkstra, J. G. E. Gardeniers, J. J. Kelly and A. Van den Berg, *J. Microelectromech. Syst.*, 2000, **9(4)**, 495–501.
16 L. J. Heyderman, B. Ketterer, D. Bachle, F. Glaus, B. Haas, H. Schift, K. Vogelsang, J. Gobrecht, L. Tiefenauer and O. Dubochet, *Microelectron. Eng.*, 2003, **208**, 67–68.
17 E. Leclerc, Y. Sakai and T. Fujii, *Biomed. Microdevices*, 2003, **5(2)**, 109–114.
18 J. Leng, B. Lonetti, P. Tabeling, M. Joanicot and A. Ajdari, *Phys. Rev. Lett.*, 2006, **96(8)**, 084503.

19 R. Ishimatsu, J. Kim, P. Jing, C. C. Striemer, D. Z. Fang, P. M. Fauchet, J. L. McGrath, and S. Amemiya, *Anal. Chem.*, 2010, **82**, 7127-7134.
20 L. Velleman, C. J. Shearer, A. V. Ellis, D. Losic, N. H. Voelcker and J.G. Shapter, *Nanoscale*, 2010, **2**, 1756-1761.
21 V. S. -Y. Lin, K. Motesharei, K. S. Dancil, M. J. Sailor and M. R. Ghadiri, *Science*, 1997, **278**, 840-843.
22 C. Pacholski, M. Sartor, M. J. Sailor, F. Cunin and G. M. Miskelly, *J. Am. Chem. Soc.*, 2005, **127**, 11636-11645.
23 L. M. Bonanno and L. A. DeLouise, *Biosens. Bioelectron.*, 2007, **23**, 444-448.
24 K. Grigoras, S. Franssila, T. Sikanen, T. Kotiaho, and R. Kostiainen, *Phys. Status Solidi a*, 2005, **202(8)**, 1624-1628.
25 C. S. Cojocaru, J. M. Padovani, T. Wade, C. Mandoli, G. Jaskierowicz, J. E. Wegrowe, A. Fontcuberta I Morral and D. Pribat *Nano Lett.*, 2005, **5(4)**, 675-680.
26 M. Gowtham, L. Eude, C. S. Cojocaru, B. Marquardt, H. J. Jeong, P. Legagneux, K. K. Song and D. Pribat, *Nanotechnology*, 2008, **19**, 035303.
27 M. J. Sailor, in *Porous silicon in practice*, WILEY-VCH, 2012.
28 A. Ivanov, Proceedings of the 2011 COMSOL Conference, Stuttgart, 2011.
29 A. Y. Sim, J. Lipfert, D. Herschlag and S. Doniach, *Phys. Rev. E*, 2012, **86**, 021901.
30 J. K. Armstrong, R. B. Wenby, H. J. Meiselman and T. C. Fisher, *Biophys. J.*, 2004, **87**, 4259-4270.
31 A. Kovacs and U. Mescheder, *Sensor Actuat. B-Chem*, 2012, **175**, 179-185.