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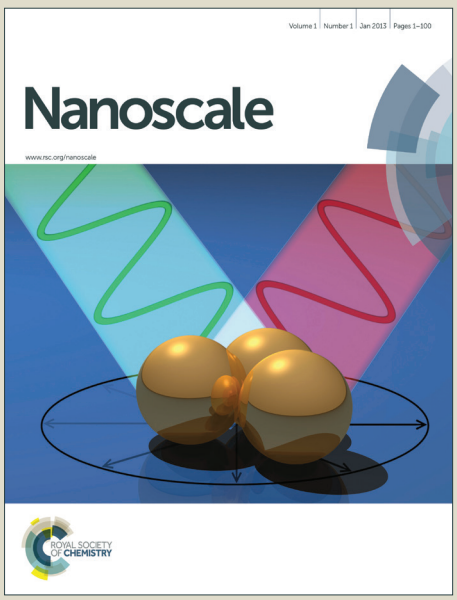

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Graphene Nano-floating Gate Transistor Memory on Plastic

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Abstrat A transparent flexible graphene nano-floating gate transistor memory (NFGTM) device was developed by combining a single-layer graphene active channel with gold nanoparticle (AuNP) charge trap elements. We systematically controlled the sizes of the AuNPs, the thickness of the tunneling dielectric layer, and the graphene doping level. Especially, we propose that the conductance difference (i.e., memory window) between the programing and erasing operations at a specific read gate voltage can be maximized through the doping. The resulting graphene NFGTMs developed here exhibited excellent programmable memory performances compared to previously reported graphene memory devices and displayed a large memory window (12 V), fast switching speed (1 μs), robust electrical reliability (10^5 s), and good mechanical (500 cycles) and thermal stability (100 °C).

Keywords: graphene, nano-floating gate transistor memory, memory window, flexible electronics, doping

1. Introduction

Flexible organic nonvolatile memory devices have attracted tremendous attention in an effort to realize low-cost, large-area, flexible charge storage media devices[1-12]. Two-dimensional graphene materials with superlative electrical and physical properties were recently incorporated into a variety of memory architectures[3-8, 13-23]. Three types of graphene memories have been demonstrated thus far: capacitor-type memory[13-15] (flash memory based on a graphene floating gate), resistor-type memory[3-7, 23] (resistive memory based on graphene oxide (GO) or GO composites), and transistor-type memory[8, 16-22] (ferroelectric memory and charge-transfer memory). Transistor-type memory devices have several advantages over capacitor or resistor-type memory devices[24]. Transistor-type memory functions through nondestructive read-out, can be realized using a single transistor, is not subject to cross-talk between adjacent memory cells, and is architecturally compatible with complementary integrated circuits (ICs)[25-27]. These features originate from the mechanism by which transistor-type memory devices operate: the gate field and channel conductance are modulated by the stored charges either in a charge trapping or a ferroelectric layer, thereby introducing reversible shifts in the threshold voltage of the device[8, 9].

Nano-floating gate transistor memory (NFGTM) devices using gate dielectric embedded with nanometer-size metallic or semiconducting nanoparticles (NPs) are considered as a promising candidate for realizing the ultimate organic nonvolatile memories due to their high speed operation, excellent reliability, capability of multilevel programming, and chances for scale down[9, 12, 24, 28]. In these devices, the levels and sites of charge trapping can be controlled precisely by varying the nanoparticle species, sizes, and density. So far, however, NFGTMs containing graphene channels have not been reported. In addition, a range of graphene-based memory applications can be enabled by mounting graphene NFGTMs onto plastic substrates to form light-weight, flexible, and portable electronic systems[11].

In this paper, a graphene channel-based NFGTM with excellent memory performance was successfully demonstrated on a plastic substrate. Single-layer graphene and gold nanoparticles (AuNPs) were used as active channel material and charge trapping elements, respectively. The AuNPs provided an effective charge storage layer embedded at the interface between the cross-linked poly(4-vinylphenol) (*c*PVP) tunneling dielectric and an Al_2O_3 blocking dielectric. A high-*k* Al_2O_3 gate dielectric was used to achieve a memory device that operates at low voltages. Note that precise control and optimization of the Au NP size, the *c*PVP thickness, and the graphene doping maximized the conductance difference between the programmed and erased states at a read gate voltage. The resulting devices yielded excellent

programmable memory properties, i.e., a large memory window (12 V), a fast switching speed (1 μs), and robust electrical reliability (10^5 s). These devices exhibited excellent mechanical (500 cycles) and thermal stabilities (100 °C).

2. Experimental Section

A poly(ethylene naphthalate) (PEN) film with a 300 nm thick indium tin oxide (ITO) was used as a substrate. ITO and PEN were used as the gate electrode and flexible substrate, respectively. A 30 nm thick Al_2O_3 blocking dielectric was deposited onto the ITO/ PEN film by chemical vapor deposition (CVD). A thin Au layer was thermally deposited onto the channel region through a shadow mask at various thicknesses: 0.5, 1, 2, 3, and 4 nm. The system was subsequently thermally annealed at 80°C for 10 min to form AuNPs. A dimethylformamide solution including poly-4-vinylphenol (PVP, M_w = 20,000 $gmol^{-1}$) and poly(melamine-co-formaldehyde) (PMF, M_w = 511 $gmol^{-1}$) with weight ratio of 2:1 was spin-coated onto the Au NPs/Al_2O_3/ITO/PEN substrate, followed by thermal annealing for 12 h at 120 °C in a vacuum oven. The thickness of the cross-linked PVP (*c*PVP) layer was controlled by varying the concentration of the solution (0.5, 1, 2, 3, and 4 wt%).

Separately, high-quality monolayer graphene films were prepared on a Cu foil (thickness 25 μm, 99.8%) via CVD, as described previously[29-33]. The graphene patterns were defined by photolithography (AZ 5214 and AZ 500 MIF developer) and oxygen plasma etching (~ 2 s) of the graphene layers on the Cu foil. A poly(methyl methacrylate) (PMMA) supporting layer was spin-coated at 4200 rpm for 40 s onto the graphene patterns on the Cu foil, and the Cu was etched using an aqueous 0.1 M ammonium persulfate solution. The graphene patterns onto PMMA layer were then transfered onto an as-prepared flexible substrate. Finally, the supporting PMMA layer was removed by hot acetone (60 °C).

The optical transmittance of the NFGTM arrays fabricated onto a PEN substrate were characterized by UV-visible spectrophotometry (Agilent 8453). The current–voltage (I-V) characteristics of the graphene NFGTMs were measured using a Keithley 4200 Semiconductor Parameter Analyzer (room temperature, vacuum, and dark condition).

3. Results and Discussion

Figure 1a illustrates the scheme by which graphene nano-floating gate transistor memory (NFGTM) arrays were fabricated on a plastic substrate. To begin with, an AuNPs charge trapping layer with various sizes was deposited onto Al_2O_3/ITO/PEN substrate. After

the deposition of AuNPs charge trapping layer with various sizes, the *c*PVP tunneling dielectrics with various thicknesses were then formed on the substrate. Dumbbell-shaped graphene patterns were then transferred onto the pre-prepared *c*PVP substrate. The narrow strip segment of the dumbbell-shaped graphene functioned as the channel of the transistor, whereas the remainder of the strip formed the source/drain electrodes[34]. The length (L) and width (W) of the channel were 400 and 200 μm, respectively. A photograph of the graphene NFGTM array is displayed in **Figure 1b**. The NFGTM array on the PEN substrate exhibited good flexibility and optical transparency. The inset of **Figure 1b** shows the transmittance of the NFGTM array on a PEN substrate over the visible and near-infrared spectral range. The transparency was 86 % at 550 nm, and the average transparency over the range of 500 ~ 1000 nm was approximately 87 %.

We first examined the effects of the AuNP size on the performance of the graphene NFGTM. The sizes of thermally deposited AuNPs were controlled by varying the deposition thickness of the Au layer (t = 0 – 4 nm). The size distribution of AuNPs was verified using scanning electron microscope (SEM), showing that increasing the thickness of the Au layer increased the AuNP size from 3.9 to 15.6 nm, as shown in **Figure 2a**. The small and sparsely distributed AuNPs gradually coarsened and were distributed more densely as the Au layer thickness increased. **Figure 2b** shows the hysteresis loop of the resulting NFGTMs for the various sizes of the thermally deposited AuNPs. The *c*PVP layer thickness was fixed at 19 nm. Hysteresis was clearly observed in the drain current (I_D), which showed a double minimum conductance (Dirac voltage, V_{Dirac}) as a function of the gate voltage (V_G). The memory window, which was defined as the difference between two minimum conductance points (ΔV_{Dirac}), increased from 0.8 to 6 V as the AuNP size increased (0 – 6.7 nm), as shown in **Figure 2c**, and **S1**. These results clearly showed that hysteresis in the transfer characteristics originated mainly from charge carrier trapping in the AuNPs under gate bias conditions (**Figure 2d**). The density of charge traps in NPs is inversely proportional to the charging energy of the NP[35]. Because the charging energy decreases as the NP size increases, more charge carriers can become trapped in larger AuNPs. However, further increase in the AuNP sizes reduced the memory window of the device. This anomalous behavior may arise from the charge leakage through the defect in the tunneling barrier (i.e., *c*PVP). As nanoparticle size is increased more than 6.7 nm, the charge leakage over the tunneling barrier increases, which gives rise to the reduction of the program window. Thus, to prevent the charge leakage a thick tunneling barrier is need, but as shown in **Figure 2e** thicker tunneling dielectrics cause the reduction of memory windows due to the less probability for tunneling. Another possible

scenario for a reduced memory window for larger nanoparticles is the screening of the trapped charges in the AuNPs. As the AuNP size increased, the high electron density of the Au screens out the trapped charges on the NP surface, thereby reducing the net charge on the NP surface[36, 37]. The criterion for the reduction of memory window is the screening length of gold. If screening length is larger than the size of nanoparticle the actual electric field from trapped charges is not much affected due to the lack of the screening. However, for the larger nanoparticles than the screening length the mobile electrons in gold can screen out the electric field of trapped charges. The screening length of gold embodied in the plastic substrate is estimated to be about 6 nm. Thus, we believe that the program window is further reduced (or saturated at the lowest value) if we use the gold film instead of gold nanoparticles. The number of trapped electrons could be calculated using the equation $\Delta n = C_i \cdot \Delta V_{Dirac}/e$, where C_i and e are the specific capacitance of the gate dielectric (~ 90 nF/cm^2) and the element charge, respectively. The total number of trapped electrons increased from 0.4×10^{12} cm^{-2} (without Au NPs) to 3.3×10^{12} cm^{-2} (6.7 nm), but then decreased to 2.2×10^{12} cm^{-2} (11.3 nm), as shown in **Figure 2c**.

The effects of the tunneling dielectric layer thickness on the performance of the graphene NFGTMs prepared with AuNPs having an optimized size of 6.7 nm were investigated. The tunneling dielectric thickness was controlled by varying the concentration of the *c*PVP solution. **Figure 2e** shows the hysteresis loop in the graphene NFGTMs prepared with *c*PVP tunneling dielectric layers of various thicknesses. The hysteresis decreased dramatically for *c*PVP layers thicker than 19 nm. This reduction was attributed to the exponential decay of the tunneling probability with increasing *c*PVP thickness[38]. However, very thin *c*PVP layer displayed poor retention (**Figure S2**), even though the devices displayed higher memory windows, because the trapped charges in the Au NPs were easily released to the graphene channel due to the incomplete coverage of the ultrathin *c*PVP layer over the Al_2O_3 blocking dielectric layer onto which the Au NPs had been deposited[38]. Consequently, we could optimize the performances of the graphene NFGTMs by controlling the AuNP size and the *c*PVP layer thickness. We found the optimal conditions that yielded the best graphene NFGTM performance included 6.7 nm AuNPs and a 19 nm thick *c*PVP layer. Even under the optimized conditions, the memory window of the graphene NFGTM was only 6 V. The poor memory performance was understood as arising from the heavy p-type doping of the graphene (discussed below). The aqueous ammonium persurfate solution was utilized as copper etchant. Residual peroxydisurfate ions on the graphene surface during the copper removal process

withdrew electrons of graphene. This introduced heavy p-type chemical doping into the graphene, resulting the V_{Dirac} shift to the positive voltage direction[32, 39].

To maximize the conductance difference at a read gate bias, we introduced simple n-type doping into the graphene. The V_G for reading was 0 V. The n-type doping was achieved by dipping the devices into a poly(ether imine) (PEI) solution[40, 41]. Amine groups in the PEI acted as effective electron donors due to the presence of lone pair electrons. The lone pair electrons were attracted to the graphene layer under the downward electric field induced by the application of a positive gate voltage, resulting in a negative shift in V_{Dirac}. The degree of n-doping was controlled by varying the PEI dipping time as shown in **Figure 3**. For the doping time of 10 min, the Dirac voltage during the forward sweep shifted toward –11 V whereas the Dirac voltage during the reverse sweep approached 0 V. These shifts maximized the conductance difference between the forward and reverse sweeps at a zero gate voltage (the highest ON/OFF ratio between the programmed and erased states).

The memory window of the graphene NFGTM depended strongly on the number of trapped charges present in the charge-trapping AuNP layer, which relied on the magnitude of the V_G. **Figure 4a** shows the changes in the memory windows as a function of the V_G sweep range, for graphene NFGTMs based on graphene doped with PEI for 10 min. During the V_G sweep from –5 to +5 V, no significant bias hysteresis (only 0.8 V) could be observed; however, the memory windows of the devices increased significantly as the V_G sweep range increased, as shown in **Figure 4b**. The prominent hysteresis loops revealed that these memory characteristics resulted from charge trapping in the AuNPs. The total number of trapped charges increased from 0.4×10^{12} cm^{-2} for a ±5 V sweep range to 6.7×10^{12} cm^{-2} for a ±20 V sweep range; however, the memory windows decreased slightly after $V_G > \pm 14$ V due to electron back-injection from the ITO gate electrode to the AuNPs *via* Fowler–Nordheim tunneling[8, 21]. Importantly, the maximum memory windows were observed to be 12 V, the highest values yet achieved among graphene-channel memory devices. **Figure 4c** shows the reversible shifts in the transfer curves after application of a V_G of +20 V and –20 at a $V_D = 0$ V over 1 s. That is, subjecting the device to a programmed V_G (V_P) of +20 V resulted in the accumulation of the electron carriers, at the graphene/*c*PVP interface, after injection from graphene to the AuNPs, as shown in the right panel of **Figure 2d**. The electron charges trapped in the AuNPs produced a low electron current and a positive V_{Dirac} shift. By contrast, the application of a negative V_G (–20 V) during erasing (V_E) resulted in the transfer of electron carriers present in the AuNPs to the graphene/*c*PVP interface (left panel of **Figure 2d**). This

process led to a high electron current and a negative V_{Dirac} shift. Importantly, the program/erase current ratio at $V_G = 0$ V was 3.6.

The operating speed of the graphene NFGTM was investigated, as shown in **Figure 4d**. The ± 20 V program and erase bias pulses were applied to the gate electrode at pulse widths that varied from 1 to 10^{-6} s. A graphene NFGTM yielded Dirac voltage points of –1 and –13 V for V_P and V_E, respectively, over 1 s. Although the memory window decreased gradually as the P/E switching speed decreased, a reasonable memory window of 6 V was obtained by applying a bias pulse of 1 μs. The stability of the graphene NFGTMs was further investigated by performing retention time and cycling tests. **Figure 4e** shows the retention characteristics of the devices. The retention time was determined to exceed 10^5 s after application of $V_{P/E} = \pm$ 20 V. The P/E states were maintained during repeated cycling tests, which included 200 cycles at a switching speed of 1 s (**Figure 4f**).

Finally, the thermal and mechanical stabilities of the graphene NFGTM were intensively investigated, as shown in **Figure 5**. **Figure 5a** shows the hysteresis loops of a graphene NFGTM at elevated temperatures between 30 and 100°C. No appreciable changes were observed as the temperature was increased, but the memory windows increased gradually up to 70°C and became saturated at 14 V. The temperature-induced increase in the memory window may have been due to the reduced charge tunneling barriers through the *c*PVP dielectric layer, suggesting that the memory window could be recovered by cooling the device to room temperature. The changes in the memory windows and program/erase current ratios are summarized in **Figure 5b**. The retention characteristics of the devices measured at 100°C revealed that our graphene NFGTM exhibited an operation stability (**Figure 5c**) that was superior to that of the previously reported charge-transfer memory obtained using $Al_2O_3/HfO_x/Al_2O_3$ dielectric stacks on a graphene channel[8].

Mechanical flexibility and robustness are important characteristics for flexible electronics applications. Fatigue tests were performed on the graphene NFGTMs. Memory hysteresis loops were measured during 500 bending cycles in which a 2 % strain was applied, as shown in **Figure 5d**. The graphene NFGTM was bent along the directions parallel to the transistor channel length. The transfer characteristics of the graphene NFGTM remained invariant under bending, even after 500 cycles. The memory windows and ON/OFF current ratios were independent of the presence of mechanical fatigue, as summarized in **Figure 5e**. The retention characteristics of the devices after 500 bending cycles indicated that our graphene NFGTM exhibited excellent mechanical stability (**Figure 5f**).

4. Conclusion

In summary, we describe the first example of a flexible and transparent graphene NFGTM array on a plastic substrate. AuNPs provided an effective charge storage layer embedded at the interface between the *c*PVP tunneling dielectric layer and the Al_2O_3 blocking dielectric layer. The graphene memory performance was optimized by controlling the AuNP size, the *c*PVP thickness, and the graphene doping. The resulting devices exhibited excellent programmable memory performances, including a large memory window (12 V), fast switching speed (1 μs), robust electrical reliability (10^5 s), and good mechanical (500 cycles) and thermal stability (100 °C).

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References

1. B. J. Kim, Y. Ko, J. H. Cho and J. Cho, *Small*, 2013, 9, 3784–3791.
2. T. Sekitani, T. Yokota, U. Zschieschang, H. Klauk, S. Bauer, K. Takeuchi, M. Takamiya, T. Sakurai and T. Someya, *Science*, 2009, 326, 1516-1519.
3. S. K. Hong, J. E. Kim, S. O. Kim, S.-Y. Choi and B. J. Cho, *IEEE Electron Device Lett.*, 2010, 31, 1005-1007.
4. H. Y. Jeong, J. Y. Kim, J. W. Kim, J. O. Hwang, J.-E. Kim, J. Y. Lee, T. H. Yoon, B. J. Cho, S. O. Kim, R. S. Ruoff and S.-Y. Choi, *Nano Lett.*, 2010, 10, 4381-4386.
5. D. I. Son, T. W. Kim, J. H. Shim, J. H. Jung, D. U. Lee, J. M. Lee, W. I. Park and W. K. Choi, *Nano Lett.*, 2010, 10, 2441-2447.
6. J. Liu, Z. Yin, X. Cao, F. Zhao, L. Wang, W. Huang and H. Zhang, *Adv. Mater.*, 2013, 25, 233-238.
7. Y. Ji, S. Lee, B. Cho, S. Song and T. Lee, *ACS nano*, 2011, 5, 5995-6000.
8. S. M. Kim, E. B. Song, S. Lee, J. Zhu, D. H. Seo, M. Mecklenburg, S. Seo and K. L. Wang, *ACS nano*, 2012, 6, 7879-7884.
9. S.-J. Kim and J.-S. Lee, *Nano Lett.*, 2010, 10, 2884-2890.
10. Y. Zhou, S.-T. Han, Z.-X. Xu and V. A. L. Roy, *Nanotechnol.*, 2012, 23, 344014.
11. S. T. Han, Y. Zhou and V. Roy, *Adv. Mater.*, 2013, 25, 5425-5449.
12. M. Kang, K. J. Baeg, D. Khim, Y. Y. Noh and D. Y. Kim, *Adv. Funct. Mater.*, 2013, 23, 3503-3512.
13. R. Yang, C. Zhu, J. Meng, Z. Huo, M. Cheng, D. Liu, W. Yang, D. Shi, M. Liu and G. Zhang, *Sci. Rep.*, 2013, 3, 2126.
14. S. Wang, J. Pu, D. S. Chan, B. J. Cho and K. P. Loh, *Appl. Phys. Lett.*, 2010, 96, 143109
15. A. J. Hong, E. B. Song, H. S. Yu, M. J. Allen, J. Kim, J. D. Fowler, J. K. Wassei, Y. Park, Y. Wang, J. Zou, R. B. Kaner, B. H. Weiller and K. L. Wang, *ACS nano*, 2011, 5, 7812-7817.
16. S. Myung, J. Park, H. Lee, K. S. Kim and S. Hong, *Adv. Mater.*, 2010, 22, 2045-2049.

17. S. Imam, T. Deshpande, A. Guermoune, M. Siaj and T. Szkopek, *Appl. Phys. Lett.*, 2011, 99, 082109.
18. M. S. Choi, G.-H. Lee, Y.-J. Yu, D.-Y. Lee, S. H. Lee, P. Kim, J. Hone and W. J. Yoo, *Nat. Commun.*, 2013, 4, 1624.
19. Y. Zheng, G.-X. Ni, C.-T. Toh, M.-G. Zeng, S.-T. Chen, K. Yao and B. Özyilmaz, *Appl. Phys. Lett.*, 2009, 94, 163505.
20. Y. Zheng, G.-X. Ni, C.-T. Toh, C.-Y. Tan, K. Yao and B. Özyilmaz, *Phys. Rev. Lett.*, 2010, 105, 166602.
21. S. Lee, E. B. Song, S. Kim, D. H. Seo, S. Seo, T. W. Kang and K. L. Wang, *Appl. Phys. Lett.*, 2012, 100, 023109.
22. E. B. Song, B. Lian, S. Min Kim, S. Lee, T.-K. Chung, M. Wang, C. Zeng, G. Xu, K. Wong, Y. Zhou, H. I. Rasool, D. H. Seo, H.-J. Chung, J. Heo, S. Seo and K. L. Wang, *Appl. Phys. Lett.*, 2011, 99, 042109.
23. Y. Ji, M. Choe, B. Cho, S. Song, J. Yoon, H. C. Ko and T. Lee, *Nanotechnol.*, 2012, 23, 105202.
24. P. Heremans, G. H. Gelinck, R. Müller, K.-J. Baeg, D.-Y. Kim and Y.-Y. Noh, *Chem. Mater.*, 2010, 23, 341-358.
25. P. Pavan, R. Bez, P. Olivo and E. Zanoni, *Proc. IEEE*, 1997, 85, 1248-1271.
26. R. Bez, E. Camerlenghi, A. Modelli and A. Visconti, *Proc. IEEE*, 2003, 91, 489-502.
27. C.-Y. Lu, K.-Y. Hsieh and R. Liu, *Microelectron. Eng.*, 2009, 86, 283-286.
28. J.-S. Lee, *Electron. Mater. Lett.*, 2011, 7, 175-183.
29. A. Reina, X. Jia, J. Ho, D. Nezich, H. Son, V. Bulovic, M. S. Dresselhaus and J. Kong, *Nano Lett.*, 2008, 9, 30-35.
30. K. S. Kim, Y. Zhao, H. Jang, S. Y. Lee, J. M. Kim, K. S. Kim, J.-H. Ahn, P. Kim, J.-Y. Choi and B. H. Hong, *Nature*, 2009, 457, 706-710.
31. X. Li, W. Cai, J. An, S. Kim, J. Nah, D. Yang, R. Piner, A. Velamakanni, I. Jung, E. Tutuc, S. K. Banerjee, L. Colombo and R. S. Ruoff, *Science*, 2009, 324, 1312-1314.
32. S. Bae, H. Kim, Y. Lee, X. Xu, J.-S. Park, Y. Zheng, J. Balakrishnan, T. Lei, H. R. Kim, Y. I. Song, Y.-J. Kim, K. S. Kim, B. Özyilmaz, J.-H. Ahn, B. H. Hong and S. Iijima, *Nat. Nanotechnol.*, 2010, 5, 574-578.
33. X. Li, Y. Zhu, W. Cai, M. Borysiak, B. Han, D. Chen, R. D. Piner, L. Colombo and R. S. Ruoff, *Nano Lett.*, 2009, 9, 4359-4363.
34. S.-K. Lee, B. J. Kim, H. Jang, S. C. Yoon, C. Lee, B. H. Hong, J. A. Rogers, J. H. Cho and J.-H. Ahn, *Nano Lett.*, 2011, 11, 4642-4646.
35. S.-T. Han, Y. Zhou, Z.-X. Xu, V. Roy and T. Hung, *J. Mater. Chem.*, 2011, 21, 14575-14580.
36. J. M. Ziman, *Principles of the Theory of Solids*, Cambridge University Press, NY, USA, 1979.
37. C. Kittel and P. McEuen, *Introduction to solid state physics*, Wiley New York, NY, USA, 2004.
38. K. J. Baeg, Y. Y. Noh, H. Sirringhaus and D. Y. Kim, *Adv. Funct. Mater.*, 2010, 20, 224-230.
39. H.-Z. Geng, K. K. Kim, K. P. So, Y. S. Lee, Y. Chang and Y. H. Lee, *J. Am. Chem. Soc.*, 2007, 129, 7758-7759.
40. M. Shim, A. Javey, N. W. Shi Kam and H. Dai, *J. Am. Chem. Soc.*, 2001, 123, 11512-11513.
41. D. B. Farmer, R. Golizadeh-Mojarad, V. Perebeinos, Y.-M. Lin, G. S. Tulevski, J. C. Tsang and P. Avouris, *Nano Lett.*, 2008, 9, 388-392.

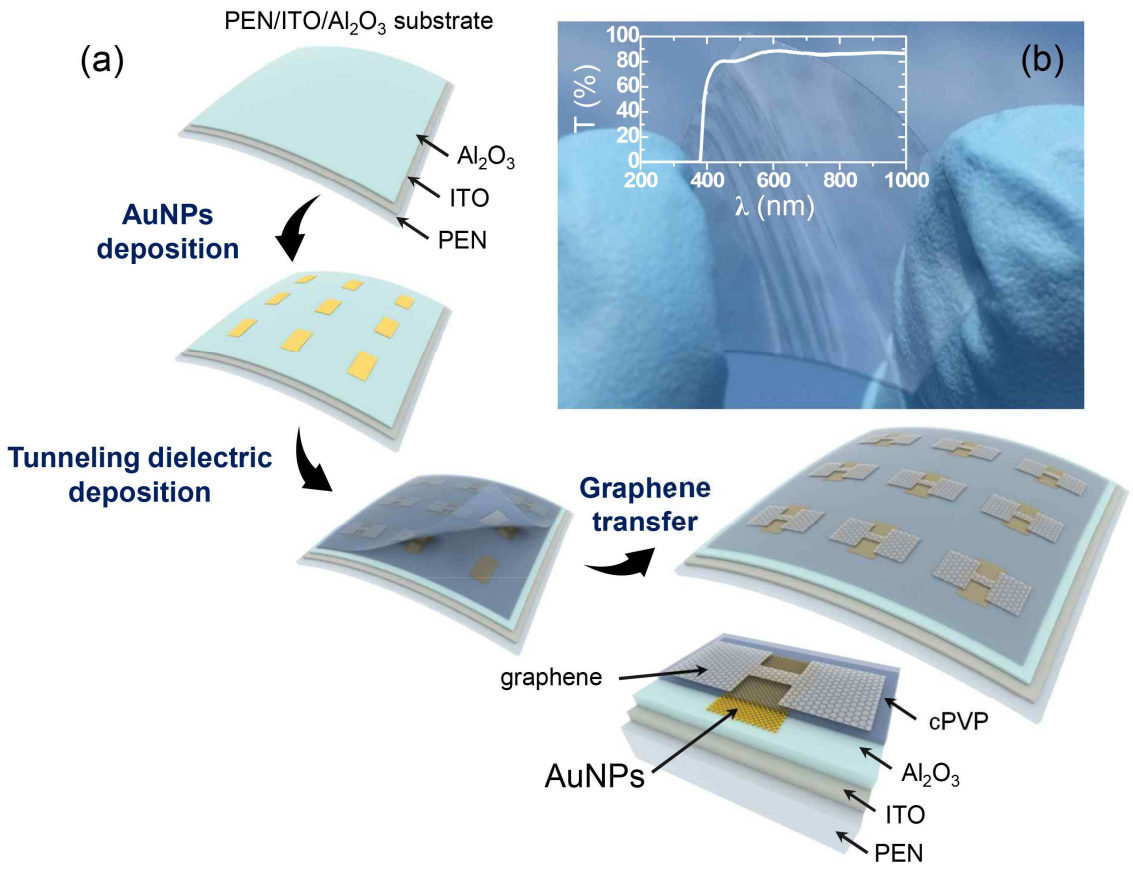

Figure 1. (a) Schematic diagram showing the fabrication of a transparent and flexible graphene nano-floating gate transistor memory (NFGTM) on a flexible plastic substrate. (b) Photograph of the graphene NFGTM array. The inset shows the optical transmittance of a NFGTM array on PEN substrate and a scanning electron microscope image of a NFGTM (scale bar: 200 μm).

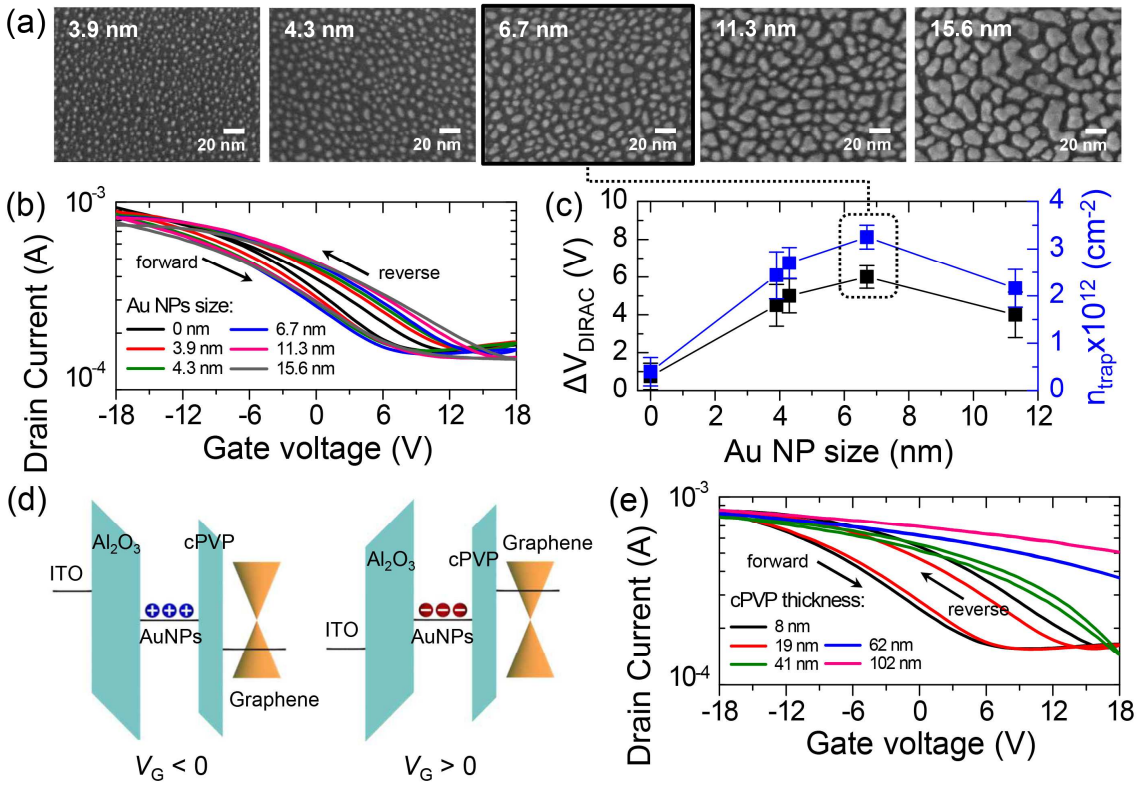

Figure 2. (a) SEM images of the thermally-deposited Au NPs. (b) Memory hysteresis loop of the graphene NFGTMs prepared from thermally-deposited Au NPs of various sizes (*c*PVP thickness = 19 nm). (c) Changes in the memory windows and concentrations of the trapped charges as a function of the Au NP size. (d) Energy band diagrams of the NFGTMs under negative and positive gate bias conditions. (e) Memory hysteresis loop of the graphene NFGTMs prepared using *c*PVP tunneling dielectric layers of various thicknesses.

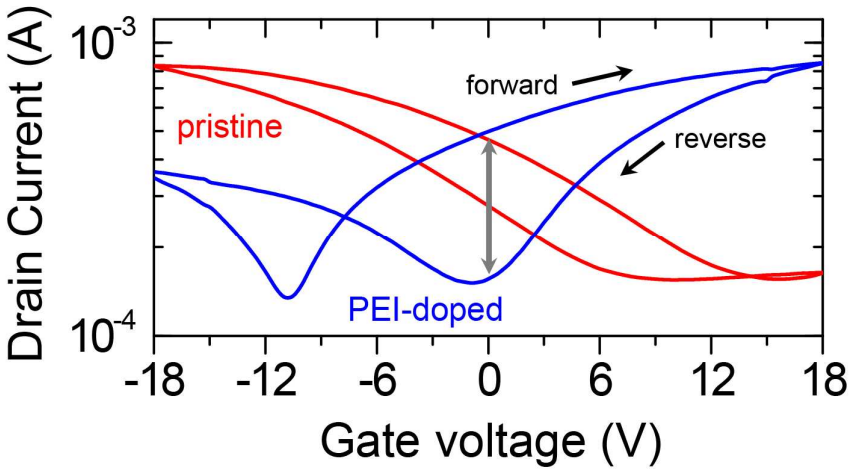

Figure 3. Memory hysteresis loop of the graphene NFGTMs based on pristine and PEI-doped graphene. The PEI treatment time was 10 min.

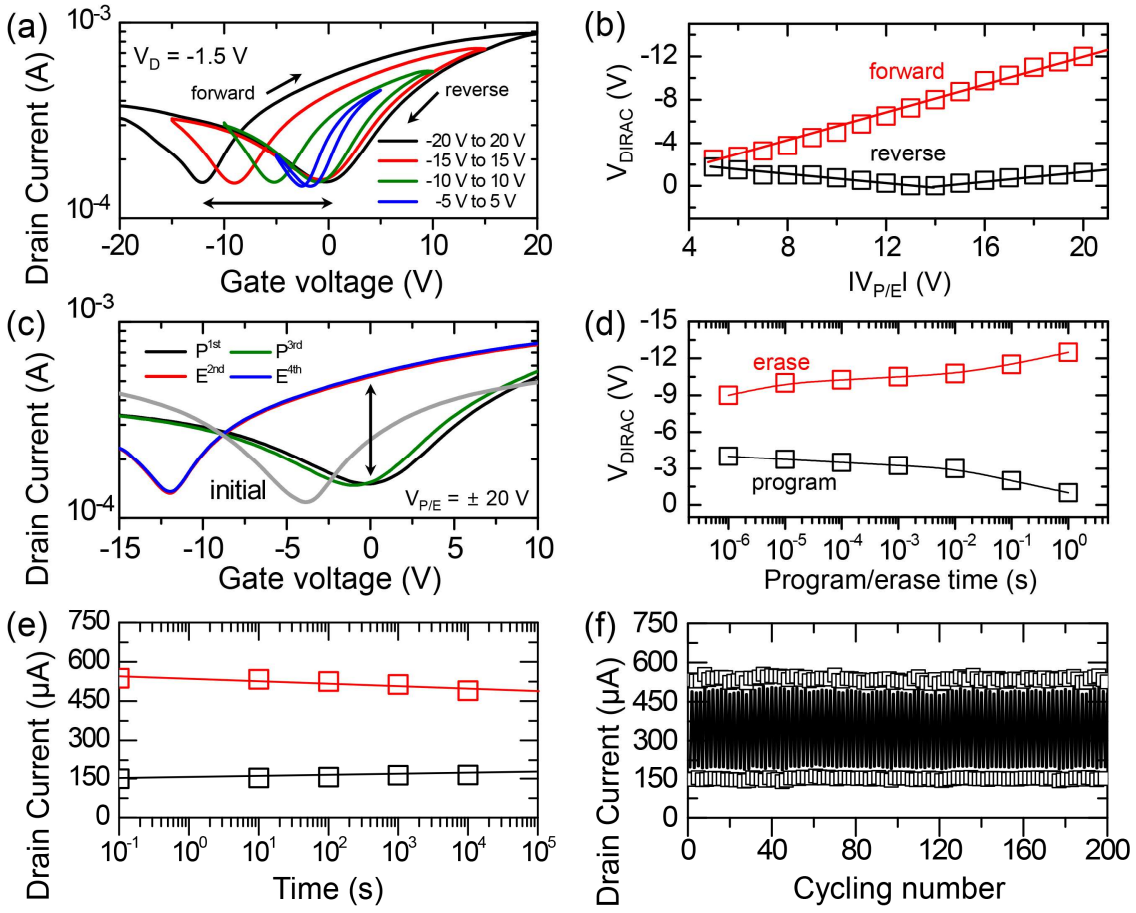

Figure 4. (a) Memory hysteresis loop of the graphene NFGTMs based on graphene doped with PEI for 10 min. (b) Memory windows as a function of applied $V_{P/E}$. (c) Shifts in the transfer curves at V_D = –1.5 V, upon application of $V_{P/E}$ = +20 V (program) and –20 V (erase). (d) P/E speeds of the graphene NFGTMs. (e) Retention time and (f) cycling tests for the graphene NFGTMs.

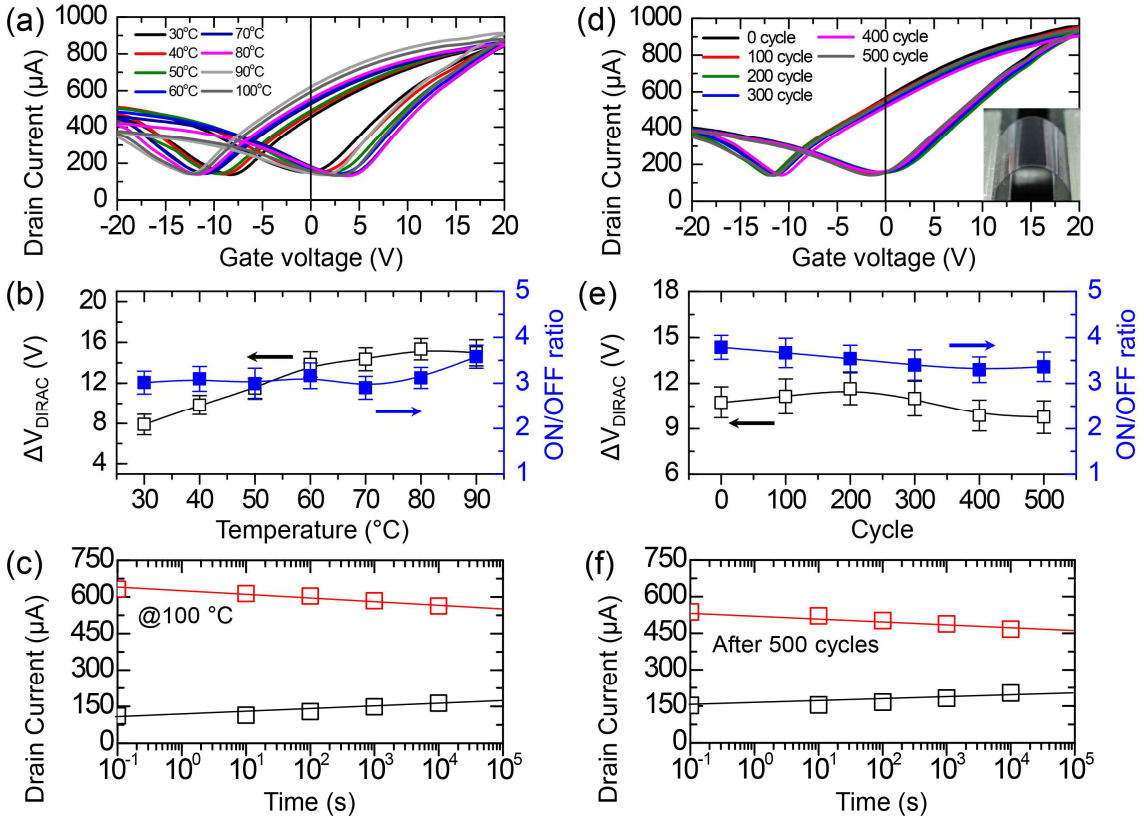

Figure 5. (a) Temperature-dependent memory hysteresis loop for a graphene NFGTM prepared using graphene doped with PEI for 10 min. (b) Memory windows and program/erase current ratio of the graphene NFGTM as a function of the temperature. (c) Retention time tests for the graphene NFGTM at 100°C. (d) Memory hysteresis loop as a function of cycle (strain = 2 %) for a graphene NFGTM prepared using graphene doped with PEI for 10 min. The inset shows the home-built bending machine. (e) Memory windows and program/erase current ratio as a function of cycle, for a graphene NFGTM. (f) Retention time tests for the graphene NFGTM after 500 bending cycles.

ToC figure