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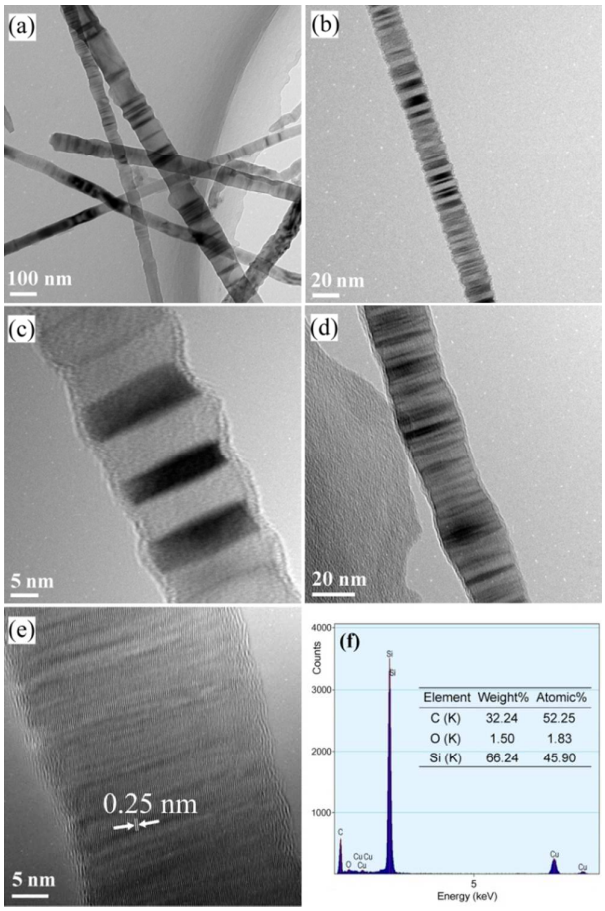

Highlight:

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Cite this: DOI: 10.1039/c0xx00000x

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ARTICLE TYPE

Synthesis and formation mechanism of twinned SiC nanowires made by a catalyst-free thermal chemical vapour deposition method

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Received (in XXX, XXX) Xth XXXXXXXXX 20XX, Accepted Xth XXXXXXXXX 20XX
DOI: 10.1039/b000000x

Twinned SiC nanowires were prepared on a silicon wafer by a catalyst-free thermal chemical vapour deposition (CVD) method at 1500 °C in a flowing Ar atmosphere. X-ray diffraction (XRD), field emission scanning electron microscopy (FESEM), energy dispersive spectroscopy (EDS), transmission electron microscopy (TEM), and high-resolution transmission electron microscopy (HRTEM) were used to characterise the phase composition, morphology, and microstructure of the as-received nanowires. The as-synthesised twinned nanowires were up to several hundred microns long and had relatively homogeneous diameters in the range 20 to 100 nm. The growth process of the twinned SiC nanowires was dominated by a vapour-solid (VS) mechanism. Based on the competition of stacking fault energy and electrostatic energy, a growth model has been proposed to understand the phenomenon of twinning.

Introduction

One-dimensional nanostructures, structures which provide a good system to investigate the dependence of electrical and thermal transport or mechanical properties on dimensionality and size reduction, have received steadily growing interest.[1] Over the past decades, one-dimensional (1-D) SiC nanostructures, *i.e.*, nanotubes, nanowires, nanorods, nanobelts, and nanocables have stimulated considerable interest due to their excellent properties, such as: high mechanical strength, high thermal conductivity, high chemical stability, and high thermal stability.[2] Among these 1-D nanostructures, SiC nanowires have attracted much attention for their potential applications in novel microelectronic, optoelectronic, and magnetic nanoscale devices.[3] Furthermore, SiC nanowire is a suitable material for the fabrication of high performance nanodevices in harsh environment applications which require high temperature resistance, high power, and high frequency. Inspired by this, research has been devoted to the synthesis of 1-D SiC nanostructures.[4]

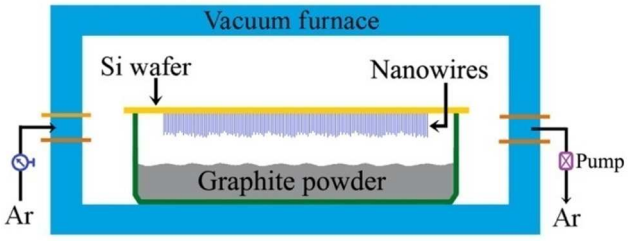
Twinning, a common crystal defect, is a type of stacking fault which has been regarded as an important microstructural defect in nanoscale materials. Various twinned 1-D nanowires have been synthesised such as: Si,[5] GaP,[6] GaAs,[7] ZnSe,[8] ZnO[9], ZnS[10], *etc*. Twinning in 1-D SiC nanostructures by vapour-liquid-solid (VLS) mechanism and vapour-solid (VS) mechanism has been reported.[11] Wang *et al*. fabricated twinned SiC nanowires by the carbothermal reduction of a carbonaceous silica xerogel prepared from tetraethoxysilane (TEOS) and biphenyl with iron nitrate as an additive.[11] Wu *et al*. have synthesised twinned SiC zig-zag nanoneedles by silicon evaporation on to multiwall carbon nanotubes at 1500 °C for 8 h.[12] Li *et al*. demonstrate a pyrolytic deposition technique that uses a TEOS precursor for preparing twinned SiC nanowires.[13] However, few reports using a simple catalyst-free thermal chemical vapour deposition (CVD) method for the construction of twinned SiC nanowires have been published.

In this paper, the growth of twinned SiC nanowires by a simple thermal CVD method on an Si wafer without the assistance of a metal catalyst is reported. The morphology, phase composition, and microstructure of the as-synthesised nanowires were characterised. The growth mechanism for the SiC nanowires and the formation procedure of the twinning structure is proposed.

Experimental

The synthesis of twinned SiC nanowires was carried out in a high-temperature vacuum furnace by a catalyst-free thermal CVD method. In brief, commercial graphite powder (10 g; purity 99.9 % (w/w)) was placed into a columnar graphite crucible (80 mm in diameter and 35 mm high). An n-type Si (100) wafer (with a resistivity of 4 Ω·cm) measuring 100 mm × 100 mm was ultrasonically cleaned and used as the substrate. Then the crucible was covered by the cleaned Si wafer and moved into the centre of the vacuum furnace as shown in Scheme 1. Afterwards, the furnace was evacuated to 10 Pa by a rotary pump and argon gas (purity 99.999% (v/v)) was introduced until the furnace pressure reached 0.14 MPa. The whole set-up was heated in flowing Ar to 1000 °C at a heating rate of 10 °C/min, then to 1500 °C at a rate of 3 °C/min and maintained at this temperature for 3 h. When the furnace was naturally cooled to room temperature, the as-grown product was collected.

X-ray diffraction (XRD), field emission scanning electron microscopy (FESEM, JEOL JSM6700F, Japan), and high-



Scheme 1 Schematic diagram of experimental setup.

resolution transmission electron microscope (HRTEM, JEOL JEM-2010, Japan, accelerating voltage 200 kV) were used to examine their phase compositions, morphologies, and microstructures. Samples for TEM observation were dispersed in absolute ethanol by ultrasonication for 10 min, and a drop of the suspension containing the products was dropped onto a copper grid coated with an amorphous carbon supporting film and then dried in air. The energy dispersive spectroscopies (EDS) linked with the FESEM and the HRTEM were used to assist with the phase identification.

Results and discussion

The general morphology of the thermal evaporation product is shown in Fig. 1. Fig. 1a shows SiC nanowires that were synthesised using the catalyst-free thermal CVD method. The FESEM images at low magnification (Fig. 1a) and high magnification (Fig. 1b) all revealed that both straight and curved nanowires grew randomly on the Si substrate. Nanowires with lengths of up to several hundred microns and relatively homogeneous diameters in the range 20 to 100 nm could be routinely achieved. Fig. 1b shows that the surface of these nanowires was rough and randomly oriented. EDS (Fig. 1c) found that the nanowires in Fig. 1a mainly contained Si and C, indicating that the products were SiC nanowires. Fig. 1d shows the X-ray diffraction (XRD) pattern of the products. The strong intensities and narrow widths of the peaks indicated that the nanowires were crystalline. As Fig. 1d indicated, all the strong peaks could be indexed to β-SiC. A small peak, signed SF ahead of the highest intensity peak (111), was assumed to have been due to stacking faults (twins).[14]

Further details of the internal structure and morphology of the as-fabricated nanowires can be revealed by TEM and HRTEM. Fig. 2a shows the TEM image of a typical sample of SiC nanowires obtained by catalyst-free CVD process. Since no metallic balls were found at the tips of the nanowires, it indicated that the growth mechanism was attributable to a VS mechanism rather than a VLS mechanism [15] as reported in the literature. Figs 2b and 2c are higher magnification TEM images of some representative products, in which the zig-zag surface is visible. There were dense stacking faults and twins along the growth direction of the nanowire. Figs 2c and 2d reveal that the nanowire was composed of a crystalline core with a diameter of between 20 and 100 nm and coated with an amorphous shell layer with a thickness of between 1 and 3 nm. Fig. 2e shows that the spacing within the crystal between two adjacent lattice planes was 0.25 nm, indicating the twinned SiC nanowire grew along the [111] direction. Generally, the literature about twinned SiC nanowires mainly concerns (111) twin.[11,16] Chen *et al.* prepared

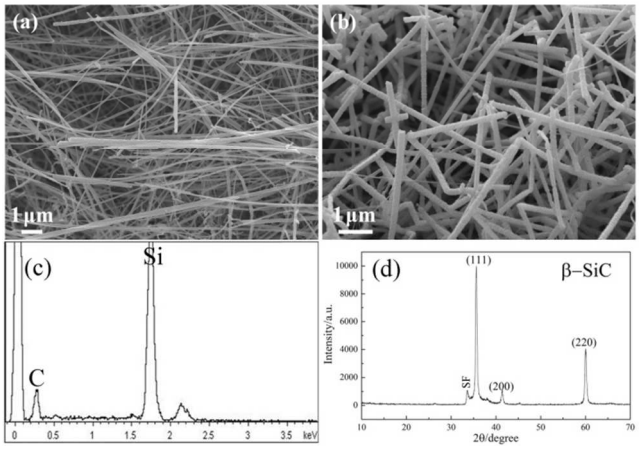


Fig. 1 (a) Low magnification and (b) high magnification FESEM images of the as-grown nanowires; (c) EDS pattern of the nanowires; (d) X-ray diffraction pattern of the nanowires.

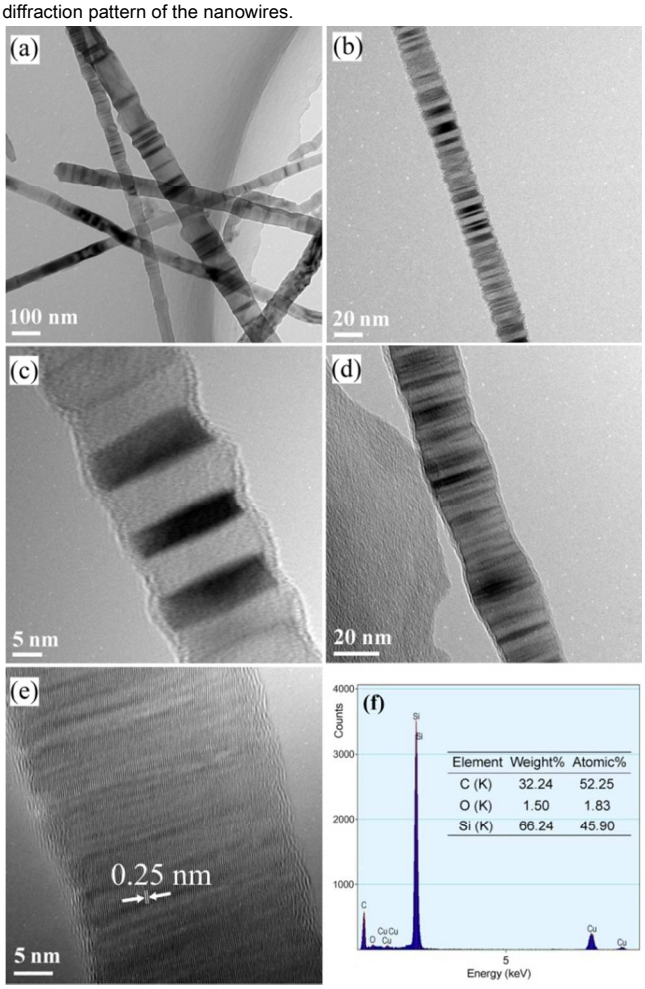


Fig. 2 (a-d) Typical low magnification TEM images of the twinned SiC nanowires; (e) A typical HRTEM image of the twinned SiC nanowires; (f) the corresponding EDS of the nanowires.

hexagonal prism shaped β-SiC nanowires with thinner tips and a (111) twin structure by an evaporation method.[16] Fig. 2f shows the EDS pattern of the twinned nanowires and demonstrates that the products mainly contained Si and C. The small amount of oxygen comes from the surviving thin oxide shell and remained as oxygen in the system. According to the TEM observations

(Figs 2c and 2d) and XRD pattern (Fig. 1d), it was believed that the core of these nanowires was crystalline SiC and that the shell was a very thin amorphous SiO_2 layer.[5, 13, 16]

During the CVD procedure, no metallic catalyst was introduced and no metallic droplets were observed at the tips of the nanowires. Thus, the growth of the nanowires in this research was not following the conventional catalyst-assisted VLS mechanism. [15] On the other hand, a catalyst-free VS mechanism for the growth of synthesised SiC nanowires was proposed. Although the exact mechanism responsible for 1-D growth in the vapour phase remained unclear, this approach has been explored by many research groups to synthesise whiskers and derivatives from a variety of materials.[1,17] VS growth is generally believed to start at nanometric nuclei created *in situ* and it proceeds along one crystallographic direction.[1,17] For example, Chen *et al., Zhang et al. and S. Al-Ruqeishi et al.* all fabricated a large number of SiC nanowires by different catalyst-free method, in which a similar VS mechanism was proposed to interpret the growth procedure. [18] Since no catalyst was introduced and no metallic droplets were detected in the nanowires' tips, a similar VS growth mechanism of SiC nanowires has been explained in our study.

In this work, the as-synthesized nanowires cover on the silicon wafer when temperature cool down. Before argon was introduced to the experimental set-up, the vapour was difficult to expel fully from the system by the rotary pump. So the residual oxygen (O_2 and H_2O) in the furnace and the oxygen released by the refractory lining can react with the graphite powder following reaction (1).[19] The graphite powder was gasified to form C vapour as the temperature gradually increased.

SiO gas was formed according to reactions (2) to (4), which increased the probability of the reaction with carbon vapour.

$$C_{(s)} + O_{2(g)} \rightarrow 2CO_{(g)} \quad (1)$$

$$SiO_{2(s)} + C_{(g)} \rightarrow SiO_{(g)} + CO_{(g)} \quad (2)$$

$$SiO_{2(s)} + CO_{(g)} \rightarrow SiO_{(g)} + CO_{2(g)} \quad (3)$$

$$Si_{(s)} + SiO_{2(s)} \rightarrow 2SiO_{(g)} \quad (4)$$

After that, the generated SiO vapour and Si wafer reacted further with CO according to reactions (5) and (6). Actually, the formed CO_2 vapour from reactions (3), (5), and (6) cannot be stable in this system on account of reaction (7) between CO_2 vapour and the graphite.

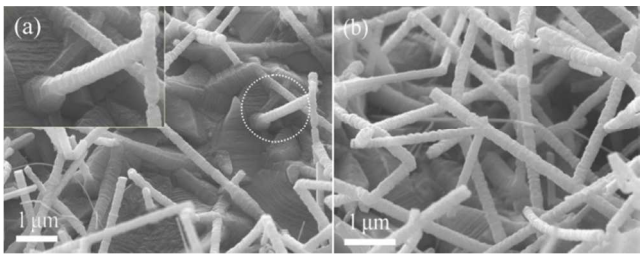


Fig. 3 FESEM image of (a) pyramid-like SiC structure and (b) SiC nanowires generated from the pyramid-like SiC structure.

$$SiO_{(g)} + 3CO_{(g)} \rightarrow SiC_{(s)} + 2CO_{2(g)} \quad (5)$$

$$Si_{(s)} + 2CO_{(g)} \rightarrow SiC_{(s)} + CO_{2(g)} \quad (6)$$

$$C_{(s)} + CO_{2(g)} \rightarrow 2CO_{(g)} \quad (7)$$

Based on the aforementioned reactions, SiC nuclei were generated on the Si substrate, as shown in Fig. 3 (a) which also shows a pyramid-like SiC structure, from which the SiC nanowires originated. Since the SiC nanowires always grew along the (111) plane resulting from the lowest-energy principle,[12,13,16] a layer of SiC nanowires was successfully formed on the Si substrate (Fig. 3b).

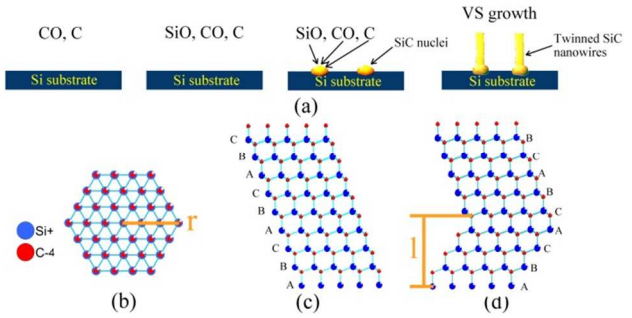
In the course of synthesising SiC nanowires, the effects of oxygen content is noticeable. M. S. Al-Ruqeishi *et al.* studied the effect of substrate locations and oxygen gas on the yield of β-SiC nanowires. [18] They revealed that introducing oxygen gas as an ambient gas instead of argon reduced the growth at locations close to the graphite source. [18] In this work, however, the gas compositions in the furnace will become very complicated at high temperatures. Under our current experimental instruments, it is quite difficult to examine the oxygen content exactly during the high-temperature reaction process. A further study on how the oxygen content affect the morphology and density of SiC nanowires is still necessary.

Scheme 2a shows the proposed mechanism underpinning such a VS process. However, it produced a type of twinned nanowire rather than conventional monocrystal nanowires. Here, the formation mechanism of such twinned nanowires is discussed.

In recent years, studies have shown that the twin structure is a common crystal defect in nanowires such as Si,[5] GaP,[6] GaAs,[7] ZnO,[9] ZnS,[10] SiC,[11] *etc*. As is known, SiC crystals possess more than 200 polytypes, in which 3C, 4H, and 6H are the most popular. The 3C-SiC polytype is the only cubic polytype which has a stacking sequence ABCABC. 4H-SiC consists of an equal number of cubic and hexagonal bonds with stacking sequences of ABCB. Two-thirds of 6H-SiC are composed of cubic bonds and one-third of hexagonal bonds, with stacking sequences of ABCACB.[20] Among them, 3C-SiC is more stable compared with other hexagonal polytypes up to a temperature of approximately 2100 °C.[21] That is to say, 3C-SiC is easy to nucleate and grow at relatively low temperatures. The literature shows that the SiC polytype content is also defined by some other conditions during preparation (pressure, environment) and presence of impurities.[22] Wei *et al.* synthesised 6H-SiC nanowires by a microwave method in the presence of nano-Al powders at below 1300 °C. [23]

Furthermore, when the diameter of a 1-D nanostructure reached nanoscale, the effects of surface energy (include solid surface, liquid surface, solid-liquid surface, twin boundary, and edge of twin boundary) become noticeable.[11] Thus, a possible explanation for the twinned structure was proposed which was attributed to the minimisation of the total energy.

As is known, the {111} planes of SiC have a lower surface energy than other {*hkl*} planes.[24] The SiC nanowires grew along the preferential [111] direction through the stacking of (111) planes. For this reason, although 4H or 6H stacking sequence are always existed in twinned SiC nanowires, the nanowires are



Scheme 2 (a) A proposed mechanism for the growth of twinned nanowires; (b) top view of single atomic layer of the nanowire with the radius *r*; (c) side view of the 3C-SiC nanowire structures; (d) side view of the twinned SiC nanowire structures.

mainly grow along [111] direction. Generally, literatures about twinned SiC nanowires are mainly about (111) twin.[11, 16] With the stacking of Si or C atoms, as seen in Scheme 2c-2d, the {111} surface on one side is either all Si atoms or C atoms. In SiC nanowires, the bonding between atoms shows both covalent and ionic characteristics, which involved charge transfer and resulted in the presence of both cations and anions. Owing to the difference of electronegativity between Si atoms and C atoms, some electrons will transfer from Si to C. Based on this, the electrostatic energy became a significant part of the total energy. In particular the surface charge interaction plays a key role in the stability of the nanowires.[16]

As shown in Scheme 2c-2d, the twinned SiC nanowires consisted of a mixture of hexagonal and cubic stackings of Si-C layers, and the regular appearance of twins suggested that the (111) twin was energetically favourable in SiC nanowires. In this case, stacking fault energy was defined as the extra energy which was used to form a twinned boundary and the electrostatic energy was defined as the potential energy of all the ions in the nanowire. In this work, the formation mechanism of the twin structure of the SiC nanowires was proposed by taking into account the stacking fault energy (E(r)) and the electrostatic energy difference between the ABC + A (Scheme 2c) stacking sequence and the ABC + B (Scheme 2d) stacking sequence ($\Delta E(r, l)$).[16] The formation of twinning boundary costs energy E(r), but $\Delta E(r, l)$ made the new layer of nanowires tend to form a twinned grain boundary. The literatures shows that the segment thickness is linearly proportional to the nanowire radius and that the electrostatic energy difference $\Delta E(r, l)$ becomes larger along with segment thickness growth.[11, 16]

Therefore the stacking fault energy may be expressed in the form of equation (8), where r is the radius of a nanowire, γ and τ are constants. The relationship between the segment thickness l and the radius r can be expressed by equation (9) on account of the negative $\Delta E(r, l)$ making the new layer of nanowire tend to form a twin boundary and the positive E(r) tending to keep the blended structure.

$$E(r) = \gamma \cdot r + \tau \quad (8)$$

$$\Delta E(r, l) + E(r) = 0 \quad (9)$$

When the thickness of new segment l' satisfied equation (9), a twinned grain boundary was formed (Scheme 2c).

Conclusions

In summary, twinned SiC nanowires were successfully synthesised by a catalyst-free CVD method on silicon wafer. The as-obtained twinned nanowires had lengths of up to several hundred microns and relatively homogeneous diameters in the range 20 to 100 nm. The VS growth mechanism was responsible for the initial nucleation and twinned nanowire formation. Moreover, a growth model was proposed to understand the phenomenon of stacking faults and twinning based on the competition of stacking fault energy and electrostatic energy. The twin structure was energetically favourable to the growth of SiC nanowires.

Acknowledgements

This work was financially supported by the National Natural Science Foundation of China (Grant Nos. 51032007 and 51272241), the Fundamental Research Funds for the Central Universities (Grant No. 2652013040) and the Research Fund for the Docoral Program of Higher Education of China (Grant No. 20130022110006). K. Chen also thanks the Innovation Research Fund for Postgraduate of China University of Geosciences (Beijing).

Notes and references

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