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Parallel Nanoimaging using an Array of 30 Heated Microcantilevers

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ABSTRACT

A key limitation of atomic force microscopy (AFM) is the size of the measurement area and the speed with which this area can be measured. Cantilever arrays have the potential to increase the measurement area and speed compared to single cantilevers, although the integration and use of cantilever arrays is still not widespread. We report integration of an array of 30 individually addressable cantilevers into a commercial AFM. Each cantilever has an integrated resistive heater-thermometer that can measure nanometer-scale topography by tracking the cantilever heat flow. Parallel imaging with this AFM array can acquire an image of size 0.510 mm × 0.425 mm, much larger than typical AFM images. We acquired a 9.05 million-pixel image in 256 seconds at a cantilever scan speed of 226 μm/sec with noise-limited vertical resolution of 1.21 nm and pixels of size 72.15 nm × 351.5 nm. This throughput is more than two orders of magnitude larger than conventional AFM measurements.

Keywords: Atomic force microscope (AFM), cantilever, array, nanotopography, high-speed imaging.

1. Introduction:

The atomic force microscope (AFM) is widely used to probe surfaces at the nanometer scale [1, 2], typically realized as a single cantilever tip. Multi-cantilever AFM has been proposed to improve the throughput (measurement speed and area) of AFM, for example in applications such as maskless nanolithography [3-5], material property analysis [6-9], high density data storage [10, 11], and high throughput biological measurements [12, 13]. Using an array of microcantilevers in parallel can greatly improve the measurement area and speed of AFM compared to single cantilevers [10, 14]. However, the independent and simultaneous operation of multiple cantilevers in the array remains a challenge.

A typical single-cantilever AFM employs an optical-lever setup, with a laser beam reflecting off of the cantilever and onto a detector [1, 2]. While this configuration is relatively easy to implement and provides high quality nanometer-scale measurements, it cannot be easily scaled up to large cantilever arrays due to the complexity in the optical setup, signal processing, and restrictions on cantilever geometries [15, 16]. One approach to realizing large cantilever arrays uses cantilevers with embedded deflection sensors; for example arrays of cantilevers with embedded topography sensors such as piezoresistive strain sensors [3, 17, 18] or heater-thermometers [4, 10, 11, 19, 20] have been used for topography imaging [10, 11, 19, 21], manufacturing [4, 19, 20], and data storage [10, 11].

There still remain many challenges to the scale-up and application of cantilever arrays. Some publications report only modest improvements in throughput due to limitations in the topography sensing physics, AFM hardware, data acquisition and processing. The performance and scalability of arrays employing optical sensing techniques are fundamentally limited by the uniformity of the illumination source and strict requirements in the cantilever and substrate geometry. However, instrumentation limitations such as the need to build custom AFMs, complex optics, speed and resolution of the camera sensor, and signal processing software currently limit the array throughput [12, 22, 23]. Issues such as poor cantilever designs, rudimentary homemade AFMs, and non-optimal topography sensing electronics, challenge the performance of arrays with embedded sensors [24, 25]. The throughput advantage of cantilever arrays can be fully realized by optimizing component and system level design parameters to maximize

array performance [19]. The design parameters include the topography sensor, cantilever and array geometry, AFM, physical adapters, electronics, control systems, data acquisition systems, and signal processing. This paper describes the integration of an array of 30 heated cantilevers into a commercial AFM to perform high speed and parallel topography imaging.

2. Array Fabrication and Calibration:

Figure 1 shows the main steps in batch fabricating an array of 30 heated cantilevers. The fabrication process is similar to previously published procedures for fabricating heated cantilevers, [26, 27] modified here to accommodate the large number of cantilevers and their electrical interconnects. The fabrication process started with a 100 mm-diameter silicon-on-insulator wafer with a 5 μm-thick silicon device layer, a 1 μm-thick buried oxide layer, and a 500 μm-thick silicon handle layer. First, the cantilever anchor beams and tip cylinders were shaped via inductively coupled plasma deep reactive ion etching (ICP-DRIE). Next, the tips were formed via a HNA (hydrofluoric acid 2%, nitric acid 95%, acetic acid 3%) isotropic wet etch and sharpened through dry oxidation [28]. The U-shaped cantilever was formed via ICP-DRIE until the buried oxide layer was exposed. The cantilever free-end was lightly doped ($\sim 10^{17}$ cm^{-3}) with phosphorus to form the resistive heater while the cantilever legs and anchors were heavily doped ($\sim 10^{20}$ cm^{-3}) with phosphorus to form current pathways such that the heater dissipated over 90% of cantilever power [26]. Electrical contacts that interfaced with the high-doped anchor beams were formed by sputtering 300 nm of gold with 10 nm of chromium as an adhesion layer, and patterning the leads via liftoff. The cantilevers were released by ICP-DRIE through the backside of the silicon handle layer followed by etching the sacrificial layer of silicon dioxide using hydrofluoric acid. A single 100 mm wafer produced 48 arrays of 30 heated cantilevers and 140 single heated cantilevers with the overall yield of 90% or higher.

Figure 2(a-b) show scanning electron microscope (SEM) images of an array of 30 heated cantilevers. A single array chip is 4.8 mm wide and 7 mm long. The tip-to-tip spacing between adjacent cantilevers is 85 μm. This spacing corresponds to the maximum distance that our AFM scanner can accommodate, such

that each cantilever tip will scan over its own field. A total of 60 metal leads, two for each cantilever, connect the cantilever anchor beams to 180 × 180 μm^2 metal pads for electrical access to each cantilever. The inset in figure 2(b) shows a zoomed view of a single cantilever. Each cantilever is about 1 μm-thick, has legs that are 100 μm long and 20 μm wide, and a heater of size 14 × 20 μm^2. The cantilever stiffness is about 0.65 N/m with a resonant frequency of about 50 kHz. Each cantilever free-end has a sharp tip having an apex radius of about 20 nm and height of about 1.5 μm.

We characterized the electrical and thermal properties of a cantilever array to enable the precise electro-thermal operation of the cantilevers. Figure 3(a) shows the steady cantilever heater temperature and electrical resistance as functions of total cantilever power. We calibrated the cantilever heater temperature by measuring the Stokes peak shift using a Renishaw InVia Raman microscope which is capable of spatial resolution near 1 μm and temperature measurement accuracy of about 1% [29]. The cantilever electrical resistance increases with temperature since the electrical resistivity of doped silicon is temperature dependent [30]. The cantilevers have a positive temperature coefficient of resistance up to a heater temperature of about 500 °C. Figure 3(b) shows the average cantilever current and resistance as functions of the applied cantilever voltage for all 30 cantilevers in the array. The error bars show the standard deviation in the measurements and the variation in the cantilever current and resistance are less than 1.6% and 4.8% respectively. These variations in cantilever properties arise from variations in the cantilever thicknesses due to limitations in the fabrication process. The trends shown in figure 3(b) are consistent for five different sets of measurements.

3. Experiments:

Figure 4 shows the hardware used to integrate cantilever arrays into a commercial AFM, an Asylum Research MFP-3D SA. Two custom printed circuit boards (PCBs) provided electrical access to the cantilevers while a custom AFM holder served as the connection adapter to the AFM. The array chip was glued onto the array adapter circuit board and the electrical leads on the array chip were wire-bonded to corresponding pads on the PCB. We cut the base of the standard AFM holder in the shape of the array

adapter board and secured the board to the holder using screws [19]. The modified AFM holder was mounted in the AFM. A 60 pin flex cable connected the array adapter circuit board to the array heating circuit board. The heating circuit for each cantilever consisted of the cantilever in series with a current-limiting sense resistor. Each heating circuit was controlled independently using dedicated data acquisition system (DAQ; National Instruments PXI 6368 and PXI 6733) channels to supply a constant voltage to the circuit and to measure the voltage across the sense resistor. A Labview program controlled the heating bias for each circuit and acquired the thermal topography signals in parallel.

Figure 5 shows the concept of thermal topography imaging using heated cantilevers [31]. The majority of the heat generated in the cantilever heater region flows to the substrate via conduction through the air between the cantilever and the substrate. The heat flow from the cantilever varies inversely with the thickness of the air-gap. When a constant voltage is applied to the cantilever circuit, the cantilever temperature varies inversely causing the cantilever voltage to vary with the distance between the cantilever and the substrate. Thus, the substrate topography can be measured by tracking the changes in the cantilever voltage as the cantilever scans the substrate. Since the thermal conductivity of air is at least two orders of magnitude smaller than that of most substrate materials, the thermal nanoimaging is not affected by the thermal conductivity of the substrate.

The cantilever temperature signal can be used to level the cantilever array onto a substrate [19, 32]. The cantilever temperatures and cantilever voltages drop rapidly as the cantilevers are brought closer to the substrate. The cantilever voltages drop slowly once the cantilevers snap into the substrate. The misalignment of the array can be measured by tracking the positions at which the tips snap into the substrate in the cantilever voltage signals. The array is leveled onto the substrate by adjusting the tilt of the AFM head until all cantilevers contacted the substrate simultaneously. Figure 5(b) shows the cantilever voltages upon successful leveling of the array. This technique obviates the need for the laser-photodetector setup used to engage cantilevers onto the substrate in typical AFMs.

In order to fully explore the imaging capabilities of our cantilever array, we designed and fabricated a special substrate which includes many microscale and nanoscale features. Figure 6 shows the (a) design

and (b) SEM image of the substrate, the design of which was based on the University of Illinois seal. The pattern consisted of three layers of nanostructures that were 25 nm, 35 nm, and 50 nm in height. The widths of the nanostructures ranged from 0.4 to 5.4 μm. The substrate was fabricated by growing a 110 nm thick layer of silicon oxide through dry oxidation followed by two steps of photolithography and CHF_3 reactive ion etching. The area within each black square represents the scan area for each cantilever which is limited by the scan range of the AFM stage to 90 μm × 90 μm. Since the tip-to-tip spacing of the array is 85 μm, the one dimensional 1 × 30 cantilever array can effectively image a continuous 90 μm × 2550 μm area simultaneously. Thus, the 510 μm × 425 μm substrate pattern was sliced into 6 rows which were placed end-to-end to form a 85 μm × 2550 μm pattern that matches the imaging capability of the array.

Each cantilever simultaneously scanned the substrate in contact-mode AFM, at a scanning speed of 226 μm/sec. We used the AFM force feedback on one cantilever in the middle of the array and minimized the force set-point to minimize tip-wear. The integral gain was reduced to 0.25 to ensure that the AFM force control only compensated for the out-of-plane slope of the substrate and did not respond to topographic structures on the substrate. The cantilevers were heated to about 450 ˚C by supplying a constant heating voltage. The thermal signals from each cantilever were simultaneously acquired by the DAQ at a sampling rate of 250 kHz. 80 raw data samples were averaged using a software routine to produce one topography pixel. The resulting 30 images were stitched together in a two-dimensional format to produce a composite AFM image.

Figure 7 shows a 510 μm × 425 μm (0.22 mm^2) AFM image of the substrate acquired simultaneously using the 30 cantilever array within 256 seconds. Each cantilever acquired a 1248 × 256 pixel image and the composite image has 7072 × 1209 pixels or 9.05 million pixels. The image has pixels of size 72.15 nm × 351.5 nm. This is a 678X improvement in throughput over conventional AFM which involves a single cantilever scanning the substrate at a scan speed of 10 μm/sec. The vertical lines in figure 7 are artifacts that occur when the tips momentarily lose contact with the substrate due to the low tip force set-point and the high scan speed.

Figure 8 shows consecutively expanded views of the AFM scan, scanning electron micrographs of the corresponding areas, and a line-scan view of a single scan. The thermal topography images show artifacts at the edges of vertical features typical of raw, unprocessed thermal topography signals [19, 31]. Thermal topography sensitivity is the change in the cantilever voltage per unit change in the topography height while the noise-limited vertical resolution is the smallest vertical displacement that can be resolved in the thermal topography signal. The topography sensitivity is 3.34 mV/nm and the noise-limited vertical resolution is 1.21 nm. The thermal topography signal was divided by the thermal topography sensitivity to obtain a height signal. The heights derived from the thermal signal match well with those from the laser-deflection signal with less than 1 nm error. Figure 9 compares the isometric views of the thermal AFM data and the corresponding SEM data. While both imaging techniques can provide high-resolution top-down views of millimeter-scale areas, only the thermal AFM image provides precise height information of the sub-100 nm tall nanostructures on the substrate.

4. Discussion:

Successful nanoimaging using cantilever arrays requires the optimization of several design choices at the component and system levels. Here we describe design considerations in the array geometry, force control, electronics, and software based on the constraints imposed by the AFM, DAQ, and the cantilever characteristics.

We fabricated the array with a cantilever pitch (85 μm) less than the scan range of the AFM (90 μm) so that we could acquire a continuous 90 μm × 2700 μm image of the substrate in one scan. In our previous work, we used an array of 5 cantilevers having a pitch of 110 μm which required us to scan more than once to acquire a continuous image of the substrate resulting in additional data acquisition and processing to form the composite image [19]. When an array of closely spaced cantilevers is heated, heat flows between adjacent cantilevers resulting in an unwanted cantilever temperature rise. This thermal crosstalk is negligible when cantilevers are operated near a substrate, since more than 98% of the cantilever heat flows into the substrate and the array chip instead of adjacent cantilevers [27]. Moreover,

since all cantilevers are operated at about the same temperature in thermal nanoimaging, the net heat flow between adjacent cantilevers is negligible. Closed loop control of cantilever temperature can be used to compensate any thermal crosstalk between cantilevers [19, 33].

The imaging experiments involved a tradeoff between tip-wear and tip-substrate traction. Since the cantilevers in the array do not have integrated actuators for force control, the remnant error from the array leveling process causes the cantilevers at the ends of the array to apply non-optimal tip-forces. The extent of error in the tip-force scales with the size of the array. Furthermore, the cantilevers in 30-cantilever array were 6 X stiffer (0.6 N/m) than those in our 5-cantilever array (0.1 N/m) due to limitations in the fabrication process. Thus, we operated the array with a force set-point that minimized tip-wear at the cost of tip-substrate traction. Figures 7-9 show data acquired after the array scanned the substrate 37 times with different tip force set-points and scan speeds of 50 - 250 μm/sec. The tip wear is noticeable in fig. 8 where the thermal topography features are wider than the actual features.

Currently, the imaging resolution and speed are limited by our measurement equipment. The limit on lateral resolution is governed by the tip radius (20 nm), and the vertical resolution is limited by the electronic noise of the cantilever (2 μV $Hz^{-1/2}$). Heated cantilevers and cantilever arrays can image surfaces at scan speeds up to 1 mm/sec without any deterioration in the thermal topography [19]. Compliant heated cantilevers enable fast scan speeds with minimal damage to the tip, substrate and without losing contact with the substrate [19]. Oversampling and post-processing the thermal topography signal became a necessity due to the inherent noise (10 mV) and the lack of built-in filtering in the measurement equipment. Although our DAQ is capable of acquiring data at 2 MHz, we were able to sample the thermal topography signals only at 250 kHz due to limitations in the DAQ software. Due to this restriction, we chose to improve the vertical resolution at the cost of scan speed and lateral resolution.

The array technology reported here can be scaled to much larger cantilever arrays by making some modifications at the system and component levels. First, the cantilevers would be configured as a compact 2D array instead of long 1D array to match the geometry of common substrates. Complex through-wafer vias become necessary to maintain a high areal density of cantilevers in 2D arrays, and to prevent

wirebonds from interacting with the substrate or ionic liquid mediums [10, 17]. The leveling technique used in this work can be extended to 2D arrays. Second, cantilever multiplexing techniques would have to be employed to cut down the number of data acquisition channels and wire-bonds necessary to interface with the arrays. Third, automated electronics would be necessary to acquire, parse, and filter data in real-time. High order low-pass filters could be used in lieu of oversampling and averaging data samples to improve topography resolution and to alleviate data acquisition problems. Fourth, cantilever stiffness should be minimized to minimize tip wear. Furthermore, the cantilevers could be integrated with ultrananocrystalline diamond tips to significantly lower tip wear and tip fouling compared to standard silicon tips [34, 35]. We note that it should still be possible to operate large 2D cantilevers in a commercial AFM without altering any component besides the cantilever holder.

The same array technology developed in this work could be used to improve the throughput of other applications of heated cantilevers such as material property measurement [6], nanomanufacturing [19, 20, 36-38], or data storage [10] through parallel and independent operation of cantilevers. Similar design ideologies can be used for cantilever arrays with different embedded sensors such as piezoresistive strain sensors [3, 39]. Finally, such array technology can be scaled to larger cantilever arrays to enable wafer-scale metrology and manufacturing thereby encouraging the widespread adoption of AFM in industry.

5. Conclusions:

We report the integration of a 1 × 30 array of heated cantilevers into a commercial AFM to perform parallel topography imaging. The array was fabricated based on a procedure used to fabricate single heated cantilevers. The thirty cantilevers in the array show nearly identical electro-thermal characteristics. Custom circuit boards were built and used to electronically interface with the array. The array acquired a 0.51 mm × 0.43 mm AFM image of a substrate at 226 μm/sec with 1.21 nm vertical resolution. The same array integration architecture can be used for nanomanufacturing and calorimetric applications.

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Figure 2: Scanning electron micrographs of an array of 30 heated microcantilevers. (a) Top-down view of the array chip showing the 60 aluminum leads and contact pads corresponding to the 30 cantilevers. (b) Isometric view of the array chip and expanded views of a few cantilevers. (Insets) Zoomed views for a single cantilever and cantilever tip apex.

Figure 3: Electrothermal properties of the cantilever array. (a) Cantilever heater temperature and electrical resistance as a function of cantilever power for a single cantilever in the array. (b) Cantilever current and electrical resistance as a function of cantilever voltage. The average current and resistance for all 30 cantilevers is plotted with the standard deviation plotted as the error bars.

Figure 4: Array integration hardware. The array was glued and wire-bonded to the array adapter printed circuit board (PCB) having electrical leads leading to a flex-cable connector. The array adapter PCB was secured onto a custom AFM holder which was mounted in the AFM. A flex-cable connected the array adapter PCB to heating circuit board that interfaced with the individual cantilever heating circuits and the data acquisition system (DAQ). The heating circuit for each cantilever consisted of the cantilever in series with a current-limiting sense resistor.

Figure 5: (a) Principle for thermal topography sensing. The thermal conductance from the cantilever varies inversely with the cantilever-substrate distance. The substrate topography is measured by tracking changes in the cantilever temperature signal. (b) Array leveling using the cantilever thermal signals. Cantilever voltages decrease rapidly as the cantilevers near the substrate and the voltages decrease slowly as the cantilevers push against the substrate. The array tilt is adjusted until all

cantilevers contact the substrate simultaneously causing the voltage signals of the cantilevers to overlap. The graphs show voltage signals from selected cantilevers and the cantilevers are numbered from left to right in the 30-cantielver array.

Figure 6: Substrate used to demonstrate parallel topography imaging. (a) Schematic of the substrate pattern consisting of three layers of different heights. The 2D substrate pattern was sliced into 6 rows which were laid end-to-end such that each cantilever imaged a unique portion of the substrate simultaneously. (b) Scanning electron micrographs of the substrate with silicon oxide nanostructures.

Figure 7: A 0.510 mm × 0.425 mm composite AFM image consisting of 9.05 million pixels, acquired simultaneously with 30 cantilevers. The array scanned the substrate in contact-mode AFM at 226 μm/sec and the image was acquired in 256 seconds. Each cantilever scanned a 90 μm × 90 μm area and the resulting 30 scans were stitched to make the complete image.

Figure 8: (a) Successively expanded AFM topography images and corresponding scanning electron micrographs from fig. 7 showing the high lateral resolution of the AFM image. Each topography pixel of the image is of size 72.15 nm × 351.5 nm. (b) Laser-deflection based height and the thermal topography signals at a section of the substrate shown in (a) (top-left AFM image). The noise-limited vertical resolution of the thermal signal is 1.21 nm.

Figure 9: Isometric views of the substrate in fig. 7 obtained using the thermal AFM image and SEM. The thermal AFM image provides precise height information of sub-100 nm tall nanostructures unlike the SEM image.

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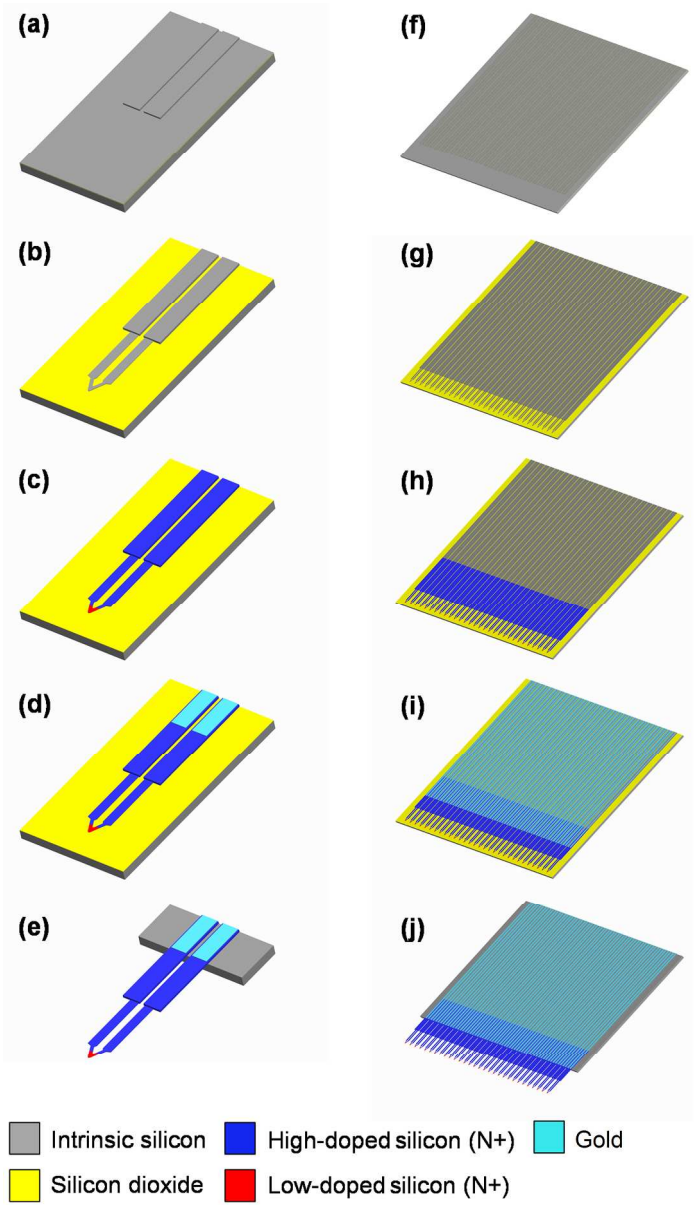

Figure 1: Fabrication process flow for (a-e) a single cantilever and (f-j) an array of 30 heated cantilevers. Fabrication begins with a silicon-on-insulator (SOI) wafer. (a,f) Anchor and tip cylinder formation via inductively coupled plasma deep reactive etching (ICP-DRIE). (b,g) Tip formation via oxidation sharpening and cantilever formation using ICP-DRIE. (c,h) Low dosage and high dosage phosphorous doping steps. (d,i) Gold metallization for electrical contacts. (e,j) Backside ICP-DRIE and hydrofluoric acid wet etch for the final device release.
529x918mm (96 x 96 DPI)

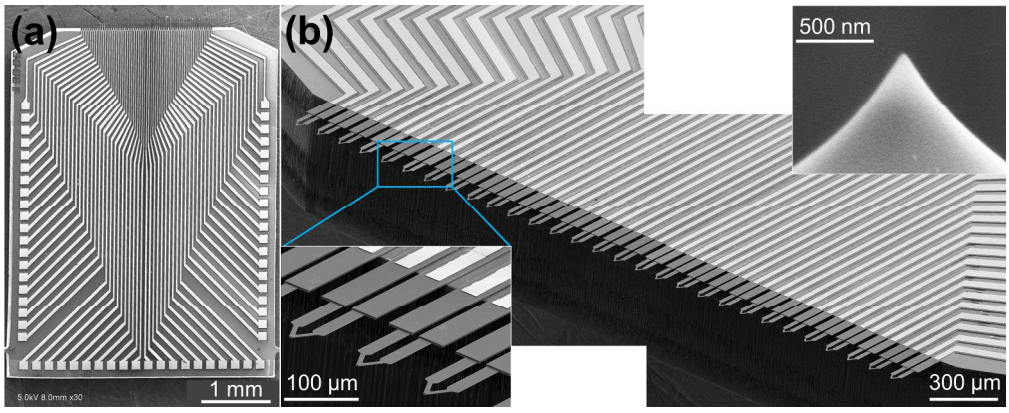

Figure 2: Scanning electron micrographs of an array of 30 heated microcantilevers. (a) Top-down view of the array chip showing the 60 aluminum leads and contact pads corresponding to the 30 cantilevers. (b) Isometric view of the array chip and expanded views of a few cantilevers. (Insets) Zoomed views for a single cantilever and cantilever tip apex.
847x338mm (150 x 150 DPI)

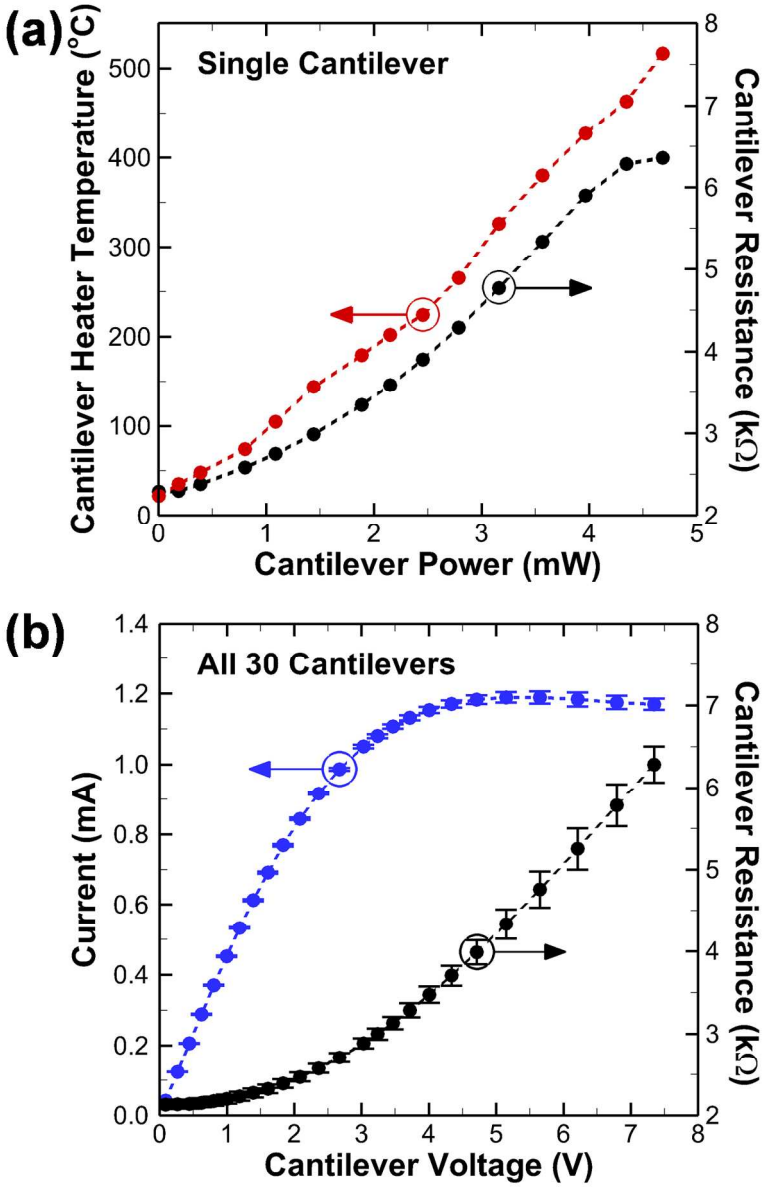

Figure 3: Electrothermal properties of the cantilever array. (a) Cantilever heater temperature and electrical resistance as a function of cantilever power for a single cantilever in the array. (b) Cantilever current and electrical resistance as a function of cantilever voltage. The average current and resistance for all 30 cantilevers is plotted with the standard deviation plotted as the error bars.
304x474mm (300 x 300 DPI)

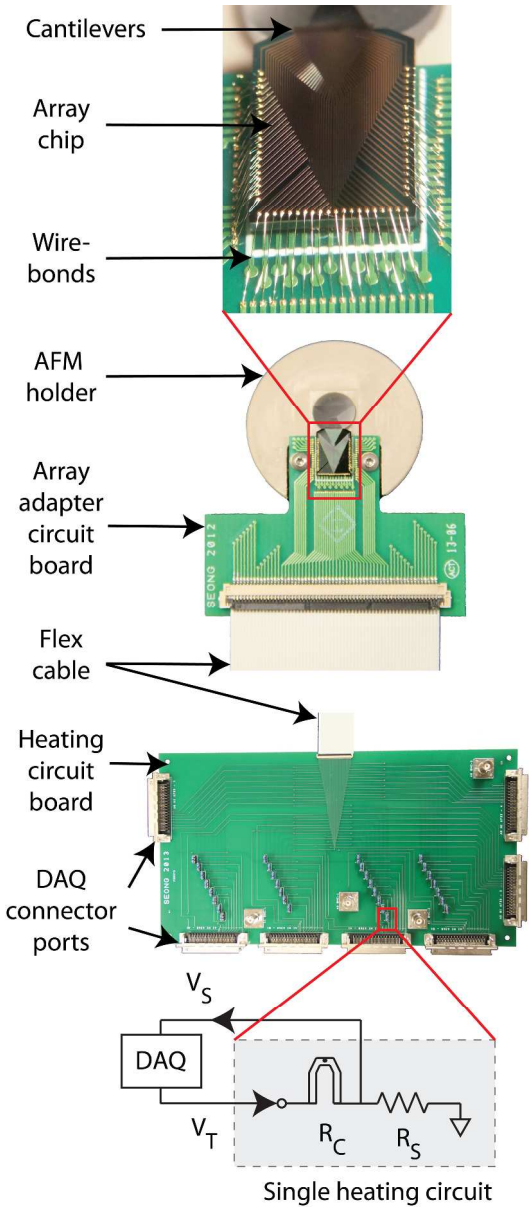

Figure 4: Array integration hardware. The array was glued and wire-bonded to the array adapter printed circuit board (PCB) having electrical leads leading to a flex-cable connector. The array adapter PCB was secured onto a custom AFM holder which was mounted in the AFM. A flex-cable connected the array adapter PCB to heating circuit board that interfaced with the individual cantilever heating circuits and the data acquisition system (DAQ). The heating circuit for each cantilever consisted of the cantilever in series with a current-limiting sense resistor.
324x742mm (300 x 300 DPI)

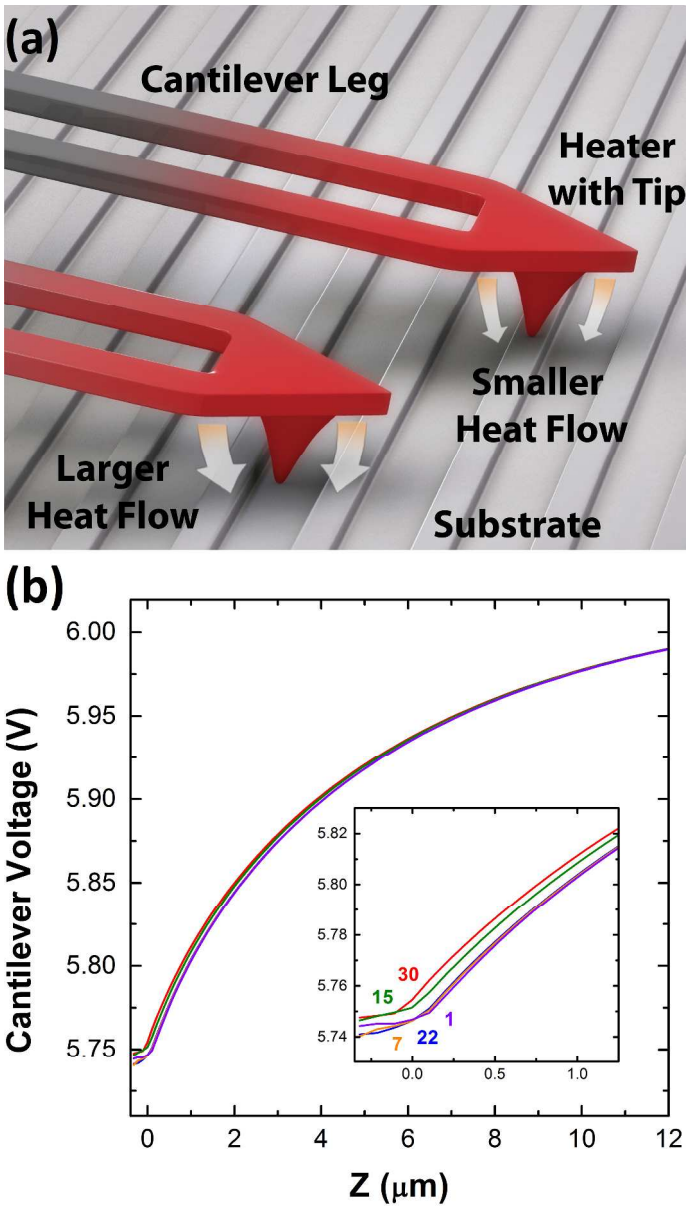

Figure 5: (a) Principle for thermal topography sensing. The thermal conductance from the cantilever varies inversely with the cantilever-substrate distance. The substrate topography is measured by tracking changes in the cantilever temperature signal. (b) Array leveling using the cantilever thermal signals. Cantilever voltages decrease rapidly as the cantilevers near the substrate and the voltages decrease slowly as the cantilevers push against the substrate. The array tilt is adjusted until all cantilevers contact the substrate simultaneously causing the voltage signals of the cantilevers to overlap. The graphs show voltage signals from selected cantilevers and the cantilevers are numbered from left to right in the 30-cantielver array.
958x1689mm (96 x 96 DPI)

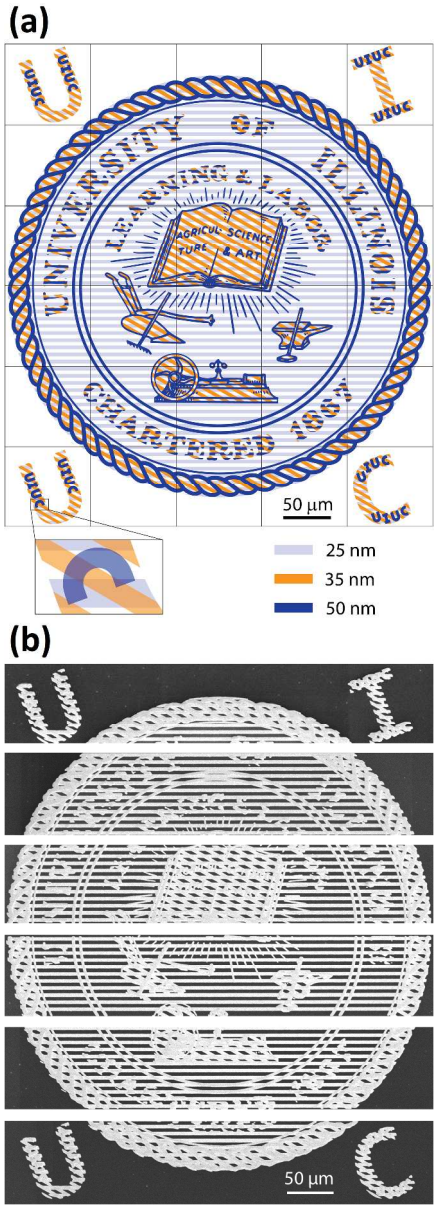

Figure 6: Substrate used to demonstrate parallel topography imaging. (a) Schematic of the substrate pattern consisting of three layers of different heights. The 2D substrate pattern was sliced into 6 rows which were laid end-to-end such that each cantilever imaged a unique portion of the substrate simultaneously. (b) Scanning electron micrographs of the substrate with silicon oxide nanostructures.
176x493mm (300 x 300 DPI)

Figure 7: A 0.510 mm × 0.425 mm composite AFM image consisting of 9.05 million pixels, acquired simultaneously with 30 cantilevers. The array scanned the substrate in contact-mode AFM at 226 μm/sec and the image was acquired in 256 seconds. Each cantilever scanned a 90 μm × 90 μm area and the resulting 30 scans were stitched to make the complete image.
536x676mm (96 x 96 DPI)

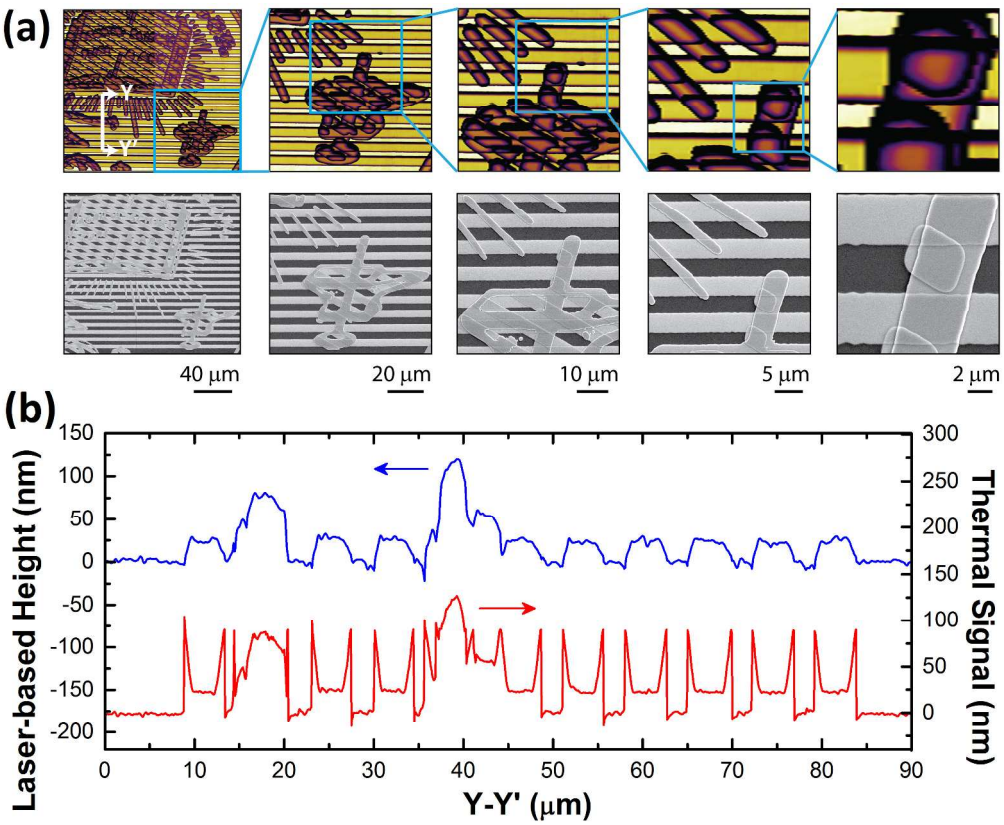

Figure 8: (a) Successively expanded AFM topography images and corresponding scanning electron micrographs from fig. 7 showing the high lateral resolution of the AFM image. Each topography pixel of the image is of size 72.15 nm × 351.5 nm. (b) Laser-deflection based height and the thermal topography signals at a section of the substrate shown in (a) (top-left AFM image). The noise-limited vertical resolution of the thermal signal is 1.21 nm.
878x720mm (96 x 96 DPI)

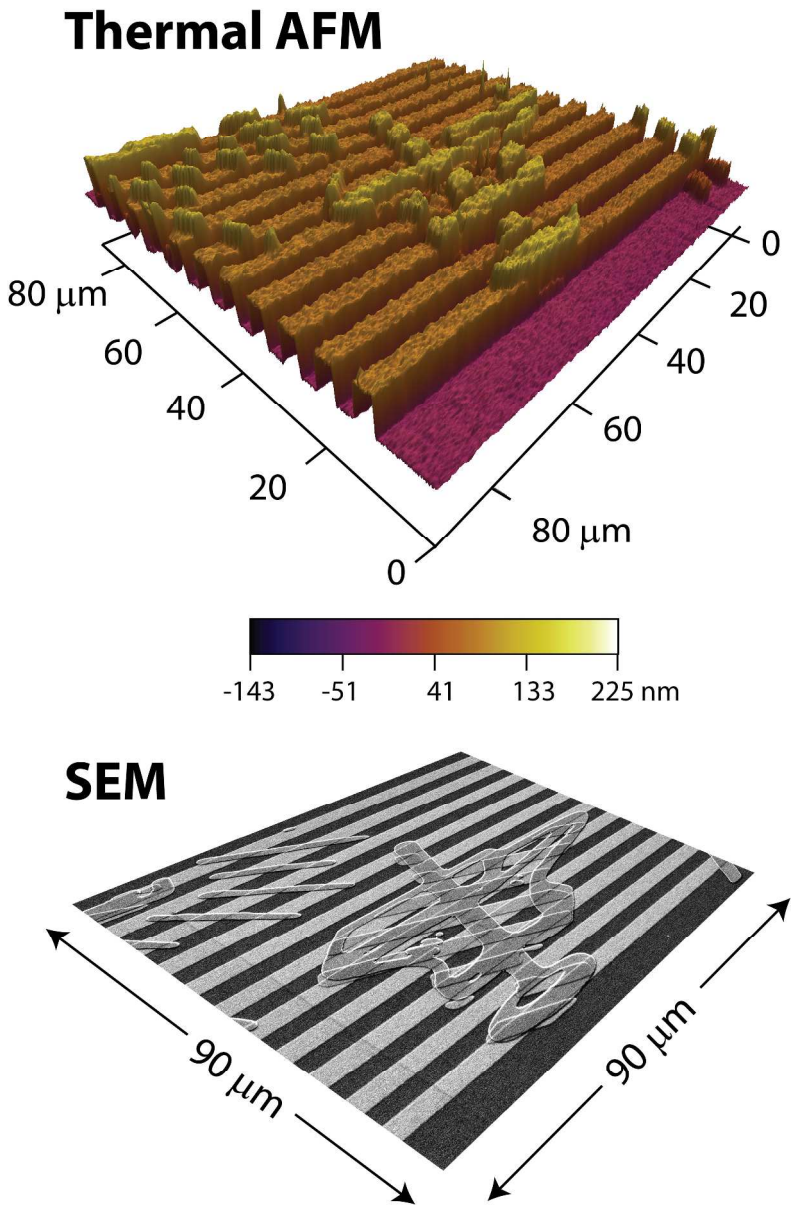

Figure 9: Isometric views of the substrate in fig. 7 obtained using the thermal AFM image and SEM. The thermal AFM image provides precise height information of sub-100 nm tall nanostructures unlike the SEM image.
434x665mm (150 x 150 DPI)