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Wet Etching Processes for Recycling Crystalline Silicon Solar Cells from End-of-life Photovoltaic Modules

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The ideal approach for disposing of end-of-life photovoltaic (PV) modules is recycling. Since it is expected that more than 50,000 t of PV modules will be worn out in 2015, the recycling approach has received significant attention in last few years. In order to recover Si wafers from degraded solar cells, metal electrodes, anti-reflection coating, emitter layer, and p-n junction have to be removed from the cells. In this study, we employed two different chemical etching processes to recover Si wafers from degraded Si solar cells. Each etching process consisted of two steps: (1) first etching carried out using a nitric acid (HNO₃) and hydrofluoric acid (HF) mixture and potassium hydroxide (KOH), (2) second etching carried out using phosphoric acid (H_3PO_4) and a HNO₃ and HF mixture. The first etching process resulted in deep grooves, 36 µm in average, on the front of recycled wafers that rendered the process unsuitable for wafers to be used in solar cell production. Such grooves were occurred due to different etching rate of Ag electrodes and silicon nitride (SiN_x). On the other hands, the second etching process did not result in such grooves and produced the recovered Si wafer with uniform and smooth surface. The recycled wafers obtained by the second etching process showed properties almost identical to those of commercial virgin wafers: thickness, 173μ m; minimum and maximum resistivity, 1.6 and 10 Ω -cm, respectively; and average carrier lifetime, 1.785 μ s. In addition, P and Al atoms were not detected in the recycled wafers by secondary ion mass spectroscopy.

1. Introduction

Crystalline silicon (c-Si) solar cells have a leading position in the photovoltaic (PV) market, and c-Si modules have been widely accepted and installed worldwide. Till 2012, the total amount of global PV module installations is more than 100 GW. Moreover, the annual PV module installation in 2013 was about 30 GW, and it is expected to double in 2020. With the increase in PV installations, the disposal of end-of-life PV modules has become an important environmental issue. Wambach et al. estimated that more than 50,000 t of PV modules will be worn out in 2015 [1]. Therefore, it is important to find ways for disposing of these end-of-life PV modules. One of the most ideal approaches would be to reuse the modules. There have been many reports describing the requirements for carrying out end-of-life module recycling [2 - 6]. The various components of a module that can be reused are the Al frame, junction box, cover glass, and solar cells. Among these, the Al frame and junction box can be easily dismantled mechanically and can be directly reused. However, specific treatments are required to recycle degraded solar cells, and these treatments are complicated. However, Si is the most important and valuable

material in PV modules and is recoverable from degraded cells [7]. In some cases, degraded solar cells are crushed into a powder form and used for ingot production [8]. However, the energy consumption during a standard module production process is approximately more than four times that during module production using recycled wafers [9]. In addition, since wafers account for more than 60% of the solar cell cost, the cost of PV modules can be further reduced using recycled wafers for fabricating the modules. While several researchers have reported methods for recovering Si wafers from degraded solar cells, there has been no report on a viable recycling method for such cells. In this research, we conducted two different chemical etching processes for recycling degraded c-Si solar cells and confirmed the validity of the processes. The validity of the processes was confirmed by comparing the qualities of recycled wafers with those of commercial virgin wafers.

2. Experimental

In this research, 6-in monocrystalline Si solar cells with three bus bars were subjected to etching. The thickness of the cells was 200 μ m with a 30- μ m-thick Al back contact. In order to recover Si wafers for reuse in the production of new PV cells, the metal electrodes (both Ag and Al), anti-reflection coating (ARC), emitter, and p–n junction had to be removed. The Al frame was removed by a mechanical process, and the EVA and back sheet were removed by a thermal process [10]. Since our focus is only on the chemical methods of recycling c-Si solar cells, the thermal processes is not discussed in detail. Two different etching processes were conducted and their efficiencies were compared.

The first etching process (etching process #1) consisted of two steps: (1) simultaneous removal of Ag electrodes, ARC, emitter layer, and p-n junction by using an etching solution mixed with 60% nitric acid (HNO₃) and 49% hydrofluoric acid (HF) (mixing ratio in vol%: 4:1) at room temperature , and (2) removal of the Al electrode from the rear side of the cells using 30% potassium hydroxide (KOH) at 80°C. The first etching step (HNO₃ + HF etching) was conducted for 60 s, and the second etching step (KOH etching) was conducted for 6 min. These etching steps were carried out under conditions optimized on the basis of previous experiments. The second etching process (etching process #2) also consisted of two steps: (1) silicon nitride (SiN_x) , which is the ARC layer, and Al back contact, was etched using 90% phosphoric acid (H₃PO₄) at 160°C for 60 min, and (2) the Ag electrodes, emitter layer, and p-n junction were etched using the HF+HNO₃ mixed solution for 60 s, as mentioned above. These etching steps were also carried out under conditions optimized on the basis of previous experiments.

Scanning electron microscopy (SEM) with energy dispersive X-ray spectroscopy (EDX) was employed to investigate the surfaces and thickness of recycled Si wafers. After complete etching, the resistivity of recycled wafers was measured using a four-point probe. Secondary ion mass spectroscopy (SIMS) was carried out to measure the doping concentration of recycled cells. The carrier lifetime of the wafers was measured using micro-wave detected photoconductance decay (PCD).

3. Results and discussion

In order to fabricate recycled c-Si solar cells using recycled wafers obtained from end-of-life PV modules, the properties of the recycled wafers should be identical or nearly identical to those in their virginal condition. To meet this requirement, it is necessary to remove Ag electrodes, ARC, emitter, p–n junction, and Al electrode from the cells. First, Ag electrodes on the front surface of the cells should be perfectly removed. The etching results for the sample subjected to etching process #1 are shown in Figure 1. It shows the SEM image of the area (with a T shape) where a bus bar and finger existed, and Figure 1 (b) shows the EDX analysis result for this area. Ag electrodes were etched by HNO₃ in the HF + HNO₃ mixed solution. EDX analysis was carried out to detect the amount of unremoved Ag on the front

surface of the cells. As can be seen in Figure 1 (b), only Si but no Ag was detected. This implies that Ag electrodes were totally removed by etching process #1.



Fig. 1 (a) SEM image of recycled wafer subjected to etching process #1, and (b) EDX analysis results for this wafer.

The SEM image of the sample (Figure 2 (a)) subjected to etching process #2 is different from that shown in Figure 1 (a). It can be seen that the T shape observed Figure 1 (a) is not present here and that the etched surface is more uniform than that of the sample subjected to etching process #1. However, the EDX analysis results shown in Figure 2 (b) are similar to those shown in Figure 1 (b): no Ag but only Si is detected. Therefore, it can be concluded that Ag electrodes were entirely removed by etching process #2.



Fig. 2 (a) SEM image of recycled wafer subjected to etching process #2, and (b) EDX analysis results for this wafer.

In order to investigate the different surface conditions of the samples shown in Figure 1 (a) and 2 (a), the cross-section of the samples was analyzed by SEM. For this analysis, the sample cross-section (marked as a red dashed line in Figure 3 (a), which is top view of the sample) underneath the location of the Ag finger was observed. As can be seen in Figure 3 (b), the T-shaped area is a groove on the front surface of the cells. This groove was formed under the location of the Ag finger during etching process #1.

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Fig 3 SEM images of sample subjected to etching process #1 (a) top view of sample and (b) cross-section of sample.

The depth of the grooves on the recycled wafer surfaces is listed in Table 1. If these grooves are not too deep, they are not an issue during the recycling of solar cells. This is because shallow grooves can be removed by several methods such as chemical mechanical polishing (CMP). The depth of the grooves in each sample was calculated as the average of the depth measured at five different points on the cell surface.

	Etched wafer #1	Etched wafer #2	Etched wafer #3
Groove depth	39 µm	32.7 µm	37.4 μm

Table 1 Depth of grooves formed on recycled wafers subjected to etching process #1.

It can be deduced from Table 1 that the groove depth is (~36 μ m) around one-fifth of the total wafer thickness. Therefore, it is required to grind the wafer by more than 40 μ m in order to obtain recycled wafers without any patterns on the surface. The expected final wafer thickness after grinding would be 130 μ m. Such a low wafer thickness is not sufficient to fabricate recycled solar cells using wafers. This is because such thin wafers have a high possibility of cracking; moreover, such wafers show low photocurrent. More importantly, current c-Si solar cell fabrication processes, which are optimized for 200- μ m-thick Si wafers, cannot be employed for such thin wafers. Therefore, it can be concluded that etching process #1 is not suitable for fabricating recycled c-Si wafers from end-of-life PV modules.

The procedure for etching process #1 and the mechanism of groove formation are shown in Figure 4. It shows the etching stages of a c-Si wafer solar cell etched using a HF + HNO₃ etching solution. Moreover, the mechanism of groove formation during the etching is also shown. Figure 4 (a) shows the cross-section of the cell in its initial form. As can be seen, SiN_x is located on the emitter, and the Ag electrode is in contact with the emitter layer. When the cell is dipped in the HF + HNO₃ solution, the Ag electrode is etched faster than SiN_x . This is because in the HF + HNO₃ solution, the etching rate of Ag is much faster than that of SiN_x . Therefore, the Ag electrode is dissolved more than SiN_x , as seen in Figure 4 (b).

Subsequently, the etching solution starts to etch the emitter layer while SiN_x is still remaining (Figure 4 (c)). Owing to the faster consumption of Ag in the solution, the area of the emitter layer underneath the Ag electrode starts to be etched even when SiN_x is not totally dissolved.



Fig. 4 Procedure for etching process #1 and mechanism of groove formation on front sample surface.

Figure 5 shows the etching procedure for etching process #2. First, SiN_x is etched by the H_3PO_4 solution at 160 °C, as shown in Figure 5 (b). Simultaneously, the Al electrode on the rear cell surface is also etched. After H_3PO_4 etching, the sample is dipped in an HF + HNO₃ etching solution. Both the Ag electrode and emitter are dissolved by the solution during this stage, as shown in Figure 5 (c). Finally, the recycled wafer without any grooves on the surface is obtained.



Fig. 5 Procedure for etching process #2.

SEM images of top view and cross-section of the sample subjected to etching process #2 are shown in Figure 6 (a) and (b). As can be seen in the Figure 6 (a), unlike etching process #2, smooth and uniform surface was achieved by etching

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process #2. We also investigated the cross-section of the sample and found that no grooves are produced on the front surface of the sample as well as the Al layer on the rear side of the sample is well etched. Therefore, we are able to achieve the groovefree recycled wafer using etching process #2.



Fig. 6 SEM images of sample subjected to etching process #2 (a) top view of sample and (b) cross-section of sample.

Table 2 lists the final thickness and resistivity of the recycled wafers after etching process #2. As mentioned above, to obtain a suitable final thickness of recycled wafers was an important prerequisite in this experiment in order to employ current c-Si solar cell fabrication processes and prevent possible cracks caused by a low thickness. As can be seen in the table, the average final thickness of the recycled wafers was approximately 175 µm and the etching rate of Si in the HF + HNO₃ solution was 0.2 μ m s⁻¹. Since etching process #2 was carried out for 60 s, we estimated that a total of 24 µm (12 µm each from the front and rear sides) of Si might have been etched. This value agreed well with our estimation of the etched Si amount. The resistivity of wafers is an important parameter for estimating the properties of initial wafers. In order to estimate the initial electrical properties of the recycled wafers, we measured the wafer resistivity and compared the obtained values with those of virgin wafers. As can be seen in the table, the minimum and maximum resistivity of the recycled wafers was 1.6 and 10.1 Ω cm, respectively. Although the resistivity of commercial virgin wafers varies with the wafer make, the average resistivity of virgin wafers lies in the range 1-10.1 Ω cm. The measured resistivity of three recycled wafers subjected to etching process #2 was close to the resistivity of commercial virgin wafers. Thus, we were able to obtain recycled wafers with resistivity nearly equal to that of commercial virgin wafers.

	Comm ercial virgin wafer	Recycl ed wafer #1	Recycl ed wafer #2	Recycl ed wafer #3	Recycl ed wafer #4	Recycl ed wafer #5
Final thicknes s	200 μm ± 10 μm	$\begin{array}{c} 175 \ \mu m \\ \pm \ 10 \\ \mu m \end{array}$	173 μm ± 10 μm	176 μm ± 10 μm	175 μm ± 10 μm	175 μm ± 10 μm
Resistivi ty	1–10 Ω·cm	2.2–10 Ω·cm	3.1–9.8 Ω·cm	1.6– 3.48 Ω·cm	3.4- 10.1 Ω· cm	2.5- 8.98 Ω· cm

Table 2 Thickness and resistivity of recycled wafers.

SIMS analysis was conducted to determine the concentration of P and Al in the recycled Si wafers. During the fabrication of c-Si solar cells, P atoms diffuse to the front surface of p-type Si wafers to form a p-n junction and an emitter layer. Similarly, an Al layer is deposited on the rear surface of p-type Si wafers to form the rear electrode as well as a back surface field (BSF) as Al atoms diffuse to the Si bulk. However, the emitter, p-n junction, Al rear electrode, and BSF must be removed to obtain recycled wafers from the cells. In other words, P and Al atoms must not be detected by SIMS measurements. For this reason, the concentrations of P and Al on the front and rear surfaces, respectively, were measured by SIMS. Figure 7 (a) shows the P concentration on the front surface of the recycled wafers, and Figure 7 (b) shows the Al concentration on the rear surface of the recycled wafers. As can be seen in the figure, P and Al were hardly detected on the front and rear wafer surfaces, respectively, throughout the penetration depth. For both surfaces, weak P and Al peaks were detected, but these small and weak peaks were more like noises. Therefore, it can be concluded that the emitter layer, p-n junction, Al rear electrode, and BSF were totally removed by etching process #2.



Fig. 7 SIMS analysis results (a) P concentration on the front surface and (b) Al concentration on the rear surface of recycled wafers.

The carrier lifetime of the recycled wafers was determined, and the obtained values were compared with that of commercial virgin c-Si wafers. The wafers were subjected to HF cleaning before the measurement, which was carried out without any passivation on both surfaces. The carrier lifetime of most commercial solar-grade crystalline Si wafers is in the range 1-3µs [11]. Figure 8 shows the carrier lifetime mapping results for the recycled wafers. Carrier lifetime is an important factor in the evaluation of virgin wafers. In this research, the carrier lifetime of the recycled wafers was measured without surface passivation by microwave PCD (WT-2000, SEMILAB). It can be seen in Figure 8 that the average carrier lifetime of the recycled wafers is 1.785 µs, which is close to that of commercial wafers. Therefore, it can be concluded that etching process #2 can be used to produce virgin-like recycled wafers from degraded c-Si solar cells.



Fig. 8 Carrier lifetime mapping results for recycled wafers.

Figure 9 shows an image of the final product of a recycled wafer. As can be seen, the recycled wafer obtained by etching process #2 had a smooth surface. The surface condition of the wafer was nearly identical to that of a commercial crystalline Si wafer after removal of saw damage by KOH.



Fig. 9 Image of a recycled wafer obtained by etching process #2.

Conclusions

In this research, we carried out two different etching processes for recycling degraded c-Si solar cells obtained from end-of-life PV modules. In order to obtain recycled wafers from degraded c-Si solar cells, metal electrodes, ARC, emitter layer, and p-n junction were removed by subjecting the cells to etching processes #1 and#2. We found that etching process #1, which consisted of HNO₃ + HF and KOH etching processes, resulted in grooves on the front surface of the recycled wafers owing to different etching rates of Ag electrodes and SiN_x in the HNO₃ + HF mixture. The depth of the grooves was about 36 µm. Recycled wafers with such deep grooves cannot be used in the fabrication of c-Si solar cells. Therefore, we concluded that etching process #1 is not suitable for obtaining recycled wafers. Further, we found that etching process #2 did not result in such grooves on the surface of the recycled wafers and that the wafers showed properties nearly identical to those of commercial virgin wafers. The final thickness of the recycled wafers obtained by etching process #2 was 173 µm, which is enough for employing current solar cell production processes for these wafers. In addition, the minimum and maximum resistivity of these wafers was 1.6 and 10 Ω cm, respectively, and their average carrier lifetime was 1.785 µs. These values are almost equal to those for commercial virgin wafers. In

addition, P and Al atoms were not detected in these wafers by SIMS analysis. Therefore, it can be concluded that etching process #2 can be used to produce virgin-like recycled wafers from degraded solar cells.

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Notes and references

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