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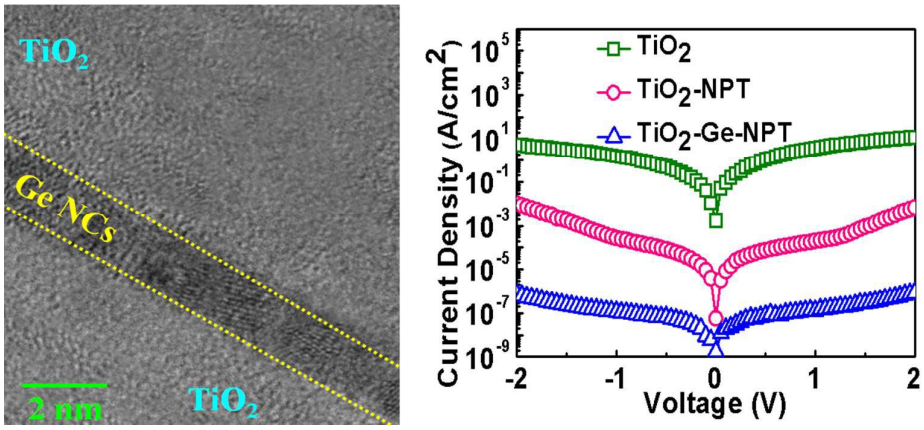

Leakage current suppression of TiO_2-based MIM capacitors by introducing plasma treatment and embedding Ge nanocrystals.

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TiO_2-based MIM capacitors featuring suppressed leakage current by embedding Ge nanocrystals

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With Pd as electrode, crystalline TiO_2-based MIM capacitors were found to demonstrate improved leakage current by adopting nitrogen plasma treatment due to the passivation of grain boundary related defects. Through the introduction of Ge nanocrystals into crystalline TiO_2, the leakage current can be further suppressed by more than 3 orders to 1.1×10^{-7} A/cm^2 at -1 V while maintaining a high capacitance density of 25.2 fF/μm^2. The major role of nanocrystals is to trap electrons and then suppress leakage current by inducing Coulomb blockade effect or building an internal field to compensate the applied external field. The MIM capacitor technology not only exhibits the prominent performance which is advantageous over other TiO_2-based capacitors, it also possesses the capability to implement low-leakage/high-reliability analog and mixed signal MIM capacitors for next generation circuits.

Metal-insulator-metal (MIM) based capacitors have been recently perceived as feasible passive components for radio frequency (RF), analog and mixed signal (AMS) integrated circuits (ICs). Unlike the applications to DRAM, in addition to meet the requirement of leakage current and capacitance, MIM capacitors for AMS applications also require good voltage linearity, low temperature coefficients and small loss tangent, tiny capacitance change under stress. Conventionally, to achieve AMS MIM capacitors with high capacitance, it occupies a large portion of chip area by employing Si_3N_4 or SiO_2 as the dielectric. Shrinking the thickness of these dielectrics may be beneficial to attain a higher capacitance density. However, it comes at the cost of deteriorated leakage current which will prevent the dielectrics from further applications. With the advent of high-permittivity (high-κ) dielectric, the requirement of large area to implement high-capacitance capacitors is relieved. The flourishing development of high-κ dielectric has ushered in a new era for high-performance MIM capacitors. Among many promising high-κ dielectrics, TiO_2 has long attracted intensive interest because its rutile phase enjoys a high κ value in the range of 90~170, depending on the crystallization orientation. Even with the potential to achieve a high κ value, one inherent material property that limits TiO_2 from further application in MIM capacitors is its high electron affinity which consequently results in high leakage current. Therefore high work function (WF) electrode is always employed for TiO_2-based MIM capacitors to suppress leakage current. In addition, doping TiO_2 with specific metal element has been proposed as an alternative approach to improve its leakage performance such as TiO_2-LaAlO,[1] TiTaO,[2] TiNiO,[3] TiHfO,[4] TiZrO,[5] TiPrO,[6] and $Sr_xTi_yO_z$,[7]. Although doped TiO_2 yields inspiring results, maintaining the dopant uniformity requires rigorous process control. Furthermore, reduced leakage can also be obtained by stacking another dielectric with larger band gap such as SiO_2/TiO_2 stack.[8] However, the capacitance density will be inevitably compromised because a larger band gap dielectric usually accompanies a lower κ value.

In this work, significantly improved leakage current performance for TiO_2-based MIM capacitors can be accomplished by introducing Ge nanocrystals into TiO_2. Embedding nanocrystals in dielectrics have been widely adopted in the technology of charge trap flash memory since nanocrystals offer a large amount of trapping sites which allow electron storage. Although memory effect is not the required function for MIM capacitors in AMS applications, the main reason to introduce nanocrystals is to utilize the trapped electrons to induce the so-called Coulomb blockade effect or build an internal field to compensate the applied external one, and therefore reduced leakage current can be expected. Recently, how the nanocrystal size affects dielectric behavior has been studied by investigating the sample with SiO_2 embedded with Ge nanocrystals.[9] The research provides a clear understanding of the quantum size effect of nanocrystals on capacitance. However, leakage current reduction pertinent to nanocrystal incorporation has never been explored in the literature. The results in this work prove the idea by demonstrating a relatively high capacitance density of 25.2 fF/μm^2 with leakage current of 1.1×10^{-7} A/cm^2 at -1 V, which is lower than capacitors without incorporating Ge nanocrystals by a factor of more than 3000. Aside from ameliorated leakage performance, capacitors with Ge nanocrystals also exhibit a small loss tangent of 0.020, a low temperature coefficient of capacitance (TCC) of 88 ^{o}C/ppm, and enhanced reliability in terms of a small capacitance change of 1.04 % under -1.5 V constant voltage stress after 10-year operation.

SiO_2 on Si was used as the starting material to form MIM capacitors. 50-nm Pd was first deposited as the bottom electrode and

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the reason to adopt Pd lies in its relatively high WF of 5.1 eV. Then 29-nm TiO_2 film was deposited as the dielectric of capacitors (denoted as TiO_2 sample). Next, rapid thermal annealing (RTA) of 500 °C was performed to crystallize TiO_2. To explore the impact of Ge nanocrystals incorporation on electrical characteristics, aforementioned 29-nm TiO_2 was replaced with TiO_2/Ge/TiO_2 laminate structure of 11.5/1.5/11.5 nm for some samples (denoted as TiO_2-Ge sample). With the same RTA condition,[10] Ge nanocrystals embedded in the crystalline TiO_2 was formed for TiO_2-Ge sample. Next, nitrogen plasma treatment (NPT) at 300 °C was performed for 1 min on some samples to investigate how nitrogen radicals affect device performance. Finally 50-nm Pd patterned with a size of 100 μm×100 μm was formed as the top electrode. Besides electrical characterization, transmission electron microscopy (TEM) and x-ray photoelectron spectroscopy (XPS) were also used to respectively confirm the formation of nanocrystals and the bonding structure of the annealed film.

Fig. 1(a) shows the cross-sectional TEM image of a TiO_2-Ge-NPT sample and nanocrystals with the size of ~1.5 nm can be clearly observed between top and bottom TiO_2 after annealing. To further analyze the bonding structure of the nanocrystals, XPS was performed and the result is displayed in **Fig. 1(b)**. As can be seen from the Ge 3d spectrum, the peak at the binding energy of 29.1 eV corresponds to the Ge-Ge bonding while the smaller peak at 32.0 eV can be assigned as GeO_x. Although GeO_x exists, the fraction is small since the area of Ge-Ge peak is much higher than that of GeO_x. The result implies that the nanocrystals shown in the TEM image are mainly composed of Ge. The formation of small amount GeO_x is reasonable because the electronegativity of Ge is larger than that of Ti and therefore it is relatively difficult for Ge atoms to obtain O atoms from pre-existed TiO_2.

Fig. 2 shows the capacitance-voltage (C-V) characteristics for samples with different process conditions measured at 10 k and 1 MHz. At 0 V, TiO_2 samples display the highest capacitance density of 33.8 fF/μm^2 (EOT of 1.02 nm) while the value for TiO_2-NPT and TiO_2-Ge-NPT samples decrease to 30.2 fF/μm^2 (EOT of 1.14 nm) and 25.2 fF/μm^2 (EOT of 1.37 nm) respectively, where EOT denotes equivalent oxide thickness. The κ value of TiO_2 is 110.8 which implies the formation of crystalline dielectric after RTA. With NPT, the value slightly decreases to 99.0 which is due to the formation of TiON.[7] With additional incorporation of Ge nanocrystals, the κ value further drops to 75.5 because Ge has a much smaller κ value than TiO_2. Besides the κ value evolution for different process conditions,

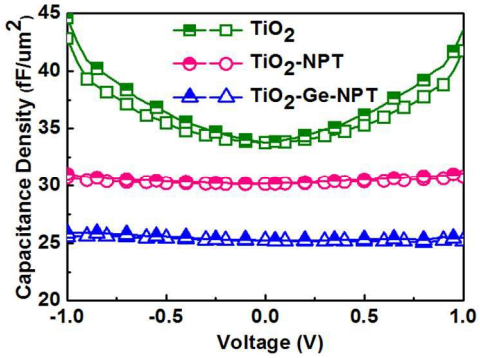

Fig. 2 C-V characteristics for TiO_2-based MIM capacitors with various process conditions measured at 10 k and 1 MHz. Half-up symbol is for 10 kHz.

it is also found that NPT process significantly mitigates the dependence of capacitance on applied voltage for TiO_2 samples which makes the capacitors more feasible in circuit applications and it can be ascribed to the passivation of grain boundary-induced defects in crystalline TiO_2 by nitrogen radicals.[8] Much improved frequency dispersion on capacitance for NPT-processed samples is mainly ascribed to the reduction of vacancies-induced mobile charges due to the passivation effect.

Based on the same mechanism, as the current-voltage (I-V) curves shown in **Fig. 3(a)**, TiO_2-NPT samples demonstrate reduced leakage current by a factor of 3652 as compared to TiO_2-samples at bias voltage of -1 V. Note that the current shown in the figure was measured by sweeping the voltage from zero to positive or negative bias. With Ge nanocrystals embedded in the TiO_2, for TiO_2-Ge-NPT samples, the leakage current further reduces to 1.1×10^{-7} A/cm^2 at -1 V, lower than TiO_2-NPT samples over 3 orders. Since the leakage current improvement may result from thicker EOT due to lower κ value as the introduction of NPT and Ge nanocrystals, leakage current at -1 V as a function of EOT for different process conditions which was obtained from separate experiments is shown in **Fig. 3(b)**. Apparently, even with the same EOT, TiO_2-Ge-NPT samples reveal the lowest leakage current which confirms that Ge nanocrystals necessarily play the essential role for the leakage current improvement. The result of leakage current suppression is consistent with other nanocrystal based devices.[11, 12, 13]

The major mechanism behind the phenomenon can be understood by the band diagram of Ge-embedded TiO_2 shown in the **inset of Fig. 4**. Due to the conduction band offset of 0.33 eV between Ge nanocrystals and rutile TiO_2,[14] part of the injected electrons from

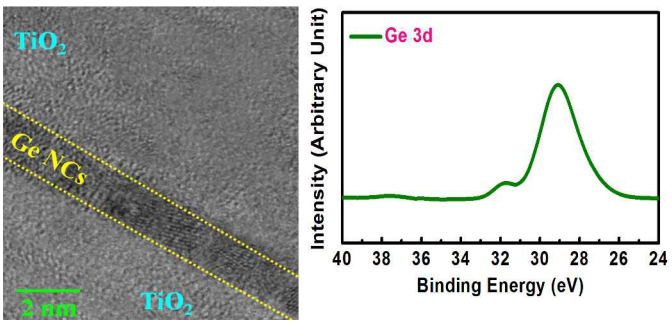

Fig. 1 Physical analysis of TiO2-Ge-NPT sample. (a) Cross-sectional TEM image. (b) XPS Ge 3d spectrum.

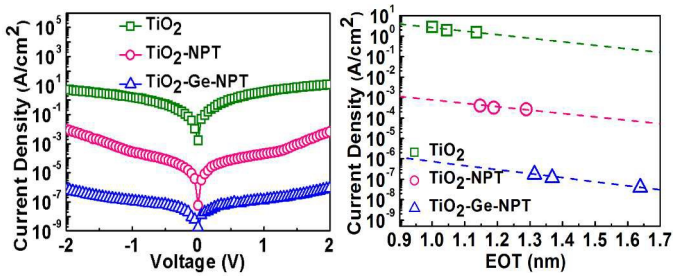

Fig. 3 (a) I-V curves for TiO_2-based MIM capacitors with various process conditions. (b) Leakage current (measured at -1 V) as a function of EOT for TiO_2-based MIM capacitors with various process conditions.

the electrode would be trapped in the Ge nanocrystals, just like the operation in nanocrystal-based memory devices. Once nanocrystals are occupied with electrons, two possible effects may occur.[12] (1) These trapped electrons in nanocrystals will prevent subsequent electrons from further injection and therefore reduced leakage current is obtained. It is the so-called Coulomb blockade effect.[11-13] The condition to observe Coulomb blockade effect in a practical device at room temperature (300 K) requires the charging energy (e^2/C_S)[15-16] to be 3 times higher than the thermal energy (k_BT, 25.9 meV at 300 K). Note that C_S denotes self-capacitance of the sphere and can be expressed as $4\pi\varepsilon_0\varepsilon_r R$ where R is the radius of a nanocrystal. Based on the electrical and physical parameters of Ge nanocrystals (ε_r~12.6 from capacitance measurement and R~0.75 nm from TEM image), C_S is 1.05 aF and charging energy is 152.32 meV. Since the charging energy is larger than thermal energy at 300 K, it proves that Coulomb blockade is possible to occur in this work. (2) These trapped electrons in nanocrystals build up an internal electric field which compensates the applied external field. It is the reduced effective electric field across the dielectric that makes the reduced leakage current. The internal electric field can be estimated as follows. For both TiO_2-Ge-NPT and TiO_2-NPT samples, current conduction mechanisms are found to be Poole-Frenkel emission (not shown). For a given electric field E_1, the leakage current for TiO_2-Ge-NPT samples and TiO_2-NPT samples are respectively J_1 and J_2 where J_1 is smaller than J_2. Since the leakage current through nitrided TiO_2 should be the same under equal electric field E_1 for both types of samples, the difference between J_1 and J_2 is attributed to the internal electric which compensates the applied external field. To obtain J_1 in TiO_2-NPT samples, the applied electric field should be decreased to E_2 which is the effective electric field in TiO_2-Ge-NPT samples under E_1. In other words, even though E_1 is applied in TiO_2-Ge-NPT samples, it experiences the effective electric field of E_2 and therefore the lower leakage current is obtained. The difference between E_1 and E_2 is the estimated internal electric filed that compensates the applied external field. From the data, the internal electric filed is about 0.7 MV/cm. The effect of a built-in internal electric field can be proven by showing the bi-directional I-V characteristic for TiO_2-NPT samples with and without Ge nanocrystals, as shown in **Fig. 4**. Cusps are observed for both types of capacitors where the current crosses zero, indicating the size of the hysteresis loop. The cusps can be found when the magnitude of external field is equal to that of the internal field. The higher absolute voltage of cusps for TiO_2-Ge-NPT samples implies that a larger amount of electrons can be trapped in nanocrystals and therefore cusps can be formed near the starting voltage of the sweep (± 2 V). This phenomenon also suggests that nanocrystals indeed store electrons during voltage sweeping and have the pivotal role in suppressing leakage current. Note that although NC-based traps may contribute to trap assisted tunneling (TAT) current, it is not the leakage conduction mechanism for the current between ± 2 V, which is inferred from the following viewpoints. (1) TAT happens when electrons are captured in the traps and then emitted to anode. However, from the hysteresis I-V curve, even though some electrons are tunneling from cathode to NC-based traps, electrons are captured (or stored in electrons) without being emitted between ± 2 V and therefore the assistance role of these traps for electron tunneling vanishes. (2) The leakage current demonstrates dependence on measurement temperature (not shown) and it conflicts the temperature-independent nature of carrier tunneling. Therefore the leakage current between ± 2 V is not from TAT, and Coulomb blockade effect play an important role in the voltage range. The inference is consistent with the simulation and experimental results in the literature[17, 18] where TAT is prohibited by Coulomb blockade at low electric field and can occur at high electric field. From aforementioned discussion, nanocrystals with smaller size is beneficial to enhance coulomb blockade effect. On the other hand, since the internal electric filed is generated by the trapped charges, it is expected that a higher density of Ge nanocrystals would lead to a larger internal electric field which is beneficial to suppress leakage current. Therefore, to further optimize the performance, smaller nanocrystals with a higher density are desirable and it may be achieved by depositing a thinner Ge layer with an optimum annealing conditions such as different thermal annealing time, ramp rate and ambient.

Fig. 5(a) displays the dependence of normalized capacitance on measurement temperature. As compared to TiO_2-NPT samples which correspond to temperature coefficient of capacitance (TCC) of 113 ppm/^{o}C, TCC for TiO_2-Ge-NPT samples improves to 88 ppm/^{o}C which can be explained by the reduced electron injection and causes higher relaxation time, consequently leading to a smaller capacitance

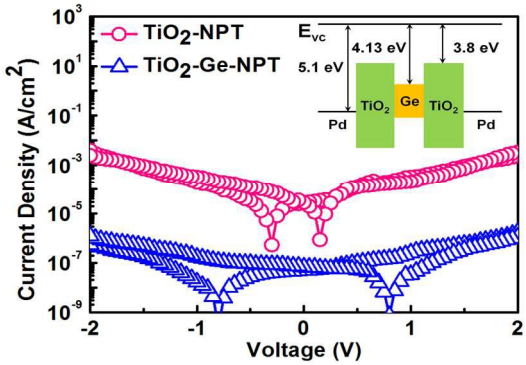

Fig. 4 Bidirectional I-V characteristics for TiO_2-NPT and TiO_2-Ge-NPT samples between ± 2 V voltage sweeping. The inset shows the band diagram (not to scale) for TiO_2-Ge-NPT samples.

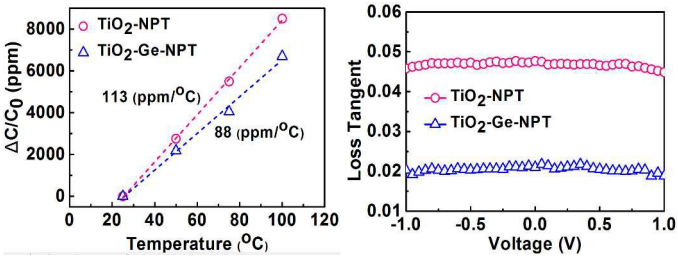

Fig. 5 (a) Temperature-dependent normalized capacitance and (b) Loss tangent for TiO_2-NPT and TiO_2-Ge-NPT samples. ΔC denotes the difference between zero-biased capacitance (C_0) at 25 ^{o}C and elevated temperature.

variation. Besides the requirement of low leakage current and small TCC, low dielectric loss is also a prerequisite for passive element applications. Dielectric loss quantifies the inherent electrical energy dissipation of a dielectric and the results are shown in **Fig. 5(b)**. At 1 MHz, loss tangent for TiO_2-NPT samples is about 0.045 and the value becomes 0.020 for TiO_2-Ge-NPT samples, which is improved by a factor of 2.2. Since loss tangent is dependent on conductance of the dielectric, once the leakage current can be reduced, improved loss tangent is expected as TiO_2-Ge-NPT samples.

Fig. 6(a) shows the impact of Ge nanocrystal incorporation on reliability performance which is quantified by capacitance variation as a function of constant voltage stress time for NPT samples. For TiO_2-Ge-NPT samples, an extrapolated capacitance variation of 1.04 % after 10-year operation under -1.5 V stress can be obtained. This performance is superior to those without incorporating nanocrystals

which is 1.58 % and the suppressed capacitance variation is mainly ascribed to fewer electron injections and trapped charges. **Fig. 6(b)** shows the stress induced leakage current (SILC) for TiO_2-Ge-NPT samples under different stress voltages measured at 25 °C. Leakage current degradation less than 25 % was observed which implies that the bonding strength of the nitrogen passivated TiO_2 is robust enough to restrain defects from generating during electrical stress and no percolation leakage paths are formed since no abrupt leakage current is observed after stress. Although SILC is insignificant, it is perceived that TAT is the major mechanism. It is the increased number of oxide traps after stress that makes TAT become more pronounced.

Table I summarizes the major device parameters for TiO_2-based[1, 3, 4, 6, 7, 8, 19, 20] and other recently published Gd_2O_3/Eu_2O_3,[21] $Al_2O_3/ZrO_2/SiO_2/ZrO_2/Al_2O_3$ (AZSZA)[22] MIM capacitors with

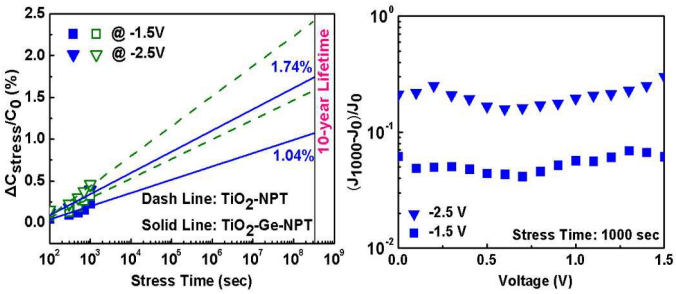

Fig. 6 (a) Capacitance change ($\Delta C_{stress}/C_0$) as a function of stress time for TiO_2-NPT samples with and without Ge nanocrystals measured at room temperature with stress voltage at -1.5 and -2.5 V. ΔC_{stress} denotes the difference between zero-biased capacitance (C_0) of the fresh and stressed devices. (b) SILC performance for TiO_2-Ge-NPT samples where J_0 and J_{1000} respectively denote the current for fresh condition and 1000-s stress.

Dielectric Material	Dielectric Thickness (nm)	Top/Bottom Electrode	Electrode WF (eV)	Capacitance (fF/μm²)	Leakage at -1 V (A/cm²)	Reference
TiO_2/Ge NCs/TiO_2 NCs: nanocrysals	11.5/1.5/11.5	Pd/Pd	5.1/5.1	25.2	1.1×10^{-7}	This work
TiO_2-LaAlO	15	Ir/TaN	5.3/4.6	24	1.4×10^{-7}	2010-Ref. [1]
TiNiO	20	Ni/TaN	5.1/4.6	17.1	7.7×10^{-6}	2007-Ref. [3]
TiHfO	12	TaN/TaN	4.6/4.6	28	4.8×10^{-6}	2008-Ref. [4]
TiPrO	16	Ir/TaN	5.3/4.6	20	1.2×10^{-7}	2009-Ref. [6]
$Sr_xTi_yO_z$ (SrO/TiO_2)	29.9/14.9	Pt/Pt	5.6/5.6	~22.5	$\sim 1.0 \times 10^{-5}$	2014-Ref. [7]
TiO_2/SiO_2	14.5/2.5	Al/TaN	4.3/4.6	11.9	8.3×10^{-7}	2012-Ref. [8]
TiO_2	25	Ni_2Si/Ni_2Si	4.6/4.6	17	1.2×10^{-5}	2011-Ref. [19]
$SiO_2/TiO_2/SiO_2$	2/16/2	TaN/TaN	4.6/4.6	12.4	8.8×10^{-7}	2014-Ref. [20]
Gd_2O_3/Eu_2O_3	8/8	Pt/Pt	5.6/5.6	12.5	1.0×10^{-7}	2013-Ref. [21]
AZSZA	1/7/3/7/1	TaN/TaN	4.6/4.6	7.4	1.1×10^{-8}	2014-Ref. [22]

TABLE I Comparison of major device parameters of TiO_2-based and other recent MIM capacitors with various dielectrics.

various electrodes for AMS applications. Nitrogen plasma treatment of Ge nanocrystals-embedded TiO_2 provides another promising avenue to obtain high capacitance density with much improved leakage current.

In conclusion, the leakage current of crystalline TiO_2-based MIM was greatly improved by introducing nitrogen plasma treatment and embedding Ge nanocrystals. The mechanism of nanocrystals induced leakage current reduction involves Coulomb blockade effect or internal electric field compensation effect. By integrating these processes, the MIM capacitors exhibit low leakage current of 1.1×10^{-7} A/cm^2 at -1 V while maintaining a high capacitance density of 25.2 fF/μm^2. In addition, the promising characteristics of the MIM capacitors are also evidenced by the small TCC of 88 ppm/°C, low loss tangent of 0.020, low SILC, and desirable capacitance change of 1.04 % after 10-year operation under -1.5 V. The desirable performance proves the eligibility of the nanocrystal-embedded MIM capacitors for advanced AMS applications.

Acknowledgements

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References

1 C. H. Cheng, C. K. Deng, H. H. Hsu, P. C. Chen, B. H. Liou, A. Chin, and F. S. Yeh, *J. Electrochem. Soc.*, 2010, **157**, H821.
2 K. C. Chiang, C. H. Lai, A. Chin, T. J. Wang, H. F. Chiu, J. R. Chen, S. P. McAlister, and C. C. Chi, *Symp. VLSI Tech.*, **2005**, 62.
3 C. C. Huang, C. H. Cheng, A. Chin, and C. P. Chou, *Electrochem Solid-State Lett.*, 2007, **10**, H287.
4 C. H. Cheng, H. C. Pan, C. C. Huang, C. P. Chou, C. N. Hsiao, J. Hu, M. Hwang, T. Arikado, S. P. McAlister, and A. Chin, *IEEE Electron Device Lett.*, 2008, **29**, 1105.
5 C. H. Cheng, H. C. Pan, S. H. Lin, H. H. Hsu, C. N. Hsiao, C. P. Chou, F. S. Yeh, and A. Chin, *J. Electrochem. Soc.*, 2008, **155**, G295.
6 C. C. Huang, C. H. Cheng, K. T. Lee, and B. H. Liou, *J. Electrochem. Soc.*, 2009, **156**, G23.
7 N. Aslam, V. Longo, W. Keuning, F. Roozeboom, W.M.M. Kessels, R. Waser, and S. Hoffmann-Eifert, Phys. Status Solidi A, 2014, **211**, 389.
8 Y. H. Wu, W. Y. Ou, C. C. Lin, J. R. Wu, M. L. Wu, and L. L. Chen, *IEEE Electron Device Lett.*, 2012, **33**, 104.
9 E. S. M. Goh, T. P. Chen, H. Y. Yang, Y. Liu, and C. Q. Sun, *Nanoscale*, 2012, **4**, 1308.
10 H. Choi, M. Chang, M. Jo, S. J. Jung, and H. Hwang, *Electrochem Solid-State Lett.*, 2008, **11**, H154.
11 T. C. Chang, S. T. Yan, P. T. Liu, C. W. Chen S. H. Lin and S. M. Sze, *Electrochem Solid-State Lett.*, 2004, **7**, G17.
12 C. C. Wang, Y. K. Chiou, C. H. Chang, J. Y. Tseng, L. J. Wu, C. Y. Chen, and T. B. Wu, *J. Phys. D: Appl. Phys.*, 2007, **40**, 1673.
13 X. Ma and C. Wang, *Appl. Phys. B.*, 2008, **92**, 589.
14 D. Tsukamoto, A. Shiro, Y. Shiraishi, Y. Sugano, S. Ichikawa, S. Tanaka, and T. Hirai, *ACS Catal.*, 2012, **2**, 599.
15 Z. Z. Lwin, K.L. Pey, N. Raghavan, Y. Chen, and S. Mahapatra, *IEEE Electron Device Lett.*, 2011, **32**, 800.
16 P. Jiang, Z. F. Liu, and S. M. Cai, *J. Appl. Phys.*, 2001, **90**, 2039.
17 H. Watanabe, K. Yao, and J. Lin, *IEEE Trans. Electron Devices*, 2014, **61**, 1145.
18 C. H. Yang, Y. Kuo, C. H. Lin, and W. Kuo, *ECS Trans.*, 2010, **33**, 307.
19 J. H. Lee, Y. C. Lin, and B. H. Chen, *IEEE Trans. Electron Devices*, 2011, **58**, 672.
20 Q. X. Zhang, B. Zhu, L. F. Zhang, and S. J. Ding, Microelectronic Eng., 2014, **122**, 1.
21 R. Padmanabhan, N. Bhat, and S. Mohan, *IEEE Trans. Electron Devices*, 2013, **60**, 1523.
22 Q. X. Zhang, B. Zhu, S. Ding, H. Lu, Q. Sun, P. Zhou, and W. Zhang, *IEEE Electron Device Lett.*, 2014, **35**, 1121.

