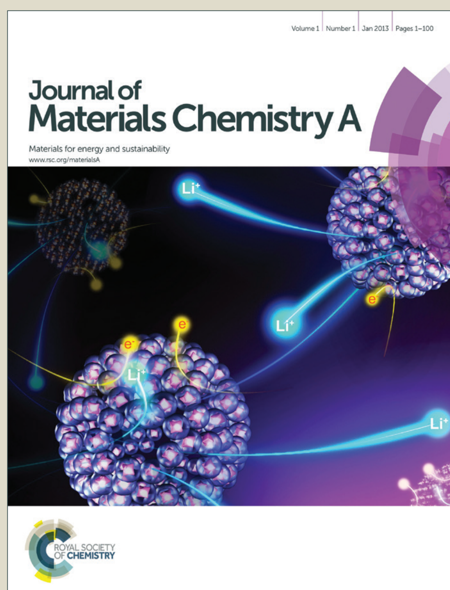
Journal of Materials Chemistry A

Accepted Manuscript



This is an *Accepted Manuscript*, which has been through the Royal Society of Chemistry peer review process and has been accepted for publication.

Accepted Manuscripts are published online shortly after acceptance, before technical editing, formatting and proof reading. Using this free service, authors can make their results available to the community, in citable form, before we publish the edited article. We will replace this *Accepted Manuscript* with the edited and formatted *Advance Article* as soon as it is available.

You can find more information about *Accepted Manuscripts* in the Information for Authors.

Please note that technical editing may introduce minor changes to the text and/or graphics, which may alter content. The journal's standard Terms & Conditions and the Ethical guidelines still apply. In no event shall the Royal Society of Chemistry be held responsible for any errors or omissions in this *Accepted Manuscript* or any consequences arising from the use of any information it contains.

ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/materialsA

Journal of Materials Chemistry A RSCPublishing

COMMUNICATION

Core-Shell $Si_{1-x}Ge_x$ Nanowires with Controlled Structural Defects for Phonon Scattering Enhancement

Cite this: DOI: 10.1039/x0xx00000x

Received 00th February 2014, Accepted 00th January 2014

DOI: 10.1039/x0xx00000x

www.rsc.org/

Jong Woon Lee,[a,g] Junho Lee,[b] Su-in Yi,[c] Young Min Seo,[f,g] Byoung Lyong Choi,[d] Choongho Yu,[c] Cheol-Woong Yang,[f] Sungwoo Hwang,[d,g] Sungjin Kim,[e] Dongmok Whang[a,f,g*] and Eun Kyung Lee[e*]

We first demonstrate core-shell $Si_{1-x}Ge_x$ alloy nanowires that can suppress the phonon propagation in nanowires without reducing the electrical conductivity. Non-uniformly distributed structural defects in the outer shells of the $Si_{1-x}Ge_x$ nanowires enhance boundary scattering during phonon transport, while a defect-free core provides a current path for electrical carriers.

With controlled atomic ratio of Si and Ge, the lattice dimension and energy band gap of $Si_{1-x}Ge_x$ alloy can be continuously tuned. This variability of $Si_{1-x}Ge_x$ alloys lead to numerous applications including electronics, optoelectronics, and thermoelectric.[1-4] In particular, various nanostructured $Si_{1-x}Ge_x$ alloys, such as superlattice $Si_{0.84}Ge_{0.16}/Si_{0.76}Ge_{0.24}$[5] and nanostructured bulk $Si_{1-x}Ge_x$[6], have been suggested to enhance the thermoelectric efficiency by enforcing phonon scattering by lattice disorder. Thermoelectric efficiency can be determined by the dimensionless figure of merit, $ZT = S^2\sigma T/k$, where S is the Seebeck coefficient, σ is electrical conductivity, and k is thermal conductivity. The strong correlation between these thermoelectric properties has made it difficult to achieve a high performance in thermoelectric energy harvesting. In particular, one-dimensional nanowires have been considered to be very effective structures for suppressing the lattice thermal contribution due to the large boundary-phonon scattering without reducing electrical conductivity.[7] $Si_{1-x}Ge_x$ alloy nanowires further reduce thermal conductivity by scattering the short and middle range of phonons that are not effectively suppressed by the nanowire surfaces.[8] Moreover, in order to maximize the phonon scattering, unique one-dimensional structures have been studied, such as rough silicon nanowires, Si-Ge core-shell nanowires, and silicon nanotubes. For instance, nanowires with a rough surface are able to reduce thermal conductivity by as much as two orders of magnitude relative to bulk crystalline silicon.[9] The thermal conductivity of Si-Ge core-shell nanowires was decreased by 75% at room temperature because of depression and localization of long-wavelength phonon modes at the Si/Ge interface.[10] In addition, silicon nanotubes can induce a 35% reduction in thermal conductivity due to phonon-boundary scattering enhancement, which results from a large surface to volume ratio.[11] In order to obtain a high figure of merit, not only a reduction in thermal conductivity, but also an increase or maintenance of electrical conductivity is important. In this study, we present core-shell $Si_{1-x}Ge_x$ alloy nanowires with a defected shell as a useful candidate for efficient thermoelectric materials. In addition to binary alloying effects, the non-uniformly distributed stacking faults inside the taper-shaped nanowire shell can also serve as barriers when phonons propagate through nanowires. Thermal conductivity of tapered $Si_{1-x}Ge_x$ alloy nanowires with an average diameter of 347 nm is as low as ~1.24 W/m·K at 300 K.

$Si_{1-x}Ge_x$ core-shell alloy nanowires with tapering shape edges were grown using Au-catalysed chemical vapour deposition (CVD) under an atmosphere of SiH_4 (10% in H_2), GeH_4 (10% in H_2), and PH_3 (100 ppm in H_2) as source gases and a doping gas, respectively (Figs. 1(a) and 1(b)). The Si substrate was cleaned with an organic solvent followed by removal of the surface oxide layer using diluted HF solution and 3-nm-thick Au was thermally deposited on the substrate. The alloy NWs were then grown by flowing 40 sccm SiH_4 (10 % in H_2), 40 sccm GeH_4 (10 % in H_2) at 480 °C and 50 Torr. In order to make an ohmic contact between nanowire and metal electrode, we doped the $Si_{1-x}Ge_x$ nanowire by adding 40 sccm PH_3 (100 ppm in H_2). The nanowire cores were uniformly grown by the typical Au-catalysed vapour-liquid-solid (VLS) mechanism, whereas vapour-solid (VS) growth on the nanowire surface resulted in the tapered shells and rough edges. As shown in the cross-sectional line profiles in Fig. 1(c), Si and Ge are distributed uniformly at tip region. At the shell region, however, the relative amount of Ge is higher than that of the core. Because there is a limit to the quantitative analysis by line scan profile, we also analysed the quantitative compositions of the core (point 1) and shell (point 2) by Energy Dispersive X-ray Spectroscopy (EDS). In order to evaluate the compositions of the core and shell, we assumed that each composition of the cores and shells of nanowires is retained during

Journal of Materials Chemistry A Accepted Manuscript

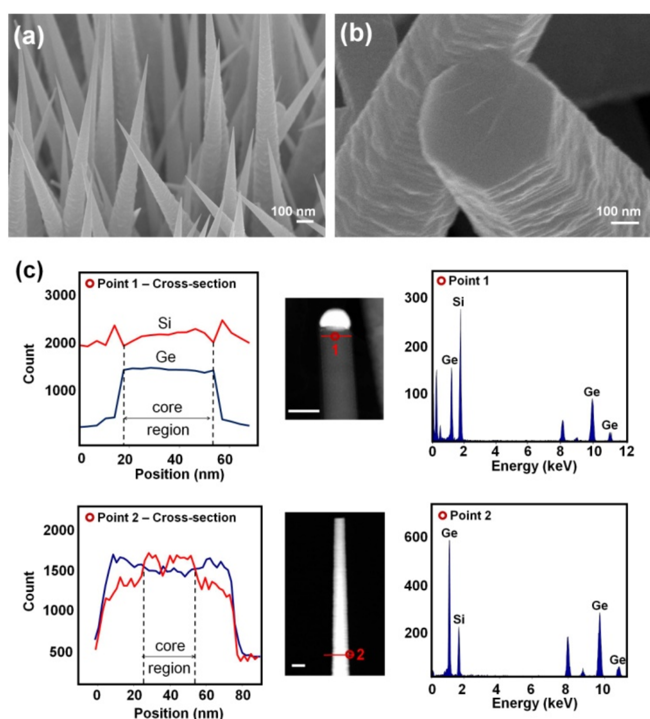


Figure 1. (a), (b) SEM images of $Si_{1-x}Ge_x$ alloy nanowires; all nanowires have a tapering shape and rough surfaces, (c) Composition of $Si_{1-x}Ge_x$ nanowire at the tip (point 1 at upper TEM image) and shell (point 2 at lower TEM image) of the nanowire by EDS. The scale bars are 100 nm. The left graphs shows distribution of Si and Ge at points 1 and 2, the right graphs are the composition Si and Ge at points 1 and 2

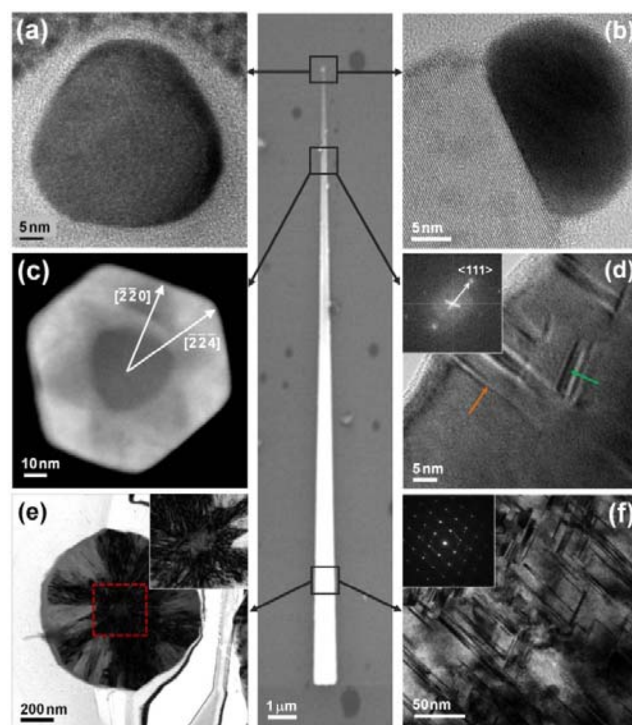


Figure 2. TEM images of the core-shell $Si_{1-x}Ge_x$ alloy nanowire: (a, c, e) are cross-sectional TEM images of $Si_{1-x}Ge_x$ alloy nanowires at the top (d = ~20 nm), middle (d = ~80 nm), and bottom (d = ~800 nm) regions; (b, d, f) are the in-plane TEM images of $Si_{1-x}Ge_x$ alloy nanowires. There is no shell on the core (a, b) at the top region, and when shell thickness is ~20 nm, the $Si_{1-x}Ge_x$ alloy nanowire is composed of a defect-free core and defected shell (c, d). The orange and green arrows in (d) indicate $[\bar{1}1\bar{1}]$ and $[11\bar{1}]$, respectively. As the diameter of the nanowires increase, plane defects distribute all over the nanowire to release the strain (e, f)

VLS and VS growth. The composition ratio of the nanowire core and shell were estimated as Si : Ge = 0.30 : 0.70 based on the composition of Si : Ge = 0.65 : 0.35 at the tip of the nanowire. The thermal decomposition rate of GeH_4 is one order of magnitude higher than that of SiH_4 at 400 °C,[12, 13] which results in the higher concentration of Ge in the shell. Using Vegard's law,[14] the lattice constants of the core and shell were calculated as 5.510 Å and 5.589 Å, respectively, which indicates that the lattice mismatch between the core and shell was ~1.4%. The lattice constant difference between the substrate and epitaxially deposited materials inevitably cause strain. In order to relax the strain, defects such as dislocations and stacking faults along with rough surfaces can be formed in nanowires, as shown in Fig. 1(b).

Figure 2 shows structural features at three different locations along the nanowire axis of the tapered $Si_{1-x}Ge_x$ alloy nanowires, with diameters of ~20, ~80, and ~800 nm (Fig. 2). At the top region, the nanowire has a defect-free structure without an outer shell (Figs. 2(a) and (b)). In contrast, as shell thickness increases and tapers, plane defects, such as stacking faults, are incorporated into the shell of the nanowire due to the accumulated strain (Figs. 2(c) and (d)). The shell of nanowire with high Ge concentration was under compressive stress while the core was under tensile stress due to lattice mismatch between the core and shell. In the core-shell $Si_{1-x}Ge_x$ alloy nanowire, when shell thickness is ~20 nm, we can identify different contrasts in the shell region due to defect density. In the core-shell structure, dislocations are generated due to the lattice constant mismatch.

Perfect dislocation is dissociated into two partial dislocations in order to enhance its energetic stability. In the Fig. 2(c), the regions, along the $[\bar{2}\bar{2}4]$ directions from the core, which is associated with the partial dislocations, is brighter than the regions along the $[\bar{2}\bar{2}0]$ direction, which have perfect dislocations. These defects are generated between the {111} planes of tapered $Si_{1-x}Ge_x$ alloy nanowires, which is perpendicular to the growth direction, as shown in Fig. 2(d). As shell thickness increases, strain is accumulated inside the core region, and finally the structural defects were generated all over the nanowire to release the strain, as shown in Figs. 2(e) and 2(f).

To evaluate electrical property of the nanowires, we fabricated electrical devices of the nanowires on a SiO_2/Si substrate with Ni/Au electrodes. (Fig. 3(a)) These nanowire devices were annealed at 400 °C for 1 min in a N_2 environment to reduce the contact resistance between the nanowire and electrodes. Temperature increasing rate was 6.3 °C/sec. The electrical resistivities of the taper-shaped nanowires were calculated with average diameter between two metal electrodes. We measured the resistivity of $Si_{1-x}Ge_x$ alloy nanowire with diameter 80 nm using 4-point measurement and compared the electrical resistivities from 2-point measurement of tapered nanowire. From the comparison, the contact resistance was found to be negligible (See more details in Electronic Supplementary Information). As shown in fitting line of Fig. 3(a),

Journal of Materials Chemistry A Accepted Manuscript

This journal is © The Royal Society of Chemistry 2012

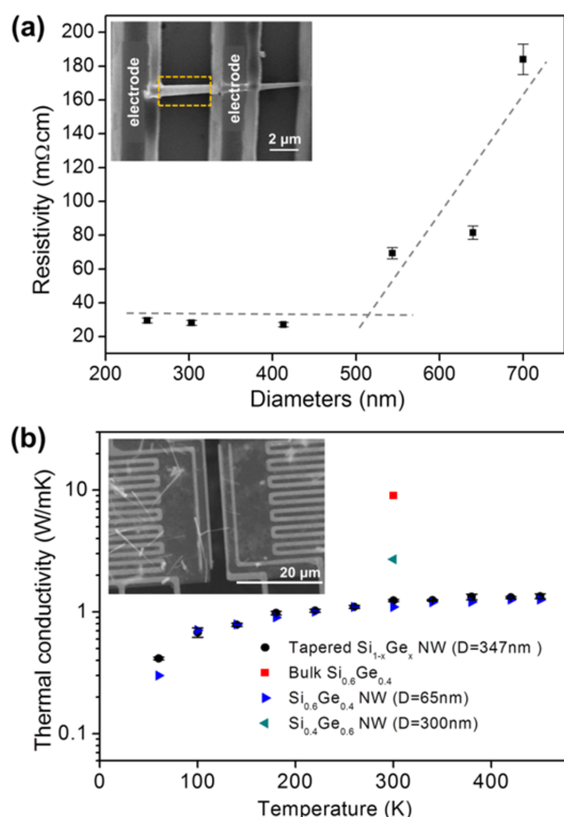


Figure 3. (a) Resistivity of core-shell $Si_{1-x}Ge_x$ alloy nanowires at 300 K (black squares). Each $Si_{1-x}Ge_x$ alloy nanowire with a different diameter was measured. The inset shows a SEM image of the device. Diameter was the average diameter (d_{max} + d_{min})/2 between two metal electrodes (yellow dashed rectangle in the inset). Resistivities of nanowires with diameters greater than about 500 nm tend to increase from a fit to the data. (dashed line) (b) The thermal conductivity of a core-shell $Si_{1-x}Ge_x$ alloy nanowire with a diameter of ~340 nm (black squares), bulk SiGe (red up-square), defect-free $Si_{0.6}Ge_{0.4}$ alloy nanowire with a diameter of 65 nm (blue squares), defect-free $Si_{0.4}Ge_{0.6}$ nanowire with diameter 300 nm (green diamond). The inset is a $Si_{1-x}Ge_x$ alloy nanowire on the MEMS device for thermal conductivities.

the electrical resistivities of tapered nanowires maintained constant values ~30 mΩ·cm up to average diameters of ~500 nm, in spite that stacking faults remained in the shell region. We infer that defect-free nature of NW core and low defect density in the shell lead to low electrical resistivity. In comparison, the electrical resistivity of the nanowire whose diameter at the middle point is greater than ~500 nm significantly increased because of high stacking fault density inside of the nanowire.

Moreover, these nanowire defects can affect the phonon propagation. We measured the thermal conductivity of a tapered $Si_{1-x}Ge_x$ nanowire with an average diameter of ~340 nm (top of 245 nm and bottom of 449 nm) at 60−450 K using a micro-device, as shown in the inset of Fig. 3(b). In order to reduce thermal contact resistance, Pt was deposited by using focused ion beam (FIB) and the sample was annealed at 600 °C in a high vacuum environment (better than 10^{-6} Torr) (See more details in Electronic Supplementary Information). The evaluated $Si_{1-x}Ge_x$ nanowire was composed of a core ($Si_{0.65}Ge_{0.35}$) and taper-shaped shell ($Si_{0.3}Ge_{0.7}$). The measured thermal conductivity of the tapered $Si_{1-x}Ge_x$ nanowire was as low as ~1.24 W/m·K at 300 K, as plotted in Fig. 3(b) (black squares). This

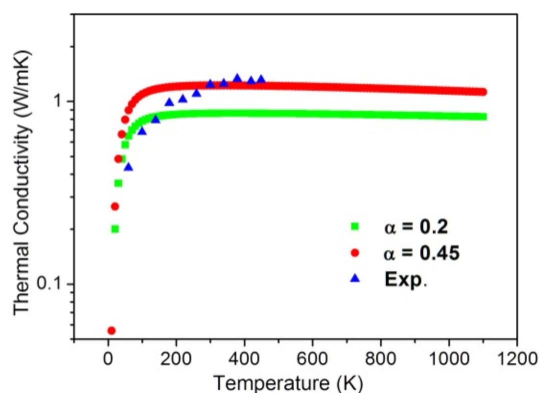


Figure 4. Thermal conductivity of a core-shell $Si_{1-x}Ge_x$ alloy nanowire (blue triangles) and calculated thermal conductivity of a $Si_{0.3}Ge_{0.7}$ shell with planar defects using the Boltzmann Transport Equation (BTE) with Callaway's model. The specularity parameter (*α*) was 0.2 (green squares) and 0.45 (red circles), respectively.

value was 84% less than that of the $Si_{1-x}Ge_x$ bulk material (red up-square in Fig. 3(b)).[15] The thermal conductivity of the tapered $Si_{1-x}Ge_x$ nanowire is significantly reduced than the conductivity of the defect-free $Si_{0.4}Ge_{0.6}$ nanowire with a similar diameter (green squares in Fig. 3(b))[15] and is similar to the value of defect-free $Si_{0.6}Ge_{0.4}$ alloy nanowire with a diameter of 65 nm[16] (blue squares in Fig. 3(b)), in spite of its larger diameter. Potential difference in the doping concentration of the nanowires may induces large difference in their electrical conductivity, but its effect on the thermal conductivity is limited[17]. In addition, our previous work has shown that the thermal conductivity of $Si_{1-x}Ge_x$ alloy nanowires is insensitive to its composition, when x (Ge mole fraction) is in the range of 0.2 to 0.8.[16] Therefore, by comparing thermal conductivity between the core-shell $Si_{1-x}Ge_x$ and the defect-free $Si_{1-x}Ge_x$ nanowires, we can conclude that low thermal conductivity of the core-shell $Si_{1-x}Ge_x$ nanowire is due to effective phonon scattering by the structural defects in the shell. We also note that thermal contact resistances between the core-shell nanowire and the membranes of device are not likely to significantly influence the results. The total thermal resistance is ~2×10^7 K/W, whereas the thermal contact resistance is estimated to be smaller than ~10^6 K/W. The contact resistance was obtained by assuming the contact length and thermal conductivity are 1μm and 0.5 ~ 1 W/m·K respectively.[18]

To analyze the phonon scattering by defects inside the shell region, we used the Boltzmann Transport Equation (BTE) with Callaway's model, which separately considered longitudinal and transverse components and used adjusted cut-off frequency.[19] A detailed description can be found in Morelli's work.[20] In addition to Normal scattering ($\tau_{N,i}$), Umklapp scattering ($\tau_{U,i}$), alloy scattering ($\tau_{A,i}$), and the nanowire's boundary scattering ($\tau_{B,i}$), we considered the phonon relaxation time from internal plane defects ($\tau_{D,i}$), which is given by:

$$\left(\tau_{D,i}\right)^{-1} = \frac{v_i}{d}\left(\frac{1-\alpha}{1+\alpha}\right)$$

where v_i is speed of sound due to longitudinal (i = L) or transverse (i=T) phonons (we used linear averages of $v_{Si,i}$ and $v_{Ge,i}$: $v_L = 0.3v_{Si,L} + 0.7v_{Ge,L}$ and $v_T = 0.3\ v_{Si,T} + 0.7v_{Ge,T}$),[20] d is the mean free path of a

Journal of Materials Chemistry A Accepted Manuscript

phonon, and α is a specularity parameter (α = 1 for specular, α = 0 for diffusive). The mean free path, d, was assumed to be the average size of single crystallites among stacking faults.[21] In our sample, the size of crystallites was distributed in the range of 2−40 nm, of which the average value was ~19 nm. Lastly, the specularity parameter, $0 < \alpha < 1$, was used to fit the experimental data in consideration of the different specularity of boundary scattering due to plane defects compared to the nanowire boundary ($\alpha \approx 0$, almost diffusive). The total relaxation time for longitudinal and transverse modes was calculated using Matthissen's rule: $(\tau_i)^{-1} = (\tau_{N,i})^{-1} + (\tau_{U,i})^{-1} + (\tau_{A,i})^{-1} + (\tau_{B,i})^{-1} + (\tau_{D,i})^{-1}$. Finally, the total lattice thermal conductivity was obtained by $k = 1/3(k_L + 2k_T)$. Considering the negligible electronic thermal conductivity, the lattice contribution was only employed to fit the experimental data. Note that, because of the ambiguity of a defined d for $\tau_{B,i}$ that stems from its hollow cylindrical geometry, we converted the thermal conductivity of the entire nanowire (k_{NW}) and the core of the nanowire (k_c) to the thermal conductance of the entire nanowire (G_{NW}) and the core of the nanowire (G_c), respectively. Then the thermal conductance of shell nanowire ($G_s = G_{NW} - G_c$) was obtained, which was converted back to the thermal conductivity ($k_s = G_s \cdot A_s^{-1} \cdot L$), where L was the length of the nanowire. The effect of scattering between G_s and G_c should be included, but was negligible in the calculation of k_c because the boundary scattering due to internal defects was dominant over that of nanowire boundary. When α = 0.2, the calculation adequately fit the data for $T < 250$ K, and by slightly adjusting α= 0.45, the experimental data up to 450 K was well described. Considering the more specular nature of plane defect boundary (α = 0.2−0.45), compared to the nanowire boundary ($\alpha \approx 0$), we can conclude that the remarkably low thermal conductivity of tapered core-shell nanowire is attributed to the interior scattering by high-density stacking faults.

In summary, the core-shell $Si_{1-x}Ge_x$ nanowire structures which have defects such as stacking faults in the shell have shown significantly reduced thermal conductivity by increasing phonon-defect interactions while electrical conductivity is maintained. Based on these results, defect-engineered nanostructures can be an effective way to highly efficient thermoelectric materials.

Acknowledgements

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean Government (MEST) (2007-0054845). D.W. acknowledges the support by Basic Science Research Program through NRF (2009-0083540).

Notes and references

[a] SKKU Advanced Institute of Nanotechnology, Sungkyunkwan University, Suwon, 440-746, Korea.
[b] Analytical Engineering Group, Samsung Advanced Institute of Technology, Samsung Electronics, Yongin, Kyunggi-do 446-712, Korea.
[c] Department of Mechanical Engineering, Texas A&M University, College Station, TX 77843 USA.
[d] Nano Electronics Laboratory, Samsung Advanced Institute of Technology, Samsung Electronics, Giheung-gu, Yongin-si, Gyeonggi-do, 446-712, Korea.
[e] Computer Aided Group, Samsung Advanced Institute of Technology, Samsung Electronics, Yongin, Kyunggi-do, 446-712, Korea.
[f] School of Advanced Materials Science and Engineering, Sungkyunkwan University, Suwon, 440-746, Korea.
[g] Research Center for Time-Domain Nano-Functional Devices, Samsung Advanced Institute of Technology, Giheung, Yong-In, Gyeonggi, 446-712, Korea.

† Electronic Supplementary Information (ESI) available: [I-V curve and 4-point measurement of SiGe alloy nanowire]. See DOI: 10.1039/b000000x/

1. J. Liu, M. Beals, A. Pomerene, S. Bernardis, R. Sun, J. Cheng, L. C. Kimerling and J. Michel, *Nat. Photon.*, 2008, **2**, 433-437.
2. N. Hrauda, J. Zhang, E. Wintersberger, T. Etzelstorfer, B. Mandl, J. Stangl, D. Carbone, V. Holý, V. Jovanović, C. Biasotto, L. K. Nanver,J. r. Moers, D. Grŭtzmacher and G. n. Bauer, *Nano Lett.*, 2011, **11**, 2875-2880.
3. J. P. Douglas, *Semicond. Sci. Technol.*, 2004, **19**, R75.
4. G. J. Snyder and E. S. Toberer, *Nat. Mater.*, 2008, **7**, 105-114.
5. S. T. Huxtable, A. R. Abramson, C.-L. Tien, A. Majumdar, C. LaBounty, X. Fan, G. Zeng, J. E. Bowers, A. Shakouri and E. T. Croke, *Appl. Phys. Lett.*, 2002, **80**, 1737-1739.
6. G. Joshi, H. Lee, Y. Lan, X. Wang, G. Zhu, D. Wang, R. W. Gould, D. C. Cuff, M. Y. Tang, M. S. Dresselhaus, G. Chen and Z. Ren, *Nano Lett.*, 2008, **8**, 4670-4674.
7. D. Li, Y. Wu, P. Kim, L. Shi, P. Yang and A. Majumdar, *Appl. Phys. Lett.*, 2003, **83**, 2934-2936.
8. W. Kim, R. Wang and A. Majumdar, *Nano Today*, 2007, **2**, 40-47.
9. A. I. Hochbaum, R. Chen, R. D. Delgado, W. Liang, E. C. Garnett, M. Najarian, A. Majumdar and P. Yang, *Nature*, 2008, **451**, 163-167.
10. M. Hu, K. P. Giapis, J. V. Goicochea, X. Zhang and D. Poulikakos, *Nano Lett.*, 2010, **11**, 618-623.
11. J. Chen, G. Zhang and B. Li, *Nano Lett.*, 2010, **10**, 3978-3983.
12. J. M. Jasinski, B. S. Meyerson and T. N. Nguyen, *J. Appl. Phys.*, 1987, **61**, 431-433.
13. J. W. Kim, M. K. Ryu, K. B. Kim and S. J. Kim, *J. Electrochem. Soc.*, 1996, **143**, 363-367.
14. A. R. Denton and N. W. Ashcroft, *Phys. Rev. A*, 1991, **43**, 3161-3164.
15. Z. Wang and N. Mingo, *Appl. Phys. Lett.*, 2010, **97**, 101903.
16. E. K. Lee, L. Yin, Y. Lee, J. W. Lee, S. J. Lee, J. Lee, S. N. Cha, D. Whang, G. S. Hwang, K. Hippalgaonkar, A. Majumdar, C. Yu, B. L. Choi, J. M. Kim and K. Kim, *Nano Lett.*, 2012, **12**, 2918-2923.
17. J. A. Carruthers, T. H. Geballe, H. M. Rosenberg and J. M. Ziman, *Proc. R. Soc. A*, 1957, **238**, 502-514.
18. C.-L. Tien, A. Majumdar and F. M. Gerner, *Microscale Energy Transport; Taylor & Francis: Washington DC*, 1998.
19. N. Mingo, *Phys. Rev. B*, 2003, **68**, 113308.
20. D. T. Morelli, J. P. Heremans and G. A. Slack, *Phys. Rev. B*, 2002, **66**, 195304.
21. A. J. Minnich, H. Lee, X. W. Wang, G. Joshi, M. S. Dresselhaus, Z. F. Ren, G. Chen and D. Vashaee, *Phys. Rev. B*, 2009, **80**, 155327.

Journal of Materials Chemistry A Accepted Manuscript

This journal is © The Royal Society of Chemistry 2012