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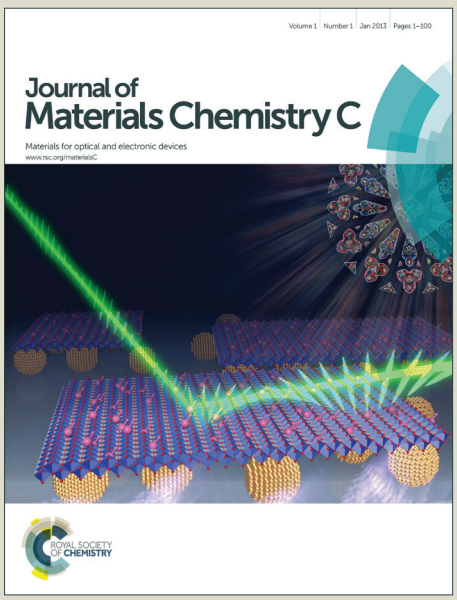

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ARTICLE

Flash memory based on solution processed hafnium dioxide charge trapping layer

Cite this: DOI: 10.1039/x0xx00000x

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Received 00th January 2014,
Accepted 00th January 2014

DOI: 10.1039/x0xx00000x

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Hafnium dioxide (HfO_2) film prepared by sol-gel technique has been used as a charge trapping layer in organic flash memory. The thickness, crystallinity and morphology of HfO_2 fabricated by various conditions were investigated. X-ray diffraction (XRD) patterns indicated the formation of monoclinic HfO_2 crystals with increasing annealing temperature. Atomic force microscope (AFM) images showed relatively smooth films of HfO_2 growth. The annealing temperature dependent effects on the memory window as well as data retention properties have been discussed. A large memory window and long data retention time have been achieved for the pentacene based flash memory. The results demonstrate that solution proceed HfO_2 film could be a promising candidate as charge trapping layer in printable flash memory.

1. Introduction

Recently, flash memories have attracted great attention as they have considerable share in the non-volatile semiconductor memory market.[1-7] Flash memory is an electronic device used for data storage with non-volatile property which can be electrically programmed and erased. Tremendous efforts have been focused on the development of flash memory for portable electronic devices, smart television, radio frequency identification (RFID) tags and so on.[8-21] Flash memory is the leading product in the market of non-volatile semiconductor memory with more strict requirements as the microelectronic technology advances where the data storage and density requirements increase dramatically. Traditional flash memory based on the concept of floating gate has the drawback that unexpected conduction between the floating gate and channel may occur and all the charges may be drained off as the floating gate is a conductor.

To solve these problems, flash memory was proposed by using insulating materials as the charge trapping elements.[22-25] Recently, various dielectric materials with high dielectric constant have been employed as charge trapping materials to improve the operating speed and get better charge retention ability. For examples, TiO_2, [26, 27] Si_3N_4,[23, 24, 28, 29] and HfO_2 [22-25, 30, 31] have been studied in previous reports. In addition, numerous methods have been developed to prepare these insulator films. Among them, HfO_2 has been widely used as it has a higher charge trapping density and can be prepared by various techniques such as chemical vapor deposition (CVD),[24, 25] physical vapor deposition (PVD),[32] and atomic layer deposition (ALD).[22, 23, 33] Although the HfO_2 can be deposited using alternative methods such as ALD, CVD, or PVD, the complicated instruments and procedures restrain their practical application. Further, the solution processed HfO_2 shows great potential in large area production, which can be printed through roll-to-roll process. To reduce the cost on the fabrication procedure, solution process method has been proposed to fabricate the HfO_2 film.[30, 34] For the first time, we demonstrate an organic flash memory based on solution processed HfO_2. Therefore, it is necessary to investigate the charge trapping property of solution processed HfO_2 and the influences on the memory effect.

Here, we report a novel organic flash memory based on sol-gel processed HfO_2. Memory devices were fabricated with sol-gel processed HfO_2 as floating gate and their respective memory properties were analyzed. In addition, the effects of annealing temperature and thickness of HfO_2 film on the memory properties have been studied. Pentacene was used as the organic semiconductor due to its high mobility and stable electrical performance.[34-38] The thickness of HfO_2 film decreases with increasing spin-coating speed or annealing temperature. We systematically studied the program/erase behavior for the fabricated devices. A memory window of 41.10 V was obtained with the data retention time of more than 10^5 s. These results indicate that the solution processed HfO_2 could be an excellent candidate for printable memory devices.

2. Experimental

2.1. Materials

Hafnium (IV) chloride ($HfCl_4$, 98%) and pentacene (sublimated grade) were purchased from Aldrich. All chemicals and solvents were used without further purification. The highly

doped Si wafer with 300 nm SiO_2 was cleaned using standard method and then transferred into the glove box filled with N_2 for further use.

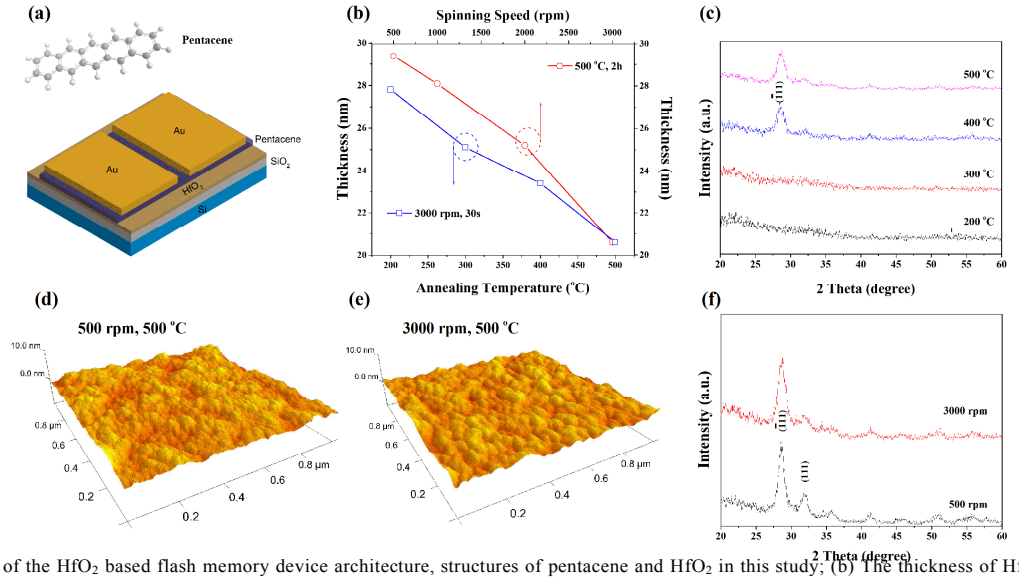

Fig. 1 (a) Schematic of the HfO_2 based flash memory device architecture, structures of pentacene and HfO_2 in this study; (b) The thickness of HfO_2 films prepared at various spinning speed or annealing temperature; (c) XRD patterns of HfO_2 films spin-coated at 3000 rpm for 30 s and annealed at 200, 300, 400 and 500 °C for 2 h; AFM images of HfO_2 film spin-coated at the speed of (d) 500 rpm and (e) 3000 rpm for 30 s and annealed at 500 °C for 2 h. (f) XRD patterns of HfO_2 films spin-coated at the speed of 500 rpm and (c) 3000 rpm for 30 s and annealed at 500 °C for 2 h.

2.2. Preparation of HfO_2 precursor

The starting materials, $HfCl_4$, C_2H_5OH, HNO_3 and H_2O were weighed according to the stoichiometric ratio of $HfCl_4$:C_2H_5OH:HNO_3:H_2O = 1:410:5:5. The solution of HfO_2 precursor was prepared by mixing the $HfCl_4$ and C_2H_5OH under nitrogen atmosphere and followed by mixing with distilled water and HNO_3. Then, to promote the hydrolysis and polymerization of the HfO_x sol-gel, the solution was filtered using a 0.2 μm PTFE filter and heated at 50 °C for 3 h.[34]

The HfO_2 film was prepared by spin-coating the HfO_2 sol-gel. To study the thickness dependent effects, the HfO_2 film on the cleaned substrate was obtained by spin-coating at different speed from 500 to 3000 rpm for 30 s, and followed by annealing at 500 °C for 2 h. Another set of HfO_2 films were prepared to investigate the temperature dependent effects using the same spinning speed of 3000 rpm for 30 s but different annealing temperature from 200 °C to 500 °C.

2.3. Device fabrication

The device architecture in this study is given in Fig. 1a. Top contact geometry was used in our memory devices. In a typical fabrication process, the HfO_2 was prepared by spin-coating its precursor on the cleaned heavily-doped p-type Si with a 300 nm native SiO_2 layer. For our device and silicon-oxide-nitride-oxide-silicon (SONOS) type memories, the HfO_2 and Si_3N_4 are used as charge trapping layers respectively. The HfO_2 functionalized as both tunneling and charge storage layer in this study while the SONOS have separated layers with SiO_2 and Si_3N_4 as the tunneling and charge storage layers respectively. For the consideration of simplicity, the device structure is shown in Fig 1a. The p-type Si acts as the control gate while SiO_2 layer serves as the blocking dielectric layer. A 40 nm pentacene, an organic compound with five fused benzene rings as shown on the top left of Fig 1a, was thermally deposited as a p-type semiconducting layer at a rate of 0.1-0.2 $Å \cdot s^{-1}$. Gold electrodes were then thermally evaporated through a shadow mask at a rate of 0.1 $Å \cdot s^{-1}$, with a channel length of 30 μm and width of 1000 μm. Gold was chosen as the source and drain contacts due to its high work function which is beneficial for hole injection and transportation.[35]

2.4. Characterization

The thickness of HfO_2 films were characterized by the ellipsometer (Rudolph Research Auto/EL). Grazing incidence X-ray diffraction (GIXRD) patterns of the deposited films were recorded using a Philips X'Pert X-ray diffractometer using Cu Kα radiation (λ = 1.5406 Å). The film morphology was investigated by atomic force microscope (AFM, Veeco Multimode V) through tapping mode. The electrical characterization of the memory devices has been measured by a Keithley 2612 source meter in a glove box filled with N_2 at room temperature.

3. Results and discussion

In this work, the thickness, phase information as well as morphology of the HfO_2 charge trapping layer were studied in detail as these properties have significant effects on the device performance.

To investigate the effects of crystallinity and thickness of HfO_2 charge trapping layer on the performance of memory device, structure shown in Fig. 1a, two set of HfO_2 films were

prepared via spin-coating at various speed and then annealed at various temperatures. Fig. 1b presents the variation of thickness of HfO_2 films obtained at different conditions. Set 1 (blue line) indicates films prepared at a same spinning speed of 3000 rpm with different annealing temperature from 200 to 500 °C, and set 2 (red line) indicates films prepared at an annealing temperature of 500 °C with different spinning speed from 500 to 3000 rpm, respectively. For set 1, the thickness of HfO_2 films decreases from around 28 to 21 nm as the temperature reduces. Further, for set 2, the thickness of HfO_2 films decreases from around 29 to 21 nm. These results show that more crystals are formed with well intact crystalline grains at higher annealing temperature for set 1. Meanwhile, larger centrifugal and air shear force led to the formation of thinner precursor layers at faster speed for set 2.

Fig. 1c shows the XRD pattern of HfO_2 films of set 1 with preparation conditions shown in section 2.2. As can be seen from the figure, no obvious diffraction peaks can be found for the films prepared at 200 or 300 °C as the temperature is too low to form crystalline HfO_2. As shown in Fig. 1e and Fig. 1f, two typical diffraction peaks around 28.2° ($\bar{1}11$) and 31.6° (111) ascribed to monoclinic phase[39, 40] could be found when the temperature increases up to 400 °C. The structure of monoclinic HfO_2 is given on the top right of Fig. 1a. There is no significant enhancement in the peak density and well agreement with the results reported by Wang *et al.* [39]. Therefore, the maximum temperature was fixed at 500 °C in this study.

We further examined the morphology of the spin-coated HfO_2 films. Fig. 1d and Fig. 1e present the AFM images of HfO_2 films spin-coated at speed of 500 rpm and 3000 rpm followed by annealing at 500 °C. The scanned area is 1 μm × 1 μm. From Fig. 1d and Fig. 1e, no obvious defects and no remarkable differences could be found. Further, the root mean square (rms) is found to be 0.559 nm and 0.620 nm for the films shown in Fig. 1d and Fig. 1e, respectively.

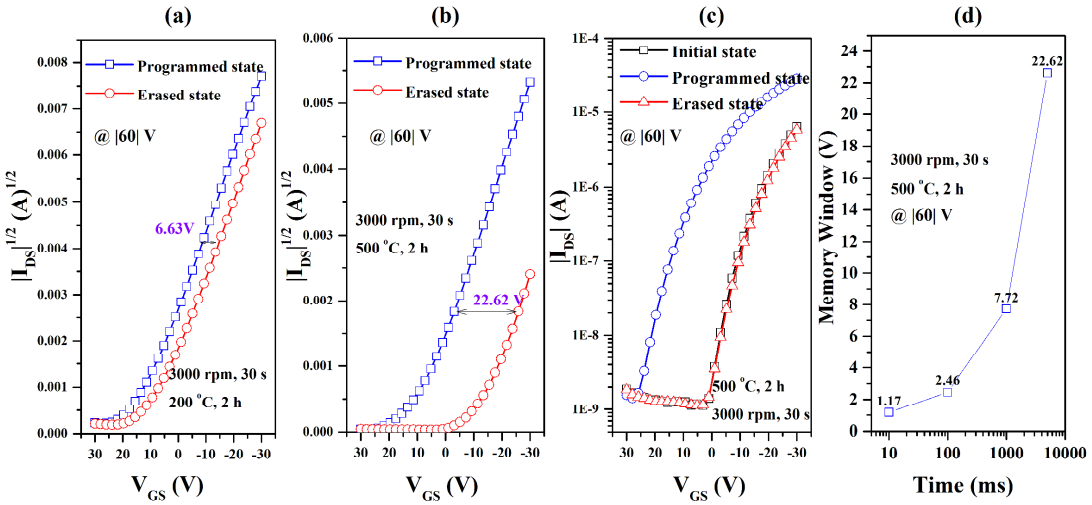

Fig. 2 Transfer characteristic of memory devices with HfO_2 spin-coated at 3000 rpm and annealed at (a) 200 °C and (b) (c) 500 °C, the program and erase voltage are +60 V and -60 V for 5 s, and (d) the relationship of program/erase time and the memory window of the device with HfO_2 spin-coated at 3000 rpm and annealed at 500 °C.

We first investigated the effect of annealing temperature on HfO_2 film for memory devices. The memory transistors with HfO_2 annealed at 200 °C and 500 °C were fabricated and transfer characteristics of these two memory devices are shown in Fig. 2a and Fig. 2b. The programming and erasing bias pulses were set at +60 V/-60 V for 5 s. A significant shift of the threshold voltage (V_T), which is determined from the intercept of the plot of $|I_{DS}|^{1/2}$ versus the gate-source voltage (V_{GS}), can be observed after applying the positive gate pulse. The memory window, ΔV_T, is defined as the change of V_T in program/erase operations. As shown in Fig. 2a and Fig. 2b, a larger memory window of 22.62 V is obtained for device with HfO_2 prepared at higher temperature. Furthermore, as shown in Fig. 2c, it is found that the transfer curve shifts towards negative voltage direction when a positive voltage is applied on the gate electrode, which proves that HfO_2 act as trapping element of electrons. Saturation mobility is determined from the slope of transfer characteristics $|I_{DS}|^{1/2}$ versus V_{GS} at drain-source voltage (V_{DS}) = -30 V by using the equation, $I_{DS} = (WC_{OX}/2L)\mu(V_{GS} - V_T)^2$. For the memory device at initial state, the transistor has a carrier mobility (μ) of ~1.02 $cm^2 \cdot V^{-1} \cdot s^{-1}$, a threshold voltage ($V_T$) of 12.11 V and an ON/OFF current ratio of over ~10^3, as shown in Fig 2c.

In addition, we tested the effect of spinning speed on the memory window of devices fabricated via spinning speed ranging from 500, 1000, 2000, to 3000 rpm. The values of memory window were determined to be 5.29 V, 8.18 V, 11.15 V and 22.62 V as shown in Fig. S1, which proves that thinner HfO_2 film traps charges efficiently in comparison with thicker films. The results revealed that the thickness of HfO_2, which was confirmed in Fig. 1b, has to be optimized to obtain superior memory characteristics. We proposed that the electric field is larger for thinner HfO_2 layer so that the electrons are easily injected in or pulled out during programming or erasing

operation. Therefore, thinner HfO_2 film obtained through either increasing the spinning speed or annealing temperature would lead to the enhancement of its charge trapping ability.

The relationship between memory window and operation time for the devices based on HfO_2 which was spin-coated at 3000 rpm and annealed at 500 ^oC was demonstrated in Fig. 2d. The memory window shifts from 1.17 V, 2.46 V, 7.72 V to 22.62 V as the programming/erasing time increases. The results show that the current memory device can be operated within a short time effectively and larger memory window can be achieved by extending the duration. In comparison with previous reports, utilizing HfO_2 nanoparticles as charge trapping layer, the devices found to operate faster.[31] Besides, the device based on HfO_2 with lower annealing temperature (100 ^oC) has been demonstrated in Fig. S2. Furthermore, we fabricated a low temperature solution processed HfO_2 layer on a thin Al_2O_3 blocking dielectric layer and the operating voltage are reduced to +5/-5 V, as presented in Fig. S3.

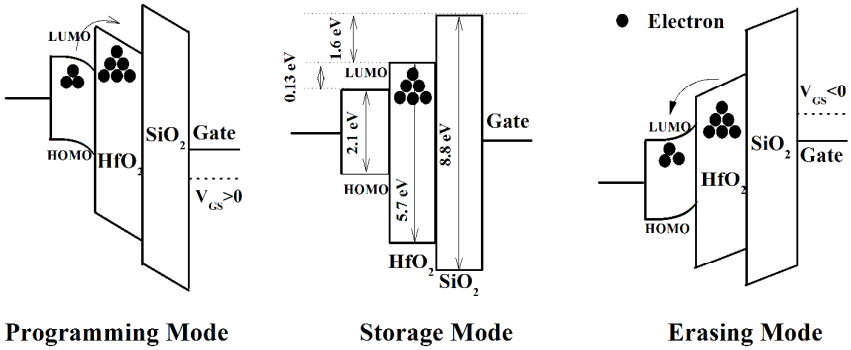

Fig. 3 The corresponding energy diagram of programming, storage, erasing modes of the fabricated devices

Fig. 3 shows the schematic energy diagram for the device in programming, storage as well as the erasing modes.[35] According to the shift direction of the transfer curves, the HfO_2 acts as an electron trapping element from the lowest unoccupied molecular orbitals (LUMO) of pentacene during programming operation when a positive voltage is applied to the gate. After programming, the electrons will be kept in the trapping sites of HfO_2 and flow back to the LUMO if a negative voltage is applied to the gate. In addition, it worth noting that HfO_2 acts as a tunneling dielectric layer as well as charge trapping element enhancing the program efficiency without an additional tunneling layer.

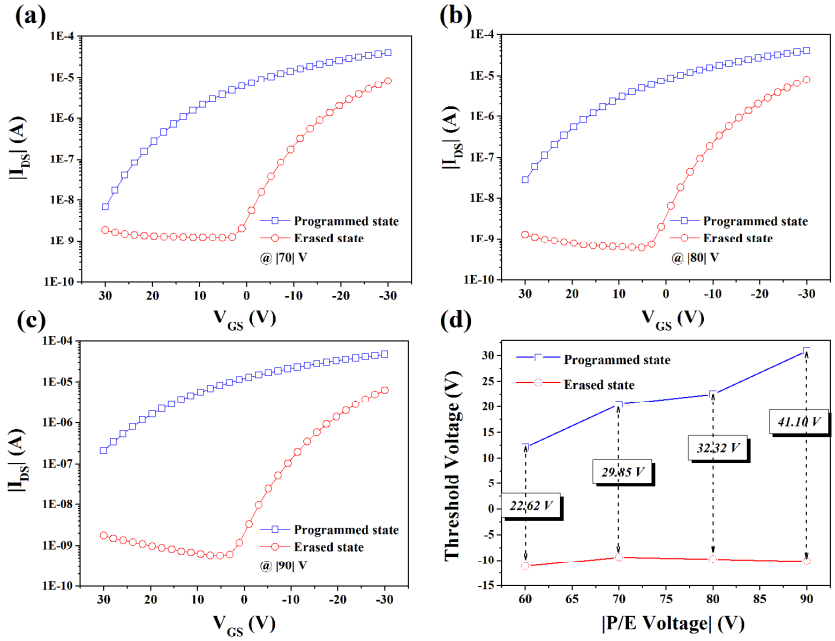

Fig. 4 I-V characteristics of devices based on HfO_2 layer (spin-coated at 3000 rpm for 30s and annealed at 500 ^oC for 2 h) under program/erase voltage at |70| V, |80| V, |90| V for 5 s, respectively.

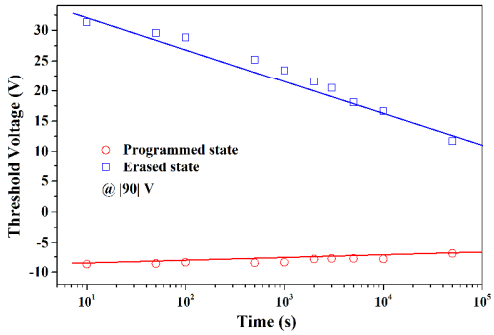

Fig. 5 The threshold voltage variation of device with HfO_2 layer spin-coated at 3000 rpm and treated at 500 °C as a function of elapsed time.

As explained in the previous discussion, the device with HfO_2 prepared at 3000 rpm and 500 °C achieved the largest memory window. We also tested the devices using various gate bias voltages from |60| to |90| V with increments of |10| V. The respective transfer curves are presented in Fig. 2c, Fig. 4a, Fig. 4b and Fig. 4c. The memory window is found to be 22.62, 29.85, 32.32 and 41.10 V with increasing program and erase voltage as shown in Fig. 4d, which is due to the increment of electrons extracted from the pentacene at larger electric field. Besides, the ON/OFF current ratio at zero gate voltage is found to be 1.15×10^3, 2.02×10^3, 2.23×10^3, and 6.56×10^3 for various gate bias voltages. These results indicate that our memory device work at the non-destructive mode perfectly at zero gate voltage for reading operation.

In order to investigate the data retention property of the memory device, the threshold voltage of a typical device with HfO_2 layer (spinning speed of 3000 rpm and annealed at 500 °C) as a function of time was measured and the result is depicted in Fig. 5. The programmed/erased states were obtained at an applied bias of ±90 V for 5s. As illustrated in Fig. 5, both the programmed and erased states degraded slowly with time. Overall, the memory window of this device is well maintained for more than 10^5 s. The memory window after 10^5 s is around 44.5 % of its initial state, which is comparable with the reported results of device using Si_3N_4 or HfO_2 layer.[23, 31, 41] Furthermore, the detailed retention and operation voltage of our devices compared with the other reported values are given in Table S1 and Table S2.

4. Conclusions

In summary, HfO_2 charge trapping layer has been fabricated using sol-gel and spin-coating method. We systematically studied the memory effects with respect to various fabrication conditions. The memory window becomes larger with higher HfO_2 annealing temperature or faster spinning speed, which mainly results from high crystallinity and thin film thickness. Moreover, after 10^5 s, the memory devices retained 44.5 % of stored charges compared to its initial state. These results indicate that solution proceed HfO_2 is a promising candidate as a charge trapping layer in flash memory.

Acknowledgement

This work was financially supported by Shenzhen Municipality project no. JCYJ20120618115445056 and City University of Hong Kong project no. 7002853.

Notes and references

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† Electronic Supplementary Information (ESI) available: [details of any supplementary information available should be included here. See DOI: 10.1039/b000000x/

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