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Engineering Silicon Crystals for Photovoltaics

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Abstract

Silicon has remained the material of choice for both microelectronic and photovoltaic (PV) industry for a few decades. In addition to its abundance, silicon can be refined to extremely high purity and grown into large dislocation-free single crystals that meet the stringent requirements of modern electronic devices in many applications. On the other hand, the customized silicon crystals, with less purity and perfectness, grown by the high-throughput directional solidification at low cost that could meet the high performance needs for solar cells have rapidly driven the PV development in the past decade. In this highlight, we review the recent engineering efforts in the state-of-the art industrial production for the customized silicon crystals, including quasi-mono and multi-crystalline silicon (mc-Si). Special attention will be focused on the so-called high-performance (HP) mc-Si that has become the mainstream material for solar cells since 2012.

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1. Introduction

Silicon is next to oxygen the most abundant material on earth. With the emergence of semiconductor industry since 1950's, silicon has be produced with extremely high purity, up to 11 N, and large dislocation-free silicon single crystals, up to 18 in, can be grown by the Czochralski (Cz) method[1]. The Cz-grown mono-crystalline silicon crystals have been used mostly in micro-electronics for very large integrated circuits (VLSIs) and in solar PV[2] for high-efficiency solar cells. On the other hand, for most of solar PV applications, especially in the solar power plant, silicon crystals need to be customized, having a high performance/cost ratio, to reach the grid-parity target. The directional solidification (DS) has emerged as a key production technology to grow the customized silicon crystals, especially the mc-Si, for the past decade[3-4]. In 2015, the annual PV installation was over 50 GW, and the DS mc-Si solar cells shared the market near 60%[5]. More importantly, the ingot quality has also been improved significantly in the recent years, especially the so-called HP mc-Si technology[3-4]; the term of HP was given by industry in terms of solar cell efficiency, production robustness, and cost. The champion mc-Si solar cell has reached 21.25% recently by Trina Solar, based on the HP mc-Si[5-6]. The average production solar cell efficiency could be easily over 19.5% with the advanced cell technology[5-6]. Although mc-Si has been developed for more than 30 years, as a tradition material for PV, the newly developed technology for HP mc-Si in crystal growth is indeed a teach-away approach. The ideas behind may shed a light to our crystal engineering community a different way of thinking in the development of industrial technology. And the innovation, even in a traditional field, could have a big impact to human being. In this article, engineering the silicon crystals to meet the cost-effective needs for PV is reviewed. We will discuss first the current DS technology used in industrial production and then the related defects during ingot growth in the next section. In Section 3, the control of nucleation and grain growth for growing high-quality ingots is reviewed. The current status of mono-like technology will also be discussed. The HP mc-Si is focused in Sec. 4, before the conclusions and outlook are drawn in Sec. 5.

2. Ingot growth and the related defects

2.1 Ingot growth

The DS technology for mc-Si has been developed for more than 30 years[3,7]. Nowadays, the normal silicon charge per run for a Gen 6 furnace used in production is around 800 kg; a Gen 6 ingot could be cut into 6x6 bricks for wafer slicing (156mmx156mm in size for the standard solar cells). In 2006, the normal size was only Gen 4 having a charge of 270 kg. The schematic of the DS silicon ingot growth is shown in Fig. 1(a). The hot zones for different generations are similar. Nevertheless, as the crucible dimension becomes bigger, the top heater becomes essential. The photograph shown on Fig. 1(b) is a Gen 7 DS station during loading, and the inset photo is a 1.2-ton ingot after crystal growth. The furnace is designed to melt silicon and to control its solidification in the upward direction. Therefore, the heater shape and the insulation layout, i.e., the hot zone, are very important, especially to keep the solidification front slightly convex[3]. The ingot growth is at a reduced pressure (~0.6 atm) flushed with argon to protect the hot zone, mainly made of graphite, from oxidation. The crucible is placed upon a graphite block, which is cooled by thermal radiation as the insulation basket, made of graphite felt, moves upwards. The power consumption of DS silicon is rather low, about 10 kWh/kg, and the labor cost is low as well. In 2012, Gen 8 growth with a charge of 1.65 tons has also been demonstrated by MEMC Co.[8]. The dimensions and normal throughputs for different generations of the DS furnace are summarized in Table 1. In a typical production procedure, solar-grade (SoG) polysilicon, having purity more than 7N[9], as well as the doping material, is loaded in a Si_3N_4-coated quartz crucible, which is placed inside a graphite case, and then covered with a graphite plate. The cover plate, as shown in Fig. 1(a), is important in the control of impurities, particularly carbon[10-11]. During crystal growth, flushing argon, through the hole of the cover plate, is to carry away SiO evaporated from the melt; SiO is due to the reaction of silicon melt and the silica crucible, i.e., $SiO_2+Si= 2SiO$. The evaporated SiO could also react with the graphite in the hot zone forming CO, i.e., SiO+C=SiC+CO. Hence, the argon flow is used to prevent the back diffusion of CO from the graphite parts. Usually, it takes about 20 h to melt the material in the crucible. As the melt is stabilized, the insulation basket shown in Fig. 1(a) is moved upward to control solidification; the growth rate is at around 1 cm/h. After the ingot is solidified completely, the insulation is lowered down again for annealing. As the temperature is below 800 ^{o}C, the insulation is moved upward again to accelerate the cooling process. The whole growth cycle for a Gen 6 furnace takes about 70 h including the meltdown, crystal growth (30–40 h), annealing, and cooling down procedures. Up to now, pretty much all the mc-Si wafers available in the market are boron-doped, i.e., p-type. The resistivity of the wafers is around 1 (top) to 2 Ω-cm (bottom). For a Gen 6 ingot, the growth yield is around 70%, after cutting off the red zone, i.e., the area in the edges having low minority lifetime due to the contamination from the coating/crucible, as well as the area near the top surface due to the segregation of impurities. About 27000 wafers, 200 μm thick, could be sliced from a G6 ingot. In other words, a Gen 6 furnace could produce 3-million wafers per year, which corresponds to 12.8 MW in terms of solar cell power output. The high throughput, 8 times higher than a normal Cz growth, and the nearly automatic growth give the DS technology a cost effective solution for PV silicon. In practice, using the lager furnace has several advantages. In addition to the higher throughput, the contact area per volume decreased linearly with the ingot width. As a result, the totally impurities from the crucible/coating materials and thus the red zone also decrease. Moreover, most of the silicon cut off from the ingot, except a small portion near the top surface, could be recycled. Therefore, nowadays the polysilicon usage has been reduced to about 5.6 g/Wp. Because producing polysilicon, usually by Siemen's process, is most energy intensive, the reduction of the silicon usage is crucial to the energy payback time. Depending on the system position, the energy payback time ranges from 0.7 to 2 years[5]. In other words, for a PV system, which could be used in general more than 20 years, the energy used for producing the mc-Si solar module could be paid back in two years.

2.2 Impurities and related defects

To reduce cost, the materials used for DS silicon are less pure than that used in Cz. For example, quartz is also used as the crucible material for DS silicon, but it is produced by slip casting using the raw silica sand contains metals up to several tens of ppm[12]. To prevent the sticking with the solidified silicon, the silica crucible needs to be spray coated with silicon nitride (Si_3N_4). Although it is purer than the crucible, the level of impurities, mainly B, P, and Al, is still several ppm. The purity of the graphite materials used for the hot zone in DS is low as well. As a result, during crystal growth impurities are introduced from the crucible/coting materials[13-15], as well as the hot zone[16]. Besides the impurities, structure defects, such as dislocations and grain boundaries (GBs), are also introduced during ingot growth, and the structure defects could propagate and further interact with the impurities during crystal growth[17-18]. These defects, especially dislocations, are usually the recombination centers for the light generated electrons and holes and therefore are harmful to the solar cell performance. The balance between the cost and the ingot quality is indeed a critical factor in production; as mentioned previously, most of red-zone silicon is recycled, of course mixed with the SoG Si. The interplays of the hot-zone design, nucleation, crystal growth, segregation, and the species transport are also quite complicate. Nevertheless, with booming of PV industry in recent years, engineering the customized mc-Si has led to a dramatic progress in production[3-4].

In addition to B, Al, and P, other metal impurities, such as Fe, Co, Ni, and Cr, are quit common in mc-Si, and again they are mainly from crucible/coating materials; some might come from the silicon feedstock[2]. During crystal growth, the extended defects usually getter and store the majority of the mobile metallic impurities, leaving rather few active metals in the intragrains[18-20], and engineering these defects opens a new era of using low-purity silicon for solar cells[21-22]. Some of these active metals, such as Ni, Cu, Fe, and Co, are extremely detrimental to minority lifetime and need to be controlled carefully during crystal growth[23]. If not, the fast diffusion metals could be further gettered during cell processing, particularly during the emitter formation by $POCl_3$ diffusion. However, their gettering efficacy is affected by precipitates, particularly at GBs[23-24]. Moreover, these metals usually tend to segregate to GBs, but this depends on the boundary types. The non-coherent GBs having high coincidence site lattice (CSL) indices, i.e., Σ values, could easily getter the rapid diffusion species such as Fe, Ni, and Cu[23-24]; the dangling bonds in GBs provide more relaxed space to attract metals. This makes these GBs electrically active for recombination of electrons and holes. On the other hand, for $\Sigma3$ GBs, typically they are not associated with the impurities[25-27], and they are electrically inactive. Nevertheless, if $\Sigma3$ GBs are decorated by dislocations, they could also be electrically active containing fast-diffusing metals[18]. The small angle GBs were also found to have better gettering capability than the large angle GBs[28]. In view of this, it had been long recognized that it was necessary to obtain large grains in DS silicon with fewer GBs; even with GBs, Σ3's were preferred. As HP mc-Si emerged, this viewpoint was demolished[3-4].

Besides, light elements, such as N, O, and C, are also common impurities in DS Si. N and O come directly from the Si_3N_4 coating and the silica crucible. In addition to the reaction of silicon with the oxygen in silicon nitride, silicon melt could infiltrate into the coating layer and further react with the silica crucible forming SiO. The SiO dissolves into silicon melt and then evaporate from the melt surface. As a result, the oxygen content is the highest, about 3 to 10 ppma, at the bottom and the lowest, about 1 ppma, at the top of the ingot because the melt/crucible contact area decreases with the solidification. On the other hand, the introduction of C is less direct. Carbon, mostly in the form of CO, is from the gas phase through the reaction of SiO and the graphite parts in the hot zone. After reaction, CO could then diffuse back to the melt[10-11], but the use of argon flushing could significantly reduce the C content in the melt and thus in the grown crystal. During ingot growth, the supersaturation of these light elements further drives the formation of the precipitates of oxide, nitride, and carbide, and they are also harmful to ingot quality. The oxygen and its precipitates are less harmful in mc-Si. However, the oxygen in the boron-doped silicon forms boron-oxygen pairs that could cause light induced degradation (LID)[28]. Although the oxygen content in mc-Si is not as high as that in Cz silicon (>10 ppma), some LID is still observed in commercial p-type mc-Si cells, particularly using the upgraded metallurgical silicon feedstock. As the oxygen content is than 3 ppma, no significant LID is observed[30]. According to the calculation by Matsuo et al.[31], the equilibrium oxygen concentrations in mc-Si is about half of that in Cz silicon. The oxygen in mc-Si is present in either interstitial atoms or silicon oxide precipitates. They are often gettered by the extended defects as well. Furthermore, the accumulation of oxygen at dislocations often leads to the nucleation of small SiO_2 precipitates due to the strain fields. However, in DS Si, oxygen never reaches the saturation level, and its precipitates are less significant as compared with carbon and nitrogen[32].

On the other hand, N in the melt often exceeds its solubility limit (about 128 ppma) due to its low segregation coefficient ($7x10^{-4}$)[33-34]. Once silicon nitride supersaturates and nucleates, due to its large diffusivity in the melt, large Si_3N_4 precipitates could grow in the form of long filaments, needles, or tubes up to several mm[32-33]. In addition, nitride particles could also come off from the powdery coating. In both cases, the precipitates or particles could be pushed by the moving solidification interface, and finally swallowed in forming inclusions. The precipitates near the growth front could be greatly reduced by increasing melt convection and decreasing the growth rate. Both help the reduction of the inclusions in the grown ingot[34]. Nitrogen and its precipitates are not electrically active and they are less harmful to solar cells. Also, large Si_3N_4 precipitates could be easily seen by infrared transmission imaging, a standard ingot inspection tool in production[33, 35].

Carbon is also less electrically active, but SiC precipitates from supersaturated carbon in the melt could cause wire breakage during slicing and shunting in solar cells. SiC precipitates in mc-Si ingots after crystal growth could also be easily visualized by infrared; the precipitates appear as dark contrast[34-35]. Figure 2 (a) shows the infrared image of a small G1 ingot grown from small silicon chips and a (100) mono-crystalline silicon seed[35]. The dark contrast was cause by SiC and Si_3N_4 precipitates. The segregation of carbon plays a crucial role in the formation of SiC precipitates. As carbon is supersaturated in silicon melt to a certain degree, SiC nucleates and grows; very often Si_3N_4 particles from the coating could be the nucleation sites of the precipitates. SiC precipitates could grow up to several mm, and the rod- and planar-like strictures have been observed for SiC[32]. Again, they seem to prefer to nucleate heterogeneously at the GBs As shown in Figs. 2(b) and (c), the SiC rods, as well as array of Si_3N_4 fibers, were often found at GBs, while Si_3N_4 filaments decorated with SiC particles were found in the intragrains, as shown in Fig. 2(c). The solubility limit of carbon in silicon melt is about 100 ppma, which gives the solubility limit in solid is about 7 ppma for the segregation coefficient of 0.07[33,34]. By considering a non-graphite crucible cover, Gao et al.[10] have grown an ingot with a very low carbon concentration. Again, with the enhancement of convection, the formation of SiC precipitates in the ingot, except at the end of growth, could also be minimized[34].

2.3 Dislocations and clusters

In addition to impurities, dislocations and their clusters are very electrically active for mc-Si solar cells; the dislocation clusters usually have an etch pit density (EPD) higher than 10^6/cm^2. Most dislocations in mc-Si are generated by plastic deformation at high temperature (>800 ^{o}C) for thermal stress relaxation during crystal growth. The thermal stress is caused by thermal gradients, but they are needed for solidification in a period of time. According to dislocation kinetics, dislocations multiply rapidly under stress and easily form clusters, especially during crystal growth at high temperature (~1410 ^{o}C). Also, dislocations develop in a few seconds, even though silicon stays at high temperature for tens of hours. As the dislocations appear and propagate upward with ingot growth, the crystal quality deteriorates quickly with height. The dislocation bundles could extend over a few centimeters. Figure 3(a) shows a lifetime mapping of the cross section of a grown G5 ingot (500 Kg). Except the red zone near the edges, which was due to the metals as discussed previously from the crucible/coating, the low-lifetime regions initiated from the bottom and propagated to the top are due to dislocation clusters. Because dislocations were bounded by GBs, especially random GBs, the lifetime images followed the grain structures closely. Therefore, from the lifetime mapping, the grains also grew upward, and this indicated that the solidification front was rather flat. The grain structures from the middle brick of the ingot are shown in Fig. 3(b). As shown, large grains could be induced at the bottom but the grains were not uniform. This is rather typical for DS because the grain size and its distribution are affected by undercooling, and the undercooling is also sensitive to coating conditions[3-4]. As the growth proceeded, some grains grew bigger, but some small equiaxed grains also appeared, which often nucleated from the subgrains induced by dislocation clusters[36-37]. More importantly, as shown in Fig. 3(c), the high-defect area revealed by acid etching increased rapidly from the bottom to the top of the ingots; the dark area had an EPD greater than 10^6/cm^2. These massive defects are detrimental to solar cell performance. In general, if the dislocation density could be controlled under 10^4/cm^2, its effect on the minority lifetime becomes small[38].

To control dislocations, the understanding of dislocation kinetics is necessary. In mc-Si, most of dislocations nucleate at low-symmetry random GBs[17, 39]. Besides, the stress concentration caused by the anisotropic thermal expansion among grains or the lattice distortion around precipitates[39-40], such as SiC and Si_3N_4, may also be the main driving force for dislocation nucleation. With these dislocations, as the ingot grows higher, dislocations multiply due to plastic deformation under thermal stress; meanwhile the thermal stress is thus relaxed. Because of high temperature, recovery is also possible. The multiplications and recovery of dislocations continue at high temperature until the end of annealing stage. Due to the long growth time of DS mc-Si, the further ingot or wafer annealing has little effect on dislocations, both on their density and structures[41-43]. In other words, as the ingot is grown, it would be very difficult to remove the dislocation clusters by thermal treatment, and this behavior is very different from metals. To illustrate this, Reimann et al.[43] carefully designed the experiments and revealed the dislocations by various etchants recently. They found that the thermal treatment of DS mc-Si wafers at high temperature, up to 1465 °C for 96 h, with and without applied stress of up to 4.2 MPa, had little effect on the reduction of dislocation density. This further indicates that as the dislocations exist in the grown ingot, which are likely from the grow-in dislocations[42], and they could not be removed easily by the post thermal treatment. Some dislocations might also be induced during annealing process, but they their impact to lifetime is not as high as that induced during growth stage.

Reducing the nucleation sources of dislocations and the thermal stress is useful in reducing dislocations. The control of initial grain nucleation and growth behaviors by high undercooling for more twin boundary formation has been proposed, and the results are very promising for small ingots[45-47.] For larger ingots, some success has also been reported recently[48-50]. However, the progress of this approach in production seems to be slow. On the contrary, by using a very different concept, Lan et al.[4,51-53] has made a significant success in reducing the defect propagations by initial grain control through an incubation layer, which will be discussed shortly. They observed that the small and uniform initial grains with a high percentage of non-coherent random GBs seem to very effective for stress relaxation during crystal growth, especially for large ingots. The success of this work increased the average mc-Si solar cell efficient in production from 16.6% to 17.2% in 2011[4, 37, 51-53]. Thenceforth, the name of "HP mc-Si" has been adopted for this technology. With this technology, SAS Co. branded the A+ wafers; currently A5+ wafers have been released. Using similar technology, GCL and LDK have also branded their S4 and M4 wafers, respectively. Interestingly, since 2012 most of the branded wafers available in the market have similar grain structures. Moreover, the yield stress at high temperature (>1000 °C) is only about a few MPa[53-55], where the thermal stress in the ingot during ingot growth is usually an order of magnitude higher[57-59]. Therefore, under this thermal stress level, dislocations could multiply easily. Therefore, the relaxation of the thermal stress through random GBs has been found crucial to the growth of HP mc-Si ingot.

3. Nucleation and grain control

Since the beginning DS technology for mc-Si in 80's, to mimic the mono-crystalline Cz Si, tremendous efforts have been paid to grow ingot with large grains with less GBs[7, 60]. However, mc-Si induced by undercooling has many grains with different orientations and sizes, as well as many GBs with different characteristics, and their control is rather difficult. Moreover, the dislocations are closely related to grain orientations and grain boundary types[39, 46, 61]. GBs could also lead to different mechanical and electrical characteristics under different orientations[62-64]. In addition, the dislocation density is also much lower for the grains containing twins or in certain orientations[46, 61]. The gettering efficacy of metals in the post cell processing is also affected by the GBs[24]. As we have discussed previously, the minority lifetime and thus the solar cell efficiency correlate closely with the dislocation density[38], and the amount of dislocation clusters (EPD$<10^6$/cm^2). Therefore, with these observations, it is rational to obtain mc-Si having large grains with the favored orientation, as well as GBs with preferred characteristics, for high-efficiency solar cells. To achieve these, the nucleation and grain control becomes very important during ingot growth. The recent results showed that the high initial cooling could induce the dendritic growth that could lead to larger grains with better quality[45-50, 65]. This approach is the so-called dendrite casting method, proposed by Nakajima's group at Tohoku University, as illustrated in Fig. 4(a)[45, 49-50]. The comparison of the grain size and orientation of the conventional and dendrite casting methods is shown in Fig. 4(b). The <110> dendrites give the growth orientation (upward) mainly in <112>. This approach was rather popular for quite some time.

Wang et al.[66] and Yeh et al.[46] further proposed spot cooling, and the idea was easily implemented in an industrial-scale furnace using a patterned cooling pad. Their dendrite casting method also gave a high percentage of twin boundaries; 80% of Σ3 GBs were obtained by Yeh et al.[46]. Nakajima et al. further[67] proposed a cooling pad with different thermal conductivities to control the dendrite arrangement in the same direction; large dendrites up to ten's of centimeters were obtained.

Beside the dendrite casting method, the most direct way to control crystal orientations and GBs is the seeded growth, which has been widely used in single crystal growth. In the early days of DS silicon, seeded growth was considered first[68-69], but the ingot quality was not as good as expected. The major problems were: (1) nucleation from the crucible wall; (2) the generation and multiplication of dislocations, especially from the seed. The seeded growth for DS silicon was pretty much discarded until 2006. A research group at BP Solar reported the growth of large DS grown mono-crystalline ingot using splitting seeds, the so-called quasi-mono or mono-like method[70-71]. BP Solar branded its quasi-mono wafers as "Mono2$^{\mathrm{TM}}$" in early 2006. However, the quasi-mono wafers didn't receive much attention until 2011. Recently, Vuchovska et al.[72] and Gu et al.[73] also showed impressive results by tuning the growth recipes. Trempa et al.[74] did a systematic study to understand the new grain formation from the wall and the junction of splitting seeds. They reported that the <100> direction, which is the orientation needed for texturing in solar cells, turned out to be the most difficult one. The twin nucleation at the (111) facets played an important role in the formation of mis-oriented grains. Therefore, controlling the convex interface near the crucible is crucial to avoid the faceting for twinning. Nowadays, with the improved hot zone for the control of the grown front, the yield of mono-like ingot growth has been significantly improved to be over than 90%, especially with the use of the partition insulation block[75-77]. Furthermore, Kutsukake et al.[78] further proposed an interesting idea using the so-called functional grain boundary, i.e., Σ5 GB by rotating the seed around <100> axis by 36.8°, near the crucible wall to block the mis-oriented grains nucleated from the crucible wall. Nevertheless, the dislocations generated from the seed joints and their multiplications under thermal stress remain the key issues in production. Figure 5 (a) shows the lifetime mapping of a Gen 2 mono-like ingot[79]. As shown, the defects generated from the joint of two reused seeds. Interestingly, the dislocations structures existed in the seeds turned out to have similar defect structures[79]. Successful growth of Gen 6 mono-like ingots has also been report by Jouini's group at INES, France, as shown in Fig. 5(b)[79], and as they claimed that the yield of mono-like ingot was near 100%, and the defects from the seed joints were suppressed by a special technique. Although the (100) mono-like wafers have the advantage in the cell processing using alkaline etching, which generates pyramid texture for better light trapping in solar cells, the dislocation clusters significantly reduce the ingot yield in production. This technology attracted much attention since 2011[80]; however, it stayed in the market only for a short period time. As the HP mc-Si technology emerged in 2011[2, 4, 6, 51-53], the mono-like wafers pretty much disappeared after 2012.

Nevertheless, research efforts still continue for the mono-like technology. Recently, the dislocation generation from the seed joints has been mitigated significantly by special seed arrangements using low-symmetry random GBs[81-83]. Hu et al.[81] purposely introduced the random GBs by twisting the angle between the adjacent (100)-oriented seeds by 10 to 45°. From their G5 ingot growth, the dislocations generated from the seed joints were significantly reduced. By combining the concepts of small- and large-angle GBs and the functional grain boundary[78], Takahashi et al.[83] proposed a novel seed manipulation for artificially controlled defect technique (SMART), and the results are shown in shown in Fig. 6. The tilt grain boundary was introduced for the seed joints to minimize the dislocation generation, while the small angle (SA) GBs were introduced to relax the thermal stress by dislocation generation. In addition, the Σ5 functional GBs were introduced to block the mis-oriented grains from the crucible wall. As shown in Fig. 6, the central area had much less dislocations after the ingot growth.

4. HP mc-Si

As mentioned previously, to mimic the mono-crystalline Si, extensive efforts have been devoted to control the nucleation and growth for large grains with preferred boundaries, such as the dendrite casting[45, 49-50] and the mono-like method[70-75, 79, 81-83]. However, as they were applied for industrial scales, up to G5 or more, the multiplication of dislocations was difficult to control, and this led to low ingot yield. The distribution of solar cell efficiency also had a long tail due to the dislocation clusters. During the development of the dendrite casting method, we obtained very small grains at the beginning incidentally. It turned out that with the small grains the multiplication of dislocation clusters was significantly reduced, and the ingot lifetime was uniform[4, 51-53]. With small silicon particles, 2 to 5 mm in diameter, as the seeds, the small and uniform grains could be easily controlled[3-4, 51-53]. Surprisingly, the percentage of non-coherent GBs was high, but the solar cell performance was better. The patent for such grain structures in the ingot and wafer was filed in 2011 and granted in 2014[84], the examples in the patent used silicon and non-silicon particles as the seeds. After this finding, different approaches for getting such a grain structure have been explored[5]. There are a few ways to induce the small and uniform grains. In addition to the control of initial undercooling, the most robust one is to use an incubation layer[3-4, 53, 84-86]. The layer could be consisted of silicon (homo-seeded)[84-86] or other non-silicon (hetero-seeded) particles[5, 84, 87-88]. Zhu et al[84] from JA Solar claimed they proposed the seed-assisted approach for HP mc-Si, but the method was already disclosed in our patent[84], which was opened to public in May, 2013, earlier than their submission date. Using notched or patterned crucibles is also feasible[6, 89]. Nevertheless, the homo-seeded approach is still the most robust one in production. The characteristics of the HP mc-Si wafers have been investigated[4, 90-92]. Figure 7(a) shows the lifetime mapping of a HP mc-Si ingot, grown from small silicon particles (2 to 5 mm in size)[4]. As shown, the lifetime was very uniform, as compared with that shown in Fig. 3(a); the low-lifetime areas due to the dislocation clusters were significantly reduced. Figure 7(b) shows the grain structures and the dislocation clusters taken from the wafers at different positions of the ingot. As shown, the grains near the bottom part of the ingot were small and uniform. Their size increased with the increasing ingot height. More importantly, as shown by the EPD mapping, the high-defect areas were confined inside the small grains and their propagation from the bottom to the top was often terminated by the random GBs[91].

The typical grain structures, orientations and grain boundary types, of the wafers taken from different positions of a HP mc-Si ingot are summarized in Fig. 8. As shown from the statistics, the grain orientations were mainly located in the low-energy planes, such as (111) and (112). More importantly, the percentage of the random GBs at the lower part of the ingot could be greater than 70%, and this is unusual due to their high energy. Even in the top portion of the ingot, the percentage of the random GBs was also more than 60%. Wong et al.[85] did a detailed analysis of the grain structures developed from small silicon beads (0.9 mm in diameter), and they found that the lowest-energy orientation, i.e., (111), tended to dominate during grain competition. However, the twining from the tri-junctions generated new grains with different orientations; this might be the reason for more (112) orientation at the top ingot. Indeed, the (111)- or (112)-dominated orientations, as well more random

GBs, are typical nowadays in commercial HP mc-Si wafers. The high-percentage of the non-coherent GBs shown in Fig. 8(b) upsets the previous understanding for high-quality mc-Si wafers; however, they played a crucial role in the reduction of dislocation clusters. Before this result was first reported by Lan et al.[53], most people believed that more twins or Σ3 GBs are needed for better lifetime[45-46, 61]; this was the core concept of the dendritic casting approach[45-46]. Indeed, if the wafers in Fig. 2(b) are carefully examined, one could find that the twin areas indeed have very few defects[46].

Recently, Reimann et al.[93] used different seed materials for the growth of HP mc-Si ingots. Seeds from single crystalline crushed (SCS), fluidized-bed-reactor (FBR) and Siemens (SIE) feedstock were considered; the data from convectional mc-Si (Multi) was included for comparison. They found that the fraction of highly defected areas near the top of the ingot was affected by the length fraction of non-coherent GBs, as shown in Fig. 9. The more of the random GBs from the seeds was, the less fraction of defected area near the top of the ingot. It is believed that the random GBs could terminate the propagation of dislocation clusters and help the relaxation of thermal stress[4, 91]. The amorphous nature at the random GBs due to the dangling bonds allows the slip at GBs, which might accommodate the plastic deformation required for stress relaxation. By examining the photoluminescence images of the wafers from the bottom to the top of an ingot, we also noticed that the defected grains were easier to be overgrown by others[4]. Moreover, from the recent investigation by Sio and Macdonald[94], the recombination activity of the GBs in HP mc-Si wafers (the GB recombination velocity is about 200 cm/s) turned out to be very low as compared with that in the traditional mc-Si wafers (~1000 cm/s). The reason for the low recombination activity at the GBs for HP mc-Si remains unknown, and needs further investigation. Due to its high performance in solar cells, having a very narrow distribution of cell efficiency, the HP mc-Si technology has become the main stream in silicon photovoltaics[95]. The average efficiency of back-surface-field solar cells in mass production has reached 18.3%. With the passivated emitter and rear contact (PERC) cell structure, the average solar cell efficiency of 19.5% has also been achieved[95].

5 Outlook

We have reviewed the current status of DS silicon crystals for solar photovoltaics. Engineering these silicon crystals by controlling their grain structures during crystal growth has made significant progress in recent years. For the mono-like silicon, the problems of having mis-oriented grains nucleated from the crucible wall and the defects developed from the seed joints have been mitigated by advanced hot zone and special seed arrangements. However, the adoption by industry for production may still take some time, depending on the robustness, yield, and cost of the technology. On the other hand, the HP mc-Si technology based on the small uniform nucleation has been widely used in production since 2012. The non-coherent random GBs were found to be important in reducing defects, while their recombination activity was found to be very low as well. Currently, more cost effective approaches, such as hetero-seeded through silica particles[84,88] or coating[6,87,95], have been adopted in production without using silicon particles as the seeds. The red zone near the crucible bottom can be greatly reduced[6,88,95]. Although the structure defects have been significantly reduced, the impurities from the crucible/coating materials remain the key issue that limits the solar cell efficiency, but again this is a dilemma between cost and quality. Using diffusion barriers for crucibles could be an alternative solution[96], and this kind of crucibles is available in the market. The reusable crucible, such as Si_3N_4 crucible [97-98], could be a cost effective solution as well. As the impurities could be further reduced, the efficiency gap of solar cells from DS mc-Si and dislocation-free Cz Si would be further narrowed. In such a case, the HP mc-Si will continue to dominate the PV market in the near future.

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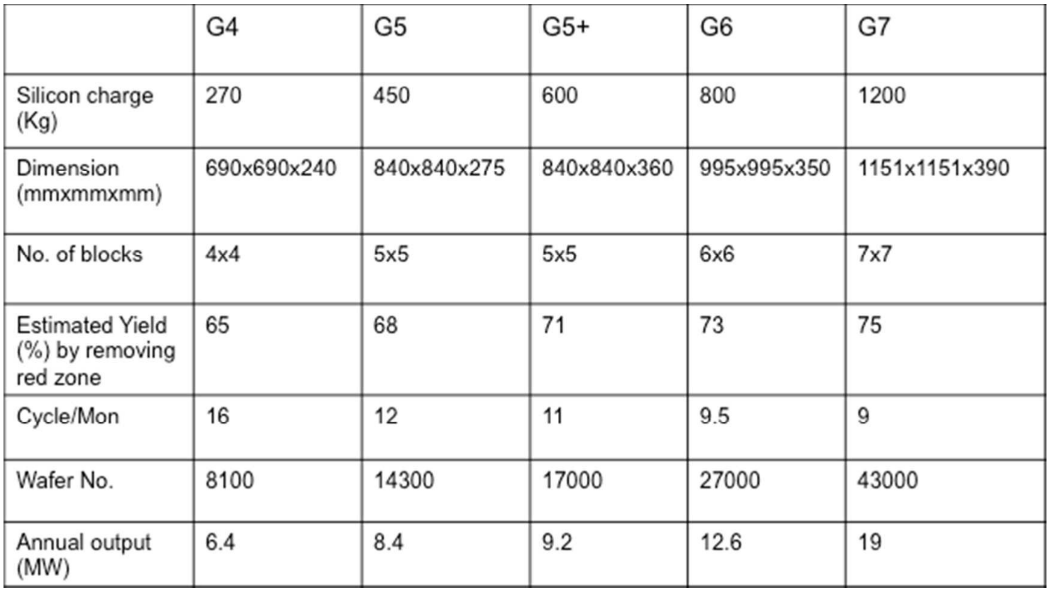
Table caption

Table 1 The generations of DS technology and their dimensions and throughputs.



	G4	G5	G5+	G6	G7
Silicon charge (Kg)	270	450	600	800	1200
Dimension (mmxmmxmm)	690x690x240	840x840x275	840x840x360	995x995x350	1151x1151x390
No. of blocks	4x4	5x5	5x5	6x6	7x7
Estimated Yield (%) by removing red zone	65	68	71	73	75
Cycle/Mon	16	12	11	9.5	9
Wafer No.	8100	14300	17000	27000	43000
Annual output (MW)	6.4	8.4	9.2	12.6	19