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Complete List of Authors:	Nourbakhsh, Amirhasan; Massachusetts Institute of Technology (MIT), ; imec, Adelmann, Christoph; Imec, TF Song, Yi; MIT, EECS Lee, ChangSeung; Samsung Advanced Institute of Technology, Asselberghs, Inge; imec, NCAIS/NAME Huyghebaert, Cedric; imec, Brizzi, Simone; Brandenburgische Technische Universität, Tallarida, Massimo; Brandenburgische Technische Universität, Schmeißer, Dieter; BTU Cottbus, Applied Physics and Sensors Van Elshocht, Sven; IMEC, Heyns, Marc; imec, Kong, Jing; MIT (Engineering), Department of Electrical Engineering and Computer Science Palacios, Tomas; Department of Electrical Engineering and Computer Science Massachusetts Institute of Technology (MIT), De Gendt, Stefan; imec,

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Amirhasan Nourbakhsh,[a, b,*] Christoph Adelmann, [a] Yi Song,[b] Chang Seung Lee, [c] Inge Asselberghs,[a] Cedric Huyghebaert,[a] Simone Brizzi,[d] Massimo Tallarida,[d,‡] Dieter Schmeißer,[d] Sven Van Elshocht,[a] Marc Heyns,[a] Jing Kong,[b] Tomás Palacios[b] and Stefan De Gendt[a]

Graphene oxide (GO) was explored as an atomically-thin transferable seed layer for the atomic layer deposition (ALD) of dielectric materials on any substrate of choice. This approach does not require specific chemical groups on the target surface to initiate ALD. This establishes GO as a unique interface which enables the growth of dielectric materials on a wide range of substrate materials and opens up numerous prospects for applications. In this work, a mild oxygen plasma treatment was used to oxidize graphene monolayers with well-controlled and tunable density of epoxide functional groups. This was confirmed by synchrotron-radiation photoelectron spectroscopy. In addition, density functional theory calculations were carried out on representative epoxidized graphene monolayer models to correlate the capacitive properties of GO with its electronic structure. Capacitance–voltage measurements showed that the capacitive behavior of Al_2O_3/GO depends on the oxidation level of GO. Finally, GO was successfully used as an ALD seed layer for the deposition of Al_2O_3 on chemically inert single layer graphene, resulting in high performance top-gated field-effect transistors.

Introduction

In recent years, the increasing limitations of the Si-based field-effect transistor technology have spurred an extensive effort to find novel channel materials. Materials such as alternative III-V semiconductors, for example InGaAs[1] or InAs[2], graphene[3, 4] and graphene-derived materials[5] as well as two-dimensional (2D) transition metal dichalcogenides such as MoS_2[6] or WSe_2[7] are of interest as they offer the potential for shorter channel transistors with higher performance than Si.

A common key issue of many field-effect devices using such alternative channel materials is the integration of gate dielectric layers with high dielectric constants into the device stack. For Si-based field-effect devices, this is commonly achieved using atomic layer deposition (ALD), which has become the reference technique for the deposition of high quality dielectric[8]. The outstanding thickness control, the high film quality and thickness uniformity, the outstanding conformality, as well as low deposition temperatures render ALD also highly suitable for the deposition of gate dielectrics on alternative channel materials. However, the direct deposition of dielectric layers on many alternative channel materials is difficult because of the chemical inertness of the surface. As a result, the dielectric films can typically nucleate only at defect sites leading to island growth and slow film closure. This is a major obstacle for the realization of high quality thin gate dielectrics on novel 2D materials such as graphene[9] or MoS_2[10] and has limited many studies to the usage of back gates. In addition, the ALD on polymers often proceeds by diffusion of the precursors into the bulk of the polymer and growth inside the film which is detrimental to the interface sharpness and the dielectric quality at the interface[11, 12].

These issues can be circumvented by the usage of a suitable seeding layer or surface functionalization. The key criteria for a seeding layer are its ability to be transferred or deposited onto the alternative channel material, its chemical compatibility with the ALD process, leading to good nucleation of the dielectric, and its impermeability for precursor gases in order to protect the underlying substrate. Furthermore, it should have only a small impact on the capacitance of the gate dielectric and thus on the performance of the field-effect device. In this paper, we propose graphene oxide (GO) monolayer as a seeding layer and we show that it fulfills all key criteria. This route can be seen as an important step in the fabrication of atomically thin Van der Waals heterostructures[13, 14] where electronic devices can be fabricated by stacking 2D materials. In

such a construction, GO can provide the connection to high-κ dielectrics, enabling gate stacks with high capacitance.

GO is a graphene-derived material and has attracted considerable attention owing to its unique and tunable electronic, magnetic, and optoelectronic properties[5, 15, 16]. In particular, much effort has been devoted to creating semiconducting GO to overcome the absence of a bandgap in pristine graphene, which greatly limits its application in electronics. In general, the introduction of foreign covalent species, such as oxygen, into the graphene lattice partially disrupts the in-plane symmetry of the carbon π-network and induces an optoelectronic bandgap in the electronic structure. GO exhibits a rich surface chemistry, which can be understood as that of a graphene sheet functionalized with chemically reactive oxygen groups such as carboxyl, hydroxyl, and epoxy groups[17, 18]. The type and the amount of these species strongly depends on the oxidation mechanism[18, 19]. GO was initially produced by wet chemistry approaches[20, 21] based on Hummers' method[22, 23]. The drawback of such techniques is that they are incompatible with large wafer processing technology and that the GO contains a significant amount of impurities, including trapped H_2O, which may be detrimental for e.g. applications using H_2O-sensitive materials as often encountered in flexible organic electronic applications. Furthermore, wet oxidation methods typically result in amorphous complex chemical structures with a variety of different oxygen groups[18] and large sample-to-sample variations. By contrast, well-controlled dry oxidation techniques can limit the oxygen groups to epoxy groups spread over the basal plane of graphene and hydroxyl groups decorating the edges of GO[18] after exposure to air.

We have already demonstrated the fabrication of GO by "dry" oxygen plasma treatments. Using this technique, the optical and electronic evolution of graphene upon oxidation was studied[5, 24] and the application of GO for making electronic devices such as Schottky diodes was demonstrated[25]. In the present work, we demonstrate a novel application of GO as an atomically thin seed layer for ALD of high dielectric constant (high-κ) oxides. The heterogeneous integration of the GO seed layer on other substrates allows for the subsequent deposition of ultrathin uniform metal oxides such as Al_2O_3 by providing suitable chemical surface groups for the nucleation of the oxide layer. Considering the transferability of graphene[26, 27], this heterogeneous integration method is applicable to almost any arbitrary surface, with particular interest for chemically inert surfaces where the lack of suitable reactive chemical groups renders the nucleation of ALD problematic. In this paper, we demonstrate that GO can be integrated as a seed layer on graphene.

In general, the ALD of dielectrics on graphene is hampered by the lack of suitable functional groups on defect-free graphene surfaces that are reactive towards typical ALD precursors such as trimethyl aluminum (TMA) and tetrakis(ethylmethylamino)hafnium (TEMAH) for Al_2O_3 and HfO_2 respectively[9] (see the Supplementary Information page for further details). Improved nucleation of ALD Al_2O_3 and HfO_2 has been observed after surface functionalization by exposure to NO_2[28, 29] or ozone[30, 31]. In addition, organic seeding layers, such as self-assembled monolayers[32] or polymer layers have been demonstrated[33]. Dielectrics have also been fabricated by deposition and subsequent oxidation of metal films[34]. Although these methods possess clear advantages over ALD directly on pristine graphene, important issues remain unresolved. Graphene surface pretreatments that involve NO_2 or ozone tend to lead to surface damage of the graphene and degradation of its electronic properties. Furthermore, organic, in particular polymer, seeding layers, and oxidized metal seeding layers decrease the total capacitance of the gate dielectric layer because of an increased gate thickness and a reduced effective dielectric constant. In all these cases, it has still been challenging to scale the thickness of the gate oxide down into the range of a few nm, as required for field effect devices rivaling the current Si-based technology, without degrading the channel mobility. In this letter, we show that all these challenges and limitations can be overcome using GO as a seed layer.

Results and discussion

GO samples were prepared by exposing graphene grown by chemical vapor deposition (CVD) on copper to different numbers of O_2 plasma pulses (see Methods). The nature of the functional surface groups on GO after O_2 plasma exposure was studied by synchrotron-radiation photoemission spectroscopy (SRPES) using soft x-ray photons. Figure 1a shows a comparison of the C 1s spectra of pristine (as grown on Cu) graphene with both partially oxidized (1 O_2 plasma pulse), and fully oxidized (6 O_2 plasma pulses) GO. The C 1s spectrum of the pristine sample showed a main peak at 284.8 eV originating from sp^2 hybridized C[19, 20]. As graphene is conducting, the peak was strongly asymmetric due to shake-up processes into the conduction band. The narrow peak width of 400 meV indicates that the polycrystalline graphene was well ordered. The weak peak at 285.5 eV in the tail of the main peak indicated the presence of oxygen on the pristine sample. This peak has been attributed to C-O single bonds, e.g., as in C–O–C (epoxide) or C-OH groups[20, 35]. The small spectral weight of

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this component indicates that the pristine graphene was rather pure. Epoxide groups, where a single oxygen atom lies midway above the C–C bond, have been calculated to be the most energetically favorable chemisorption configuration[36] of O on graphene, although the chemical shift between C-O-C and C-OH is too small to be resolved and thus the peak assignment is not unambiguous. Additional very weak components at 287.3 eV and 289.5 eV were observed in the C 1s spectrum which can be attributed to carbonyl and carboxyl/CO_2 functional groups, respectively[20, 35]. Both components can be expected to be present at structural defects and edges of the polycrystalline graphene sheet. After exposure to the O_2 plasma the peak assigned to C-O-C single bonds became more prominent, while the carbon sp^2 peak significantly decreased in spectral weight and broadened slightly. In addition, the C-O-C peak shifted gradually by about 200 meV (to 285.3 eV after 6 O_2 pulses) towards the sp^2 peak, which may be linked to the increasing predominance of epoxide over hydroxyl groups after the dry plasma oxidation. This transformation from sp^2 hybridized C to epoxide was essentially complete after 6 plasma cycles. In addition, the weak carbonyl and carboxyl peaks present on graphene disappeared and a novel peak appeared at 288.8 eV. This peak can be attributed to a O-C=O functional group[20, 35]and may stem from carbonyl groups situated, e.g., at defects or grain boundaries of the polycrystalline GO. The decreasing O-C=O/C-O-C intensity ratio with the number of O_2 plasma pulses indicates that the formation of O-C=O at defects was initially more efficient than the surface oxidation (epoxide formation) but quickly saturated. The above picture is consistent with the O 1s SRPES spectra of fully oxidized GO (figure 1b), which showed two peaks, which can be attributed to C-O single bonds (532.2 eV) as well as (O-)C=O double bonds (533.6 eV)[35], respectively. An additional peak at 530.9 eV stemmed from a very thin surface Cu oxide (or hydroxide).

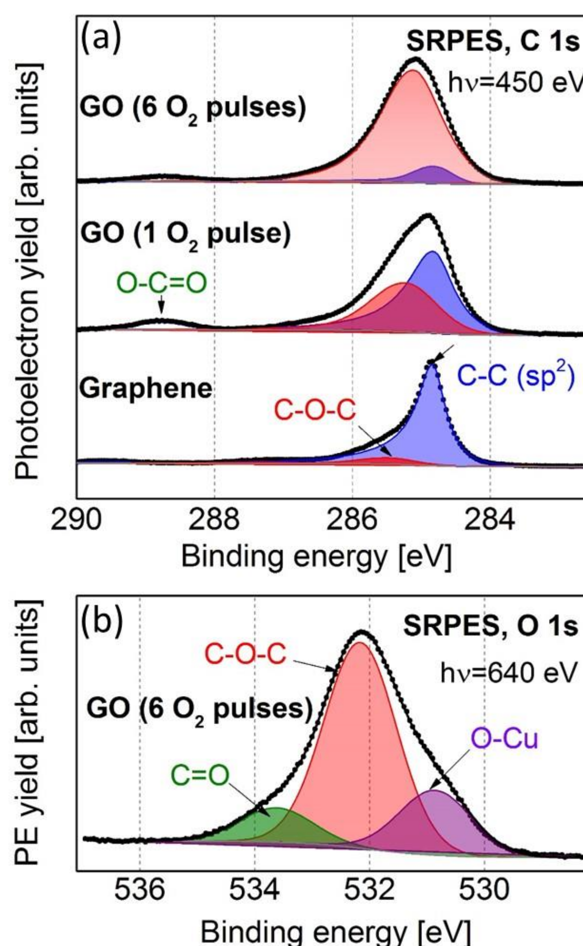

Figure 1. (a) C 1s SRPES spectra of pristine (as grown on Cu) graphene as well as of both partially oxidized (1 O_2 plasma pulse) and fully oxidized (6 O_2 plasma pulses) GO. (b) O 1s SRPES spectrum of fully oxidized GO (6 O_2 plasma pulses).

Next, we analyzed the surface morphology and cross-sectional micrographs of Al_2O_3 deposited by ALD on GO. For this purpose, graphene was first transferred on Si wafers and then partially oxidized (1 plasma pulse), and the Al_2O_3 layer was then deposited on GO using TMA and H_2O at 150 °C. The nucleation behavior of the ALD of Al_2O_3 from TMA and H_2O is schematically

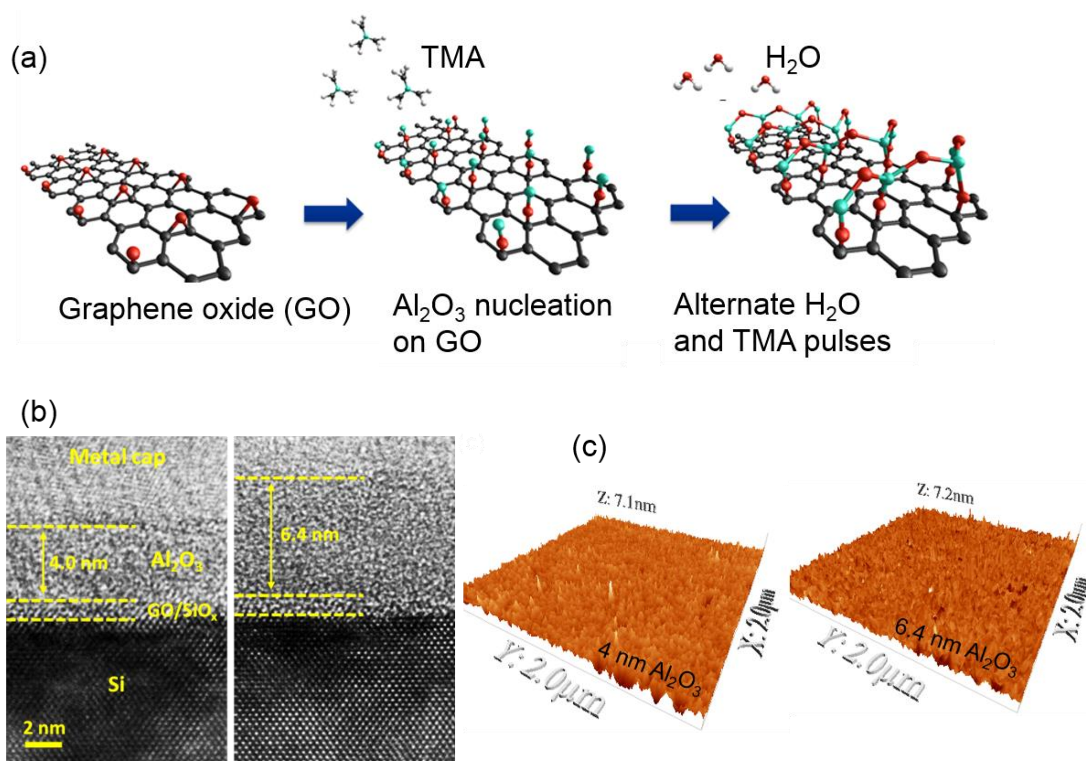

Figure 2. (a) Schematic diagram of ALD nucleation on GO. The (b) TEM and (c) AFM micrographs of ~4 and ~6.4-nm-thick Al_2O_3 deposited on lightly oxidized GO (1 plasma pulse) indicate that the deposited layers were continuous and smooth

depicted in Figure 2a. Figure 2b shows transmission electron micrographs for ~4 and ~6.4-nm-thick Al_2O_3 deposited on the partially oxidized GO. The Al_2O_3 layers were regular, smooth, and continuous which demonstrates that the low oxidation condition already provided a sufficient density of ALD nucleation sites on GO for 2D nucleation. Although the GO layer could not be clearly distinguished in the micrograph, a buffer layer of ~1 nm composed of Si native oxide and graphene could be identified. Figures 2d and 2e show the AFM images of the 4 and 6.4 nm Al_2O_3 films on GO, respectively. The low rms roughness of 4.1 Å and 3.7 Å for the 4 nm and 6.4 nm Al_2O_3 films, respectively, clearly confirm the good nucleation of Al_2O_3 on GO. Note that these values were very similar to the roughness of the initial oxidized Si surface, which is typically ~3–4 Å. Hence, GO is an excellent seeding layer for the ALD of Al_2O_3 from TMA and H_2O, leading to regular nucleation and the formation of closed and smooth thin films.

To analyze the electrical evolution of graphene during the oxidation process, we fabricated graphene devices on SiO_2/Si substrates. The channel of a graphene device was formed by single-layer graphene (SLG) flakes deposited by micromechanical exfoliation. Large-area CVD SLG was then transferred onto the SiO_2-supported graphene flake, forming a double-layer graphene stack (see Figure 3a). Standard lithography was used to pattern narrow ribbons, and multi-terminal devices were fabricated using Au lift-off metallization. Depending on the location (on or off the exfoliated SLG flake), the devices either consisted of double-layer graphene (sample A) or SLG (sample B), as shown in the schematic diagram of the device structures in Figure 3a.

Figure 3b describes the evolution of the sheet resistance of samples A and B with the number of O_2 plasma pulses during a subsequent oxidation. The resistance of sample B monotonically increased with an increasing number of O_2 plasma pulses to a value of ~10^8 Ω/□, which is in agreement with the sp^2 to sp^3 change in hybridization of the carbon atoms, while the sheet resistance of sample A was relatively unaffected by oxidation. Quantitatively, the sheet resistance of sample A increased only by about twofold, which indicates that the underlying (metallic) SLG remained intact while the top layer (CVD SLG) underwent oxidation.

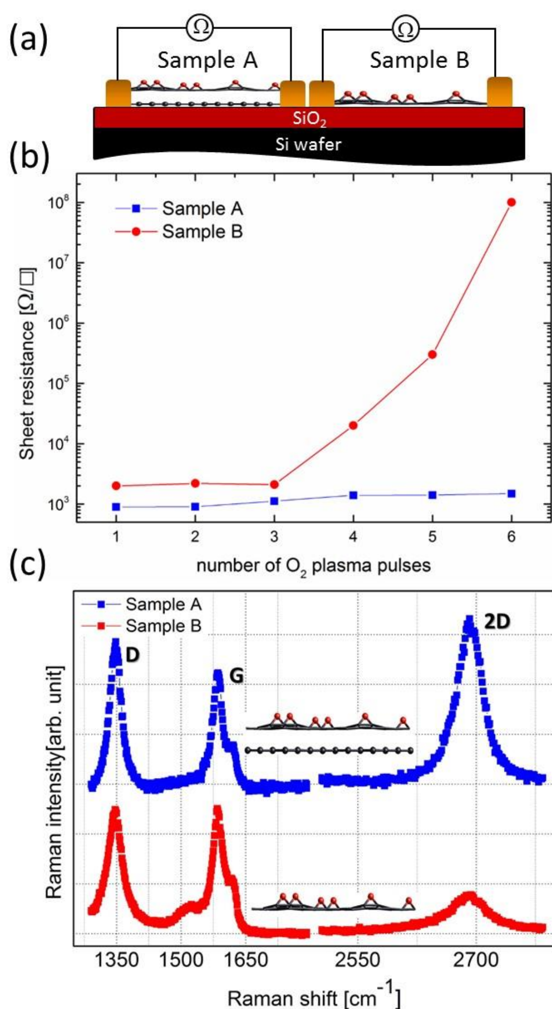

Figure 3. (a) Schematic diagram of samples A and B. (b) Relationship between sheet resistance and number of O_2 plasma pulses for a graphene monolayer deposited on a Si substrate capped with SiO_2. (c) Raman spectra of SLG and double-layer stack of graphene under the highly oxidized condition (6 plasma pulses).

Raman spectroscopy further confirmed that the underlying graphene layer was not affected by the O_2 plasma exposure. Figure 3c compares the Raman spectra of samples A and B under the highly oxidized condition (6 plasma pulses). Both sample show the presence of D peak, which is among the most discussed Raman features in functionalized graphene. We attribute this peak to the presence of oxygen atoms covalently bonded to the top layer of sample A and sample B. Another central feature in Raman spectra of SLG is the 2D peak around 2700 cm^{-1}, which is attributed to a two-phonon intervalley Raman scattering process[37]. Due to oxidation, the 2D peak of sample B broadened (FWHM of 110 cm^{-1}) and its intensity significantly decreased (I_{2D}/I_G= 0.30), but the shape, position (~2675 cm^{-1}), FWHM (~36 cm^{-1}), and intensity (I_{2D}/I_G= 1.45) of the 2D peak of sample A indicates that the underlying graphene layer remained intact as the top layer underwent oxidation.

In a next step, as an application of the GO seeding layer, we investigated top-gated graphene field effect transistors (FETs) and graphene-insulator-metal (GIM) capacitors. In general, the ALD of thin dielectric films on graphene is not easy because there is no surface functional group or defect on the inert graphene surface, which are needed for chemical surface reactions the conventional ALD processes are based on. In this work, devices were fabricated by Van der Waals assembly of two layers of CVD-grown graphene to form a double-layer stack on a SiO_2/Si substrate followed by patterning in 50 × 50 μm^2 and 25 × 25 μm^2 pads for capacitors and 1 × 3 μm^2 ribbons for FETs. Then, the upper layer was fully oxidized (6 O_2 plasma pulses), isolating the bottom graphene layer as the bottom electrode of the GIM capacitor. Subsequently, a 10-nm Al_2O_3 layer was deposited by ALD on the GO. Finally, the top electrode was patterned by electron-beam lithography and a metal lift-off process. Figure 4a shows an optical image of a pair of graphene FETs as well as a pair of GIM capacitors.

We first evaluated the transfer characteristics of the graphene FETs. Figure 4b compares the source-drain current versus top-gate bias (I_{ds} vs V_{tg}) of a representative FET at different back-gate biases (V_{bg}). At first glance, the transfer properties of this GO mediated top-gated graphene-FET, i.e., ambipolarity, with almost symmetric electron and hole transconductances (and therefore mobilities) and non-zero conductivity, indicate a healthy graphene FET. This shows that the fabrication of the top gate stack including on-site O_2 plasma oxidation of the upper graphene layer and the subsequent ALD of Al_2O_3 did not degrade the electronic quality of the underlying SLG.

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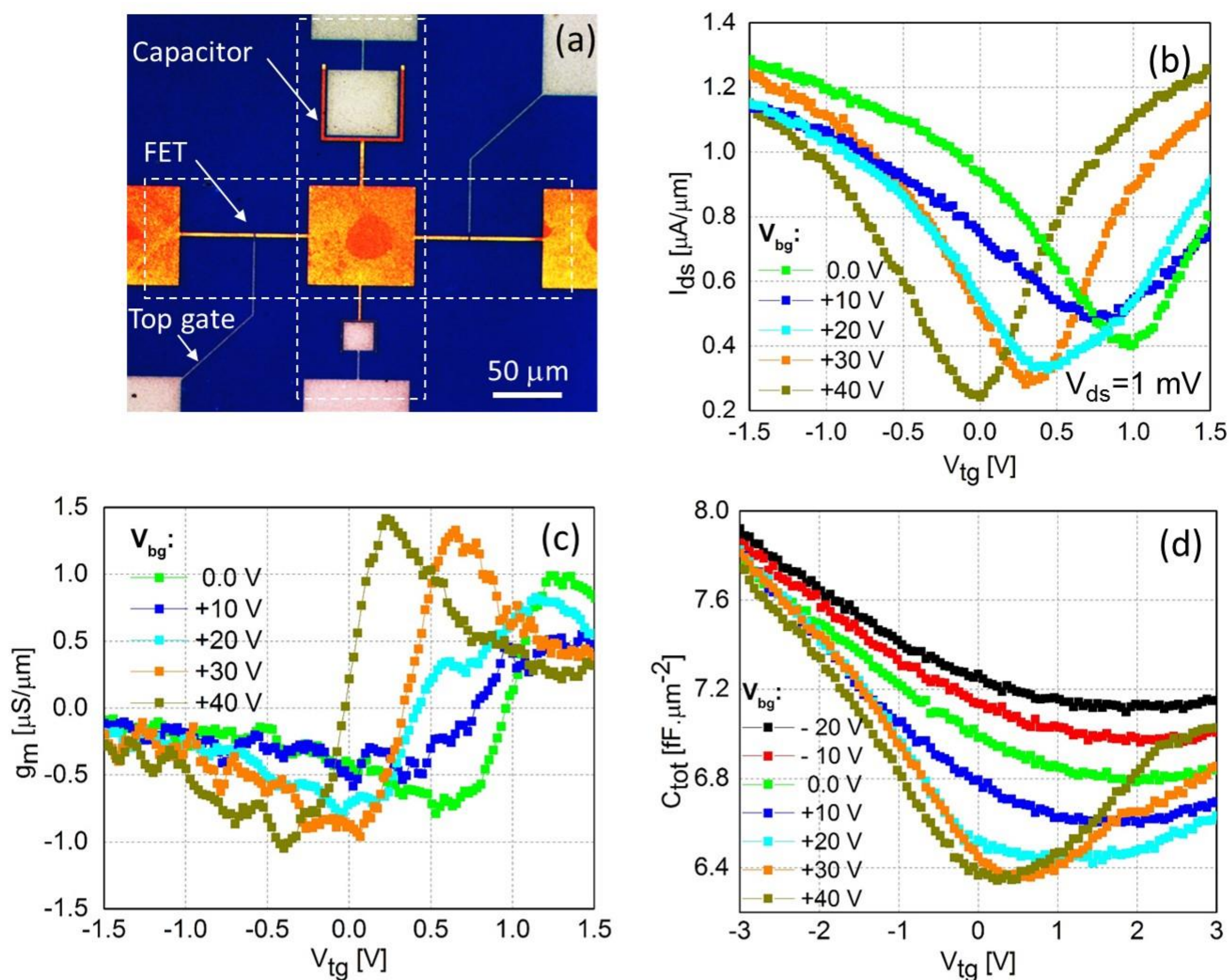

Figure 4. (a) Optical image of a pair of top-gated FETs with source-drain length/width of 1.2 μm/3 μm and top gate length of 1 μm and a pair of GIM capacitors with active areas of 50 × 50 μm^2 and 25 × 25 μm^2. The graphene layers (bottom electrodes of the capacitors) were in contact with the measurement pads by a U-shaped metal frame. (b), (c) and (d) are the transfer characteristics (I_{ds} vs V_{tg}) transconductance (g_m vs V_{tg}) and capacitance–voltage (C_{tot} vs V_{tg}) of the devices shown in (a), respectively.

In our device, V_{np} at V_{bg}=0 (no excess charge from the back gate) was V_{tg}= ~1 V, which indicates that graphene was p-doped. The extra holes in graphene were mainly introduced by chemical doping of graphene because of the interaction with the more electronegative underlying SiO_2.[38] However, applying increasing positive V_{bg} decreased V_{tg} to ~0.0 V, which corresponds to the neutrality condition (E_F=E_D). The excess field effect electron concentration, which needs to be provided by the back gate to compensate the chemically induced holes, and therefore reach the neutrality condition (n=0), can be expressed as $n = -\eta V_{bg}$, where η = ~2.4 × 10^{11} cm^{-2} V^{-1} takes into account the details of our planar capacitor (90 nm SiO_2). Applying progressively positive V_{bg} shifted the V_{np} value toward zero, where, at V_{bg} = +40 V, V_{np} = ~0 V, which indicates that the hole concentration was about n = 9.6 × 10^{12} cm^{-2}. Applying negative V_{bg} up to –20 V further increased the hole concentration in graphene up to n = ~1.4 × 10^{13} cm^{-2}. The Fermi level shift relative to E_D was calculated by $\Delta E_F = sgn(n)\sqrt{n\pi}\hbar\upsilon_F$,[39] where ν_F is the Fermi velocity (~10^6 m/s) and ħ is the reduced Planck constant. In this case, we obtained the maximum ΔE_F of 440 meV at V_{bg} = –20 V. In the literature, a value of ~4.42 eV[40] for the work function of pristine SLG (where n=0 and E_F=E_D) has been reported. Therefore, the field-effect doping procedure allows further tuning of the work function value within the range 4.4–4.9 eV. At V_{bg} = 0 V, the top-gated graphene FET possessed a maximum transconductance (g_m) of $|g_{m,max}|$= 1.0 and 0.7 μS/μm for electrons and holes, respectively. In the event of restoring channel neutrality (V_{bg} = 40 V), the electron and hole $|g_{m,max}|$ increased to 1.4 and 1.0 μS/μm, respectively, which can be attributed to the improvement of

the field effect mobility in the small doping regime. These parameters indicate that the device performance is comparable to that of back-gated graphene-FETs with pristine SLG deposited on SiO_2 and measured in ambient conditions, confirming that the on-site preparation of GO on SLG has negligible effect on its electronic and structural properties. This demonstrates that GO monolayer can be used as an ALD seed layer to grow Al_2O_3 on SLG for the fabrication of top-gated FETs while completely protecting the underlying channel material.

The C_{tot} (V) curves of a typical GO-mediated GIM capacitor at varying back-gate bias (V_{bg}= −20 V to 40 V) are plotted in Figure 4d. A pronounced dependence of C_{tot} on V_{tg} also changed positions and values of $C_{tot,min}$ with V_{bg} were observed. In the following, we explain the reasons for these behaviors. In general, contrary to a typical metal–insulator–metal (MIM) capacitor, which exhibits a constant capacitance, a GIM capacitor, despite the absence of a band-gap in graphene, shows an explicitly V_{tg}-dependent capacitance. This behavior can be understood by considering the quantum capacitance (C_q) of graphene, which is an important property for systems including 2D electron gases (2DEGs) such as graphene. C_q describes the response of the 2DEG to the conduction and valence band movements when the capacitor is biased, and is proportional to the density of states (DOS) of the 2DEG[41, 42]. Since a graphene monolayer does not completely screen a transverse electric field, it behaves as a capacitor rather than a classical metal, which gives rise to a finite C_q. This capacitance is in series with the capacitance of the surrounding dielectric and semiconductor substrate. The $C_{tot,min}$ occurs when C_q obtains its minimum value, corresponding to the minimum of DOS where E_F=E_D. Therefore, the V_{tg} values at $C_{tot,min}$ for different V_{bg} must essentially be the same as V_{np} in the transfer characteristics curves. This can be observed in the experimental results shown in Figure 4b and d, despite small variations that can be attributed to the area of the graphene layer in the capacitor being orders of magnitude larger than the one in the FET and therefore suffering from random charge impurity and the intrinsic uniformity of CVD graphene.

In addition to the shift of V_{np} upon varying V_{bg}, we observed that the C_{min} values also monotonically decreased when increasing V_{bg} from –20 to 40 V. We attribute this behavior to a broadening in the DOS resulting from long-range Coulomb impurities, which also causes the finite graphene conductivity at the Dirac point. The Coulomb potential is truncated by the formation of electron–hole puddles that screen the disorder potential[43]. Disorder-induced puddling in graphene has been demonstrated by several research groups.[44-46] In general, substrate-induced structural distortions and chemical doping from the resist residue are considered the main possible sources of impurities. Rakheja et al.[47] have theoretically shown that C_q at the Dirac point progressively increases by the DOS broadening energy. Therefore, because the graphene C_q is in series with the dielectric capacitance, its increase (decrease) results in an increase (decrease) of the total capacitance. As shown in Figure 4d, neutralizing the already p-doped graphene by injecting field effect electrons from the back gate (positive V_{bg}) considerably lowered C_{min}, indicating smaller Coulomb interaction and therefore smaller puddling in the neutrality condition, which is a reasonable assumption.

In addition to the broadening in the DOS, which is caused by environmental effects such as substrate effects or chemical doping, the DOS, and therefore C_q, can undergo major changes upon modification of the graphene electronic structure by covalent oxidation. The C_q per unit area is given by $C_q = g(E)e^2$, where g(E) is the DOS and e is the unit charge. In the effective mass approximation, the DOS in the 2DEGs is given by $g(E) = g_v m^* / \pi \hbar^2$, where g_v is the valley degeneracy, $\hbar$ is Planck's constant, and m^* is the effective mass.[41] The linearly vanishing DOS of the graphene monolayer gives rise to a small C_q in the vicinity of the Dirac point, which thus influences the behavior of the overall GIM capacitor. To assess the effect of oxidation on C_q, we have performed first-principles calculations based on DFT to obtain the DOS and effective mass of the monolayer GO with various concentrations of epoxy groups ($C_{18}O_x$, x = 0–8) spread over the basal plane. The DOS of pristine graphene (C_{18}) and two representative oxygen densities ($C_{18}O_4$ and $C_{18}O_8$) are shown in Figure 5a. Progressively denser oxygen functionalization strongly affected the electronic structure of graphene. The DOS of pristine graphene (without oxygen adatoms) showed no bandgap. However, increasing the oxygen density resulted in opening of a bandgap, which monotonically increased with oxygen density to 2.5 eV, revealing that graphene undergoes a semimetal-to-insulator transition with oxidation. The calculated opening of the DOS bandgap upon oxidation was in good agreement with the progressively increasing sheet resistance of the GO device shown in Figure 3b. Figure 5b shows the electron and hole effective masses as a function of oxygen density. Both electron and hole masses were significantly increased by oxidation.

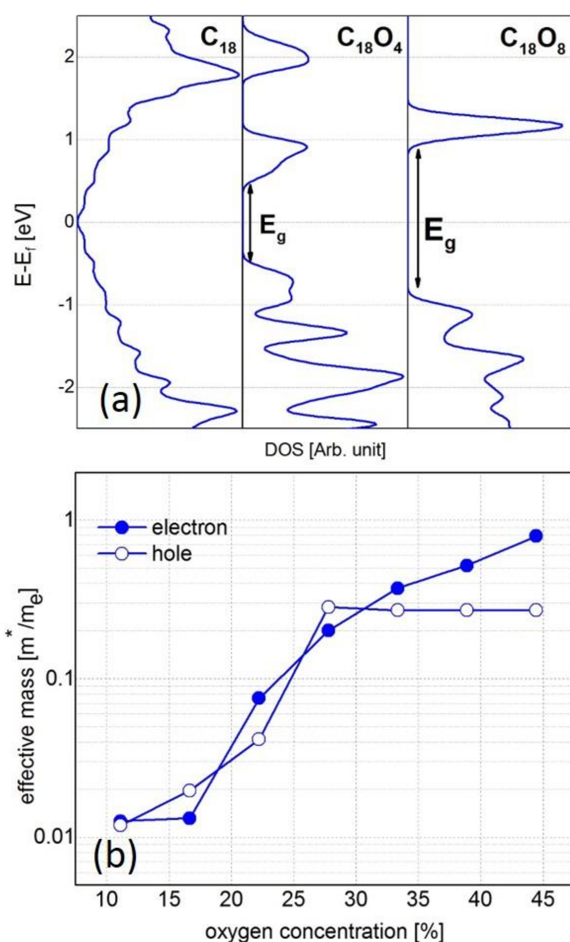

Figure 5. (a) Total DOS of pristine graphene (C18) and graphene oxide with two different oxygen densities ($C_{18}O_4$ and $C_{18}O_8$) monolayer and (b) effective electron/hole mass for different oxygen densities.

However, the hole mass saturated at 0.3 m_e for oxygen concentrations above 25%, while the electron mass monotonically increased with increasing oxygen concentration to ~1.0 m_e at an oxygen coverage of 0.45. The increase of the effective mass is expected to lead to an increase of C_q, which is in series with the oxide capacitance, and therefore an increase of the total capacitance. To examine this hypothesis, we studied $Al/Al_2O_3/GO/SiO_2$ capacitors on p^+ Si(100) with different degrees of oxidation of GO. GO was prepared by oxidizing transferred graphene on SiO_2/p^+ Si. Different degrees of oxidation were obtained by choosing three levels of oxidation: low (1 plasma pulse), medium (3 plasma pulses), and high (6 plasma pulses), which will be referred to in the following as conditions A, B, and C, respectively. Subsequently, Al_2O_3 layers with thicknesses between 4 and 15 nm were deposited by ALD on the GO. Finally, the samples were capped with an Al layer, which was then patterned by lithography into capacitors electrodes. Figure 6 shows the capacitance equivalent thickness (CET) as a function of the physical thickness of Al_2O_3 for oxidation conditions A, B, and C, respectively, as well as for a set of reference samples without GO. The reference samples showed, as is expected, a linear dependence of the CET on the physical Al_2O_3 thickness. The slope of the curve corresponded to a dielectric value of $\kappa = 8.3$ for Al_2O_3, in keeping with previous results[48]. A CET offset of 1.1 nm was observed, which is in good agreement with the thickness of the SiO_2 layer between Al_2O_3 and the Si substrate.

The behavior was found to change when GO was inserted into the capacitors. For the most oxidizing conditions C, the CET was identical to that of the reference samples within the accuracy of the measurement. This confirms that the highly oxidized GO had essentially no effect on the CET scaling. In contrast, for the less oxidizing conditions A and B, the CET values for a given thickness of Al_2O_3 were higher than for the reference samples and increased with decreasing oxidation of graphene, confirming the presence of serial C_q, which is strongly dependent on the oxidation level and essentially independent of the Al_2O_3 thickness.

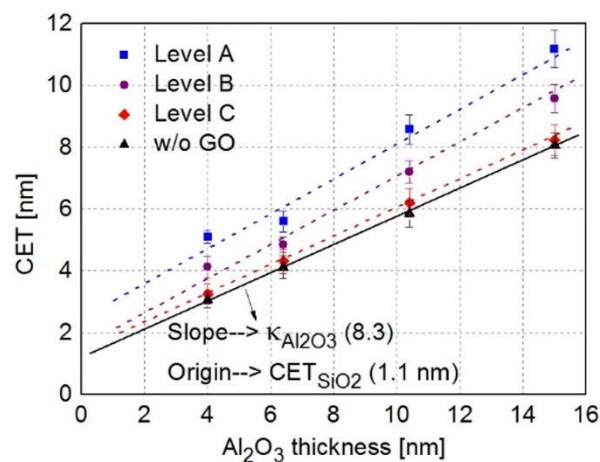

Figure 6. CET as a function of the physical Al_2O_3 thickness deposited on GO/Si with different levels of oxidation of graphene and pristine Si wafer as a reference.

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Conclusions

To conclude, we have demonstrated the suitability of GO as a seeding layer for the ALD of gate dielectrics. GO was obtained by dry O_2 plasma oxidation of single layer graphene. SRPES indicated that the oxidation mainly introduced C–O–C epoxy groups on the surface, which are reactive towards typical ALD precursors, such as TMA. As an example, a stack of two SLGs were transferred onto the channel material and GO was then formed by selective oxidation of the top SLG. The *on-site* prepared GO was then used as an ALD seed layer to grow Al_2O_3 on SLG with negligible effect on its electronic and structural properties as confirmed by Raman spectroscopy and field-effect measurements. Because of the high gas impermeability of graphene, the underlying channel material was fully protected during the oxidation. This method opens a very versatile route for the fabrication of top-gated MOS structures on channel materials where direct ALD is difficult or impossible. Also, because of the inertness of graphene, the binding with the channel material is believed to be due to weak der Waals-type bonds, which minimized the effect of the seed layer on the electronic properties of the channel material. We further demonstrate that GO is highly effective as a seeding layer. The ALD of Al_2O_3 on GO led to regular and smooth films without any growth inhibition and thus enabled the scaling of the gate oxide thickness down to a few nm, as required for advanced FET devices. It was further observed that sufficiently oxidized GO did not contribute measurably to the gate capacitance. The proposed ALD seeding technique can be considered a robust method for integration of high-quality ultra-thin high-k dielectrics, in particular into van der Waals-bonded semiconductors to enable a gate stack with high capacitance.

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Notes and references

[a] imec, Kapeldreef 75, B-3001 Leuven, Belgium
[b] Department of Electrical Engineering and Computer Sciences, Massachusetts Institute of Technology, 77 Mass Avenue, Cambridge, Massachusetts 02139, United States
[c] Material and Device Research Center, Samsung Advanced Institute of Technology, Giheung-gu, Yongin-si Gyeonggi-do, 446-712, South Korea
[d] Brandenburgische Technische Universität, Angewandte Physik—Sensorik, Konrad-Wachsmann-Allee 17, 03046 Cottbus, Germany

† Electronic supplementary information (ESI) available

‡ with Brandenburgische Technische Universität at the time of this work, currently with ALBA-CELLS, Carretera BP1413 Km. 3,3, 08290 Cerdanyola Del Vallès (Barcelona), Spain.

[*] Corresponding author: anour@mit.edu

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