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Fast Transfer-free Synthesis of High-quality Monolayer Graphene on Insulating Substrates by Simple Rapid Thermal Treatment

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The transfer-free synthesis of high-quality, large-area graphene on a given dielectric substrate, which is highly desirable for device applications, remains a significant challenge. In this paper, we report on a simple rapid thermal treatment (RTT) method for the fast and direct growth of high-quality, large-scale monolayer graphene on a SiO₂/Si substrate from solid carbon sources. The stack structure of solid carbon layer/copper film/SiO₂ is adopted in the RTT process. The inserted copper film does not only act as an active catalyst for the carbon precursor but also serves as a “filter” that prevents premature carbon dissolution, and thus, contributes to graphene growth on SiO₂/Si. The produced graphene exhibits high carrier mobility of up to 3000 cm² V⁻¹ s⁻¹ at room temperature and standard half-integer quantum oscillations. Our work provides a promising simple transfer-free approach using solid carbon sources to obtain high-quality graphene for practical applications.

Introduction

Graphene, a quasi-2D material, has attracted considerable attention because of its excellent transport properties, which make it a promising material for applications ranging from radio-frequency devices and transistors to optoelectronic devices.¹⁻⁴ The tremendous interest in graphene has led to various kinds of preparation methods,⁵⁻¹² such as exfoliation from bulk graphite, chemical vapour deposition (CVD) on transition metals, and reduction of graphite oxide. Among these, CVD on transition metals appears to be the most promising for producing high-quality, large-scale graphene; in this method, carbon sources, such as methane and acetylene, are commonly used as precursors with metal catalytic substrates.^{8-10, 13} Although the CVD growth method possesses advantages such as low cost and large scale, using metal catalytic substrates requires a process for transferring graphene onto a desired substrate for further applications. Such transfer process is not only inconvenient but also causes additional contamination, wrinkling, and breakage of the graphene, which result in problems in the devices. To overcome these issues, the transfer-free synthesis of graphene on a desired

substrate has been attempted using two main strategies.¹⁴⁻¹⁶ The first approach involves directly growing graphene by metal-catalyst-free CVD on dielectric substrates such as SiO₂,¹⁴ Al₂O₃,¹⁵ BN,^{17, 18} and SrTiO₃.¹⁹ However, producing high-quality, large-scale graphene using this method is difficult. The second approach involves directly synthesizing graphene by thermally converting a solid carbon film coated on insulating substrates through a metal catalyst capping layer.¹⁶ Recently, Zhuo *et al.* reported that the carrier mobility of graphene produced by this method could reach up to 1835 cm² V⁻¹ s⁻¹.²⁰ Apart from these two main strategies, the transfer-free synthesis of graphene is also performed through metal-vapour-assisted CVD, in which a metal catalyst in vapour form reacts with carbon precursor gases in the gas phase as well as on the substrate surface. This process enables metal residue-free growth of high-quality, large-scale graphene comparable with graphene grown on metal foil in terms of structural defect level. However, the as-grown graphene exhibits a maximum carrier mobility of only ~800 cm² V⁻¹ s⁻¹ at room temperature. Therefore, the development of large-scale graphene with high quality through a simple process remains a considerable challenge.

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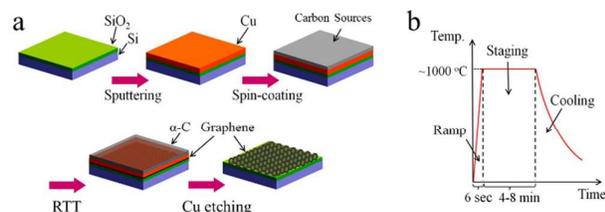


Fig. 1 Schematic illustration for the transfer-free growth of graphene on insulating substrates. (a) Copper films are sputtered on a SiO₂/Si substrate with the thickness of 500 nm. After annealing the copper films at 950 °C, solid carbon source such as PMMA or sucrose is spin coated on top of the film. The RTT process is carried out with the heating rate of 160 °C /s. After keeping at the staging temperature (800–1000 °C) for 4–8 minutes, the sample is cooled down to room temperature in about 30 minutes. Afterwards, on top of the copper film the amorphous carbon forms. While at the Cu–SiO₂ interfaces, there is large area monolayer graphene. The Cu layer together with α-C is finally dissolved away in a 0.1M FeCl₃ solution. Monolayer graphene formed directly on the SiO₂/Si wafer is obtained without any further process. (b) the heating, staging and cooling processes.

For CVD-grown graphene, nickel and copper are the commonly used metal catalysts. However, the growth kinetics and mechanism between nickel and copper are different because of the varying solubility of carbon in these metals.^{8, 12} In the case of nickel, where carbon solubility is high, graphene growth is governed by segregation and precipitation processes, which generally produce multilayer graphene. To suppress multilayer formation, Weatherup et al. introduced a carbon diffusion barrier (Al₂O₃) inserted into an amorphous-C/Ni bilayer stack, which effectively prevented premature carbon dissolution and significantly improved monolayer graphene formation.²¹ In the current work, the extremely low carbon solubility in copper is considered by inserting a copper film between a solid carbon layer and SiO₂. We then demonstrate a simple rapid thermal treatment (RTT) method for the fast and direct growth of large-scale graphene on a SiO₂/Si substrate from solid carbon sources. During the RTT process, the copper film inserted between the solid carbon layer and the SiO₂/Si substrate does not only act as an active catalyst for the carbon precursor but also as a “filter” that prevents premature carbon dissolution, and thus, contributes to the formation of graphene on SiO₂. The produced monolayer graphene exhibits high carrier mobility and standard half-integer quantum oscillations. It should be noted that our RTT method is completely different from the previous reported rapid growth methods where plasma treatment should be used for generate precursors.²² Our RTT method that carried out at atmosphere pressure is a simple process that cannot only produce high-quality monolayer graphene with a scale as large as ~1 mm² but can also be applied to most catalyst materials. Amorphous carbon (α-C) from carbonized poly(methyl methacrylate) (PMMA) or sucrose (C₁₂H₂₂O₁₁), which is used as a solid carbon source in this case, also significantly simplifies the synthesis process of graphene.

Experimental

Materials

We used copper films with a thickness of ~500 nm sputtered on a SiO₂/Si substrate. The copper films were sputtered under a base pressure of ~2 × 10⁻⁶ Torr. The copper coating rate was below 0.1 Å/s to ensure the high quality of copper films. The copper films were annealed at 1000 °C in Ar/H₂ (1:1) gas atmosphere under ambient-

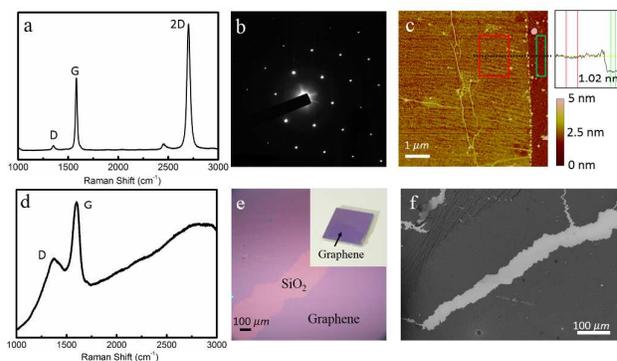


Fig. 2 Characterization of as-grown graphene samples. (a) Raman spectrum of a Randomly selected area of as-grown graphene shows the D, G and 2D peaks. (b) The TEM diffraction pattern of as-grown graphene sample, displaying the typical hexagonal crystalline structure of graphene. (c) AFM characterization of as-grown graphene sample. (d) Raman spectrum of as-grown amorphous carbon on top of the copper film. (e) Optical and (f) SEM images of the as-grown graphene on a SiO₂ substrate.

pressure for 6 hours. The cooling rate was 0.01 °C/s. PMMA (MICROCHEM 950 A2) and sucrose (C₁₂H₂₂O₁₁) were used as the solid carbon sources. The PMMA films spin-coated onto the copper film was about 100 nm thick. While the thickness of C₁₂H₂₂O₁₁ dilute layer on copper film was around 500 nm.

RTT process

The RTT was carried out on a Rapid Thermal Processor (RTP-1300). The SiO₂/Si substrates containing annealed copper films and solid carbon sources on top were placed in the center of the processing chamber on a 4-inch Si substrate. The 12 pcs of halogen lamps make it possible to do heat treatment on the sample uniformly as well as rapidly. The sample was heated to the growth temperature with a heating rate of 160 °C/s protected by Argon gas in the atmosphere. After staying at the growth temperature for 4–8 minutes, the system was cooled down to room temperature in about 30 minutes.

Electronic Measurement

The electronic properties of the as-grown graphene were evaluated based on the bottom-gate field-effect-transistor configuration.^{23, 24} The metal electrodes were prepared by standard electron-beam lithography in Raith e_LiNE system and then electron-beam thermal evaporation (Ti/Au 5/45 nm). Transport measurements were carried out using standard lock-in technique (SR830) with a current source provided by Keithley (model 6221). The measured data are shown in Fig. 7 and the extracted carrier mobility of electrons and holes for this device is ~2,600 cm²V⁻¹s⁻¹ and ~3,000 cm²V⁻¹s⁻¹, respectively.

DFT calculation

CASTEP code is used with an ultra-soft pseudo-potential and PBE-style generalized gradient approximation.²⁵ Transition state search is also performed with CASTEP.²⁶ The cut off energy is set to 400 eV. A 108 super-cell cell is used for bulk Cu and a 216-atom super-cell is used for edge dislocation model. A vacuum layer is inserted for edge dislocation to relax the strain. A residual force of 0.02 eV/Å is used as convergence criteria for geometry optimization. The similar parameter has been used in our previous study on metal catalyst.

Results and discussion

Fig. 1(a) illustrates the substrate preparation for growing graphene on a SiO₂/Si wafer though the RTT process. First, a 500 nm-thick

copper film was deposited on a silicon wafer covered with 300 nm SiO₂ using a DC sputtering system. Then, an annealing process was performed at 1000 °C. Before depositing the solid carbon source onto the copper film, the substrate covered with copper film was immersed in dilute hydrochloric acid to remove copper oxide. Two carbon sources, PMMA and sucrose, were spin-coated on the surface of the copper films. The PMMA- and sucrose-coated samples then underwent RTT, as depicted in Fig. 1(b). During this treatment, a sample was rapidly heated to approximately 1000 °C at a heating rate of approximately 160 °C/s. After heating the sample at the maximum temperature for 4–8 minutes, it was then cooled down to room temperature for approximately 30 minutes. During the entire annealing process, the heating chamber was filled with ultrapure argon gas to prevent oxidation. Graphene directly formed at the copper–SiO₂ interface, whereas α -C remained on the surface of the copper film. Due to the lattice matching between graphene and copper, the etching process is very critical. Here, we first heated the sample to 180 °C to oxidize the copper film partially. Then this film, along with α -C, was finally dissolved in a mixed FeCl₃/HCl solution (0.1M/0.01M). Finally, the graphene that formed directly on the SiO₂/Si wafer was obtained without any further process.

Fig. 2(a) shows the typical Raman spectrum of the PMMA-derived as-grown graphene using the RTT method at 1000 °C. The Raman spectrum clearly presents a sharp 2D peak at ~2680 cm⁻¹, along with a very weak D peak at ~1350 cm⁻¹ and a G peak at ~1580 cm⁻¹. The 2D band can be fitted well to a single Lorentzian shape with a full width at half maximum (FWHM) of approximately 40 cm⁻¹. Furthermore, the I_{2D}/I_G intensity ratio is ~1.8. These data indicate that graphene is grown in a monolayer. In addition, the I_D/I_G intensity ratio is only as low as ~0.05, which shows the low population of sp³-type defects in graphene. According to the I_D/I_G intensity ratio, the grain size of our graphene is 210 nm as estimated by the empirical relation²⁷

$$L_a(\text{nm}) = 2.4 \times 10^{-10} \lambda^4 (I_D/I_G)^{-1},$$

where λ is 514.5 nm. The as-grown graphene film was further examined by transmission electron microscopy (TEM). Then, it was detached from the SiO₂/Si substrates using a buffered oxide etch and was suspended on a copper grid for TEM measurements. The clear hexagonal electron diffraction pattern with an inner intensity stronger than the outer intensity, as shown in Fig. 2(b), further confirms that the as-grown graphene film has a single layer. The aforementioned results demonstrate that the RTT process produces high-quality monolayer graphene on a SiO₂/Si substrate with low degrees of structural defects. Fig. 2(d) presents the Raman spectrum measured from the upper surface of a copper film. A high Raman background signal that results from copper surface-plasmon emission forms a broad band with two intense peaks: a 1D peak and a G peak. The as-grown graphene films are different from the graphene films grown on copper foil by regular CVD. The excess carbon source supply by PMMA and the short annealing period may be responsible for the deteriorated quality of the graphene films on the upper surface of the copper foil. Therefore, the formation of graphene on a SiO₂/Si substrate indicates that the copper film is not only an active catalyst for carbon precursor but also acts as a “filter” to prevent premature carbon dissolution, which contributes to the formation of graphene on SiO₂. Interestingly, the RTT process can generate high-quality monolayer graphene as large as ~1 mm². A uniform color contrast between the graphene region and bare SiO₂/Si in the bright-field optical microscope image shown in Fig. 2(e) reveals a large-size graphene on a SiO₂/Si substrate. The AFM image of a randomly selected area is shown in Fig. 2(c), demonstrating the thickness of the graphene at a smooth area to be around 1 nm. Importantly, we notice the existence of obvious wrinkles of graphene in AFM and SEM (Fig. 2(f)) images, possibly introduced during the etching process of the top copper layers. We

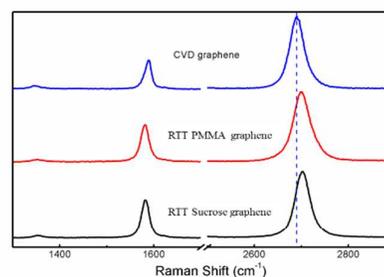


Fig. 3 Raman spectrum of as-grown graphene film grown on top of the copper film through regular CVD method using methane and hydrogen as carbon source (in blue), and Raman spectra of PMMA/sucrose-derived graphene films grown on SiO₂/Si through RTT method at 1000 °C, respectively (in red/black).

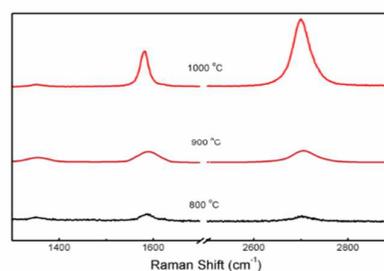


Fig. 4 Raman spectra of PMMA-derived graphene films grown at different temperatures through RTT method.

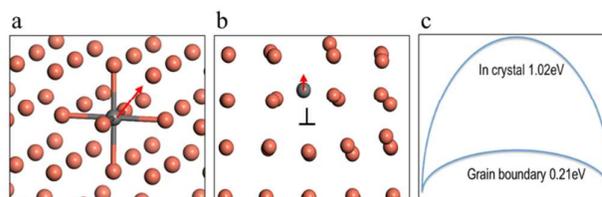


Fig. 5 (a) The relaxed octahedral interstitial site in Cu crystal. The atom diffusion direction is (111), indicated by the red arrow. (b) The relaxed interstitial site on an edge dislocation. The diffusion direction is the direction of edge dislocation. (c) The diffusion barrier along Cu(111) direction in (a) and the edge dislocation direction in (b). The initial and final states are two neighboring interstitial site.

believe that a slow etching rate is needed. We also notice that people used Cl₂ gas as the copper reactant,²⁸ which might be a possible method for the improvement of our copper etching process in the future.

One of the advantages of the RTT process is that graphene grown on SiO₂/Si can be realized by using different solid carbon sources. The same growth condition using C₁₂H₂₂O₁₁ as a carbon source was adopted for the graphene growth on SiO₂/Si. Fig. 3 shows the Raman spectrum of the graphene grown on SiO₂/Si using C₁₂H₂₂O₁₁ as the carbon source. The Raman spectrum exhibits I_{2D}/I_{1D} ≈ 1.9 with a 2D band that is fitted well to a single Lorentzian shape with an FWHM of ~40 cm⁻¹ and featuring a typical characteristic of monolayer graphene. The negligible 1D peak further indicates low degrees of structural defects in graphene. Apparently, C₁₂H₂₂O₁₁ can also generate high-quality graphene similar to that obtained using PMMA as the carbon source. As shown in Fig. 3, the 1D and 2D bands of

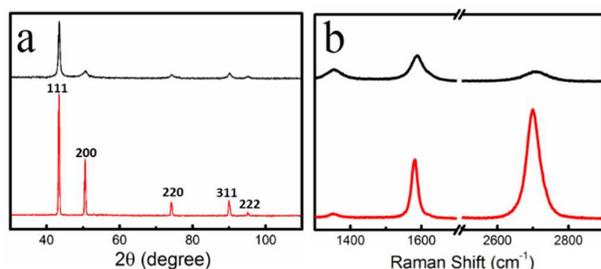


Fig. 6 (a) X-ray diffraction spectra of the sputtered copper films before (in black) and after (in red) annealing. (b) Raman spectra of as-grown graphene films using the non-annealed/annealed (black/red) copper film.

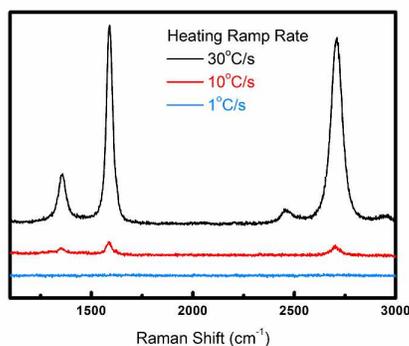


Fig. 7 Raman spectra of PMMA-derived graphene films with different heating ramp rates.

the PMMA-/sucrose-derived graphene grown using the RTT process peaked at $\sim 1350\text{ cm}^{-1}$ and $\sim 2680\text{ cm}^{-1}$, respectively. Compared with the graphene grown by regular CVD on copper foil, the PMMA-/sucrose-derived graphene grown using the RTT process exhibits obvious blue shifts in both 1D and 2D bands. These shifts are generally attributed to compressive strain resulting from the different thermal expansion coefficients between graphene and a substrate.

In the RTT growth method, growth temperature plays a crucial role in forming monolayer graphene on SiO_2/Si . The Raman spectra in Fig. 4 exhibit the relationship between growth temperature and the structural characteristics of the graphene films. The weak 1D, G, and 2D peaks start appearing at a low temperature of $800\text{ }^\circ\text{C}$. Then, these peaks synchronously become intense after the growth temperature increases to $900\text{ }^\circ\text{C}$. The random nucleation and poor surface migration of carbon are presumed to be the major causes of the enhanced 1D peak associated with the defects at these growth temperatures. The defective graphene structure is significantly ameliorated by increasing growth temperature by up to $1000\text{ }^\circ\text{C}$, during which the 1D peak becomes indistinguishable. However, given the growth-temperature dependence of the graphene structure, the carbon atoms that dissociated from PMMA are able to diffuse from the upper surface of the copper film and onto the SiO_2/Si surface even at a low temperature of $800\text{ }^\circ\text{C}$. This finding indicates that the grain boundary of the copper film serves as a passage for carbon atoms accessing the SiO_2/Si surface during the growth process. To gain a detailed understanding of this behavior, density functional theory is applied to simulate the diffusion pathway of carbon in copper thin film. Cu(111) crystal grains are dominant in the copper thin film, as shown in Fig. 6(a); thus, the diffusion barriers against carbon in the copper crystal and the grain boundary have been calculated in terms of Cu(111), and the results are shown

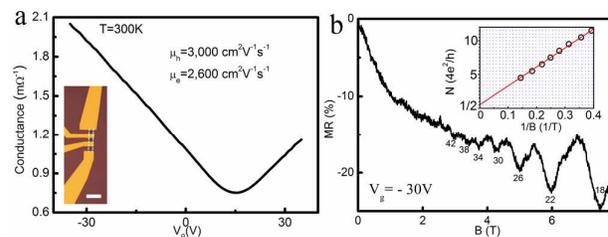


Fig. 8 (a) Transport measurements of PMMA-derived MLG by RTT method at $T=300\text{ K}$. The inset is an optical image of the FET device with the scale bar of $20\text{ }\mu\text{m}$. (b) Quantum oscillations in the corresponding MLG. SdHO at constant gate voltage $V_g=-30\text{ V}$ as a function of magnetic field B is shown. The inset shows the SdHO peaks that are uniformly spaced as a function of $1/B$.

in Fig. 5. In this case, the interstitial site with the lowest energy in the copper crystal is identified as an octahedral site, as shown in Fig. 5(a). Our calculation indicates that the diffusion barrier from one octahedral site to a neighboring site is 1.1 eV . The grain boundary is simulated by an edge dislocation, as shown in Fig. 5(b). Different twinning grain boundaries can be regarded as a series of edge dislocations. The lowest-energy site is located immediately below the extra copper column. The energy barrier for carbon to diffuse along the edge defect line is calculated to be only 0.2 eV , which is significantly lower than the carbon diffusion barrier in the copper crystal. Therefore, we consider the grain boundary as the main diffusion path during graphene growth.

To understand the growth mechanism of graphene further, the effect of the copper film on the graphene structure before and after the annealing process was investigated. Fig. 6(a) shows the X-ray diffraction (XRD) spectra of the copper film before (in black) and after (in red) the annealing process. The XRD spectra reveal various crystal orientations of Cu(111), Cu(200), Cu(220), Cu(311), and Cu(222). The diffraction peaks become notably sharp after the annealing process, particularly the (111) diffraction peak, which indicates a remarkable enhancement in crystal fraction in the copper film after the annealing process. Based on the diffraction peaks, the grain sizes of different crystal orientations can also be calculated using the Debye–Scherrer formula²⁹

$$D = \frac{0.9\lambda}{\beta \cos\theta},$$

where D is the grain diameter size, λ is the X-ray wavelength (0.15406 nm), β is the FWHM, and θ is the diffraction angle. Copper grain size before annealing is only as large as 15 nm , using the (111) diffraction as reference. After the annealing process, grain size remarkably increases to 42 nm . The increased grain size and crystal fraction obviously contribute to the growth of high-quality graphene, as indicated in Fig. 6(b). In general, the graphene film grown using the copper-catalyzed CVD process is achieved by the surface absorption and decomposition of hydrocarbon precursors through the active copper surface, in which low carbon solubility in copper results in the self-limited growth of monolayer graphene.³⁰ The difference between our proposed process and the copper-catalyzed CVD process is that the precursors in our work should be initially diffused from the upper surface of the copper film onto the SiO_2/Si surface through the grain boundary, as previously discussed. Given that carbon solubility in copper crystal is low, the grain boundary is regarded to provide passage, through which small doses of the precursors can access the SiO_2/Si surface. After reaching the SiO_2/Si surface, the precursors will undergo a process similar to that in copper-catalyzed CVD to induce graphene growth. During this stage, grain boundaries significantly influence graphene nucleation and growth.^{30–32} Previous experiments revealed that grain boundaries

could induce nucleation sites and form continuous non-uniform polycrystalline graphene film with numerous domain boundaries.³⁰⁻³² Apparently, increasing copper grain size can reduce the grain boundaries and densities of nucleation sites. Consequently, such reductions decrease the fraction of domain boundaries, which improves graphene structure. Thus, increasing grain size and crystal fraction can logically contribute to producing high-quality graphene, as shown in Fig. 6(b). Therefore, controlling copper grain boundary is important in the RTT process for growing high-quality graphene.

Usually, a low heating rate produced flat and smooth surfaces with larger copper grains during CVD growth of graphene on the copper foil. This also resulted in a lower density of nucleation sites. Here, we investigated the influence of the heating ramp rate on the quality of as-grown graphene using the RTT method. Raman spectra of PMMA-derived graphene films with different heating ramp rates are shown in Fig. 7. A sharp D peak appeared at the heating ramp rate of 30 °C/s. No graphene signal was observed when the heating ramp rate was below 10 °C/s. As discussed above, large copper grain sizes resulting from the pre-annealing process do help the formation of high quality graphene. The heating ramp rate in the RTT process is believed to have little influence on the crystal quality of the copper films because the copper films are pre-annealed. However, it is known that rapid heating induces a thermal gradient across the copper film which can never be neglected and thus eventually affects the carbonization process of solid carbon precursors and their diffusion rate across the copper films. A high heating ramp rate facilitates the diffusion of carbon atoms while a low heating ramp rate results in a small thermal gradient, hindering the accumulation of carbon atoms at the copper-SiO₂ interfaces.

Transport measurements based on a bottom-gate field-effect transistor configuration were also conducted to characterize the grown graphene. The typical transport properties are shown in Fig. 8(a). By applying the widely used fitting device model that combines minimum carrier density at the Dirac point and quantum capacitances, carrier mobility can be extracted from the transport data. The extracted carrier mobilities of electrons and holes for the device are ~2,600 cm²V⁻¹s⁻¹ and ~3,000 cm²V⁻¹s⁻¹, respectively, with a residual carrier density at the Dirac point of ~1×10¹² cm⁻² at room temperature. We measured eight more samples, of which the mobilities range from 2,000 cm²V⁻¹s⁻¹ to 3,300 cm²V⁻¹s⁻¹. Compared with the mobilities of our CVD graphene samples (1,000 cm²V⁻¹s⁻¹ to 4,000 cm²V⁻¹s⁻¹), the mobilities of RTT graphene samples are in the same order. The high quality of the grown monolayer graphene was also confirmed by the Shubnikov–de Haas oscillation (SdHO) measurement.³³ Fig. 8(b) shows the experimental data of SdHO at a gate voltage of -30 V with a vertically applied magnetic field that varies from 0 T to 8 T. The Landau level filling factors are indicated at each valley. These SdHO peaks are uniformly spaced as a function of 1/B as shown in the inset in Fig. 8(b). The intercept extrapolated by the linearly fitting curve reveals the origin of the filling factor, N = 1/2, which indicates a Berry's phase of π, that is, the characteristic of the standard half-integer quantum oscillations of monolayer graphene.³³

Conclusions

In summary, we present a simple and effective transfer-free RTT process for the fast growth of high-quality, large-scale graphene on SiO₂ substrates using solid carbon sources. In the RTT process, the quality of the thin copper layer inserted between a solid carbon layer and a SiO₂/Si substrate is a critical factor in controlling graphene quality. Our graphene-based devices exhibit satisfactory electrical properties, including a promising carrier mobility of 3,000 cm²V⁻¹s⁻¹ and standard half-integer quantum oscillations. This work provides a

controllable, effective, and economical transfer-free route to obtain high-quality, large-scale graphene for practical applications.

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Author contributions

N.W., Z.W., and R.H. conceived the projects. Z.W. and Y.Q.G. conducted the experiments including copper film preparation, rapid thermal treatment, sample characterization and data analyses. Y.Z.G. conducted the DFT calculations. N.W. and R.H. are the principle investigator and coordinator of this project. Z.W., R.H., and N.W. provided the physical interpretation and wrote the manuscript. Other authors provided technical assistance in sample preparation, data collection/analyses and experimental set-up.

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