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Low-Temperature Fabrication of High Performance Indium Oxide Thin Film Transistors

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ABSTRACT

In this study, indium oxide (In_2O_3) thin-film transistors (TFTs) were fabricated by solution-process at low temperature. A single precursor in a single solvent system was used as the In_2O_3 precursor to minimize the carbon-based impurities. The 300 °C-annealed In_2O_3 TFT with channel thickness of 12 nm exhibits enhanced performance, which shows saturation mobility (μ_{sat}) of $3.08 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, an on/off current ratio ($I_{\text{on}}/I_{\text{off}}$) of 1.04×10^8 , a threshold voltage (V_{T}) of 12.7 V, and a subthreshold swing (SS) of 1.49 V/dec. Finally, high-performance In_2O_3 TFT based on solution-processed zirconium oxide dielectric was realized, which shows the distinguished electrical performance ($\mu_{\text{sat}} = 13.01 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, $I_{\text{on}}/I_{\text{off}} = 1.09 \times 10^7$, $V_{\text{T}} = 1.2 \text{ V}$, and $\text{SS} = 0.1 \text{ V/dec}$). These results suggest that solution-processed In_2O_3 TFTs could potentially be used for low-cost, low-temperature, and high-performance electronic devices.

1. Introduction

Metal oxide thin-film transistors (TFTs), widely used in integrated circuits, have several advantages such as high electron mobility, high optical transparency, and

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simple synthesis process. The development of large-area, low-cost electronics depends strongly on the high-throughput fabrication process and the choice of materials with appropriate performances. Metal oxide thin films have been grown by vacuum-based deposition methods.^{1,2} However, vacuum-based processes significantly increase manufacturing cost and pose major obstacles for realizing large-area and inexpensive electronic devices. In contrast, solution-phase processes, such as ink-jet,³ screen printing,⁴ dip-coating,⁵ spray pyrolysis,⁶ and spin coating⁷, offer the attraction of low-cost, high-throughput and low-temperature processability. Therefore, metal oxide thin films formed via solution-process is a key processing methods for next-generation TFTs.⁸⁻¹¹

Recently, enormous efforts have been devoted to develop the solution-processed TFT devices. The properties of the TFT devices based on the solution process are even comparable to vacuum-deposited products.^{8,9} However, the metal oxide thin film fabricated by the traditional sol-gel system generally requires high annealing temperature because an incomplete decomposition below 400 °C causes very poor electrical performance.^{9,12} In general, most of the metal oxide TFTs fabricated by the solution process need high-temperature annealing to obtain good semiconductor properties because of the high pyrolysis and dehydroxylation temperatures for typical multi-element precursors.^{13,14} Moreover, the chemical residuals from the additives have negative effects on the device performance and on the stability.¹⁵ To resolve these problems, a single precursor in a single solvent system was used for a self-combustion process to minimize the carbon-based impurities.¹⁶

In_2O_3 is one of the representative metal oxide semiconductors with a wide band gap (3.6-3.75 eV). Its high transmittance in the visible region and high electron mobility make In_2O_3 a potential candidate for the transparent electronic devices.¹² In_2O_3 exhibits various electrical properties, such as metallic, semiconducting, and insulating characteristics, depending on its stoichiometry and the defects in the material.⁷ Indium oxide is an insulator in the stoichiometry form, In_2O_3 . However, it is an n-type semiconductor in the oxygen-deficient form, $\text{In}_2\text{O}_{3-x}$. With increasing

oxygen deficiency, it exhibits metallic characteristics.⁷ The electrical performance of indium oxide can also be modified by controlling the number of metal oxide frame, lattice defects and grain boundaries, etc. Hosono et al. have ever indicated that the thermal annealing reduces the density of the shallow localized states beneath the conduction band minimum, which can improve the electron transport properties.³⁴ In other studies, the electrical properties is observed to be varied with synthesis condition evolved, and is doubtless related to the stoichiometry and defects in the material.^{35, 36}

The precursors used in the solution-processed metal oxide TFTs contained organic and/or inorganic ligands. The successfully fabrication of the TFTs requires significant amount of thermal energy. The device performance could be significant adjusted by the annealing condition.³⁸ Barquinha et al. proposed that the channel thickness also plays an important role in determining the electrical performance of the TFTs.³⁹ In his report, transparent transistors with active layer thicknesses ranging from 15 nm to 60 nm were fabricated at room temperature using RF magnetron sputtering. However, the thickness dependence of solution-processed TFTs is seldom investigated.^{40, 41} Due to the high attraction of the application in the modern electronic devices, it is important to analyze the key factors that influence the performance of the solution-processed metal oxide TFTs such as annealing temperature and the channel thickness.

Apart from the channel layer, the gate dielectric plays an important role in fabricating the high-performance TFTs. Conventional dielectrics, such as SiO₂ or silicon nitride, are currently being replaced by high-*k* materials, such as zirconium oxide (ZrO_x),^{17, 18} aluminum oxide,^{19, 20} and hafnium oxide.²¹ Among these dielectric materials, ZrO_x is regarded as one of the most promising high-*k* materials because of its excellent properties, including high permittivity, large band gap, and the low leakage current density.^{22, 23} In our reports published previously, the physical properties of ultra-thin ZrO_x films (~ 7 nm) and the high-performance TFTs based on ZrO_x were characterized in detail.^{22, 23, 37}

In this report, In_2O_3 TFTs with various channel thicknesses were fabricated by solution process and annealed at various temperatures. The annealing temperature and the channel thickness dependence of In_2O_3 TFTs were investigated. Finally, the In_2O_3 TFT based on a solution-processed ZrO_x dielectric was integrated and investigated.

2. Experiment section

2.1 Precursor solutions

0.05 M indium nitrate hydrate [$\text{In}(\text{NO}_3)_3 \cdot x\text{H}_2\text{O}$] was dissolved in 2-methoxyethanol [$\text{C}_3\text{H}_8\text{O}_2$] to form a solgel solution, the solution was stirred at room temperature for 1 h without adding other chemicals. The ZrO_x precursor solution was prepared by dissolving Zr acetylacetonate [$\text{Zr}(\text{C}_5\text{H}_7\text{O}_2)_4$] in *N,N*-dimethylformamide [$\text{C}_3\text{H}_7\text{NO}$] at a concentration of 0.1 M with the addition of an equimolar concentration of ethanolamine [$\text{C}_2\text{H}_7\text{NO}$], and the solution was stirred at 70 °C for 3 h to enhance the hydrolysis.¹⁷

2.2 Fabrication of transistors

A bottom-gate and top-contact device structure was adopted for the In_2O_3 TFTs, as shown in Fig. 1. Heavily doped silicon substrates with 100 nm thermally-grown SiO_2 layer were used as the gate electrode and dielectric layer. In_2O_3 precursor solution was spin-coated on the SiO_2/Si substrate at a speed of 4500 rpm for 20 s. The samples were dried at 150 °C on a hot plate for 3 min to cure the thin films. This procedure was repeated several times to achieve the desired thickness of In_2O_3 channel layer. The samples were then annealed at various temperatures ranging from 250 to 350 °C for 1 h to investigate the correlation between the annealing temperature and the electrical performance. Moreover, the correlation between the film thickness and the electrical performance were also investigated. Al source and drain electrodes were thermally evaporated on the In_2O_3 thin films through a shadow mask. The channel length and width for all devices in this study were 250 and 1000 μm , respectively.

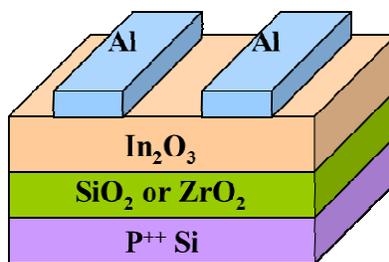


Fig. 1 Schematic illustration of the bottom-gate and top-contact In₂O₃ TFTs.

To integrate the fully-solution processed In₂O₃ TFTs based on high-k dielectric, thermally-grown SiO₂ dielectric was replaced by solution-processed ZrO_x thin film. The ZrO_x precursor solution was spin-coated on the silicon substrate at a speed of 5000 rpm for 20 s. The dielectric was dried at 150 °C on a hot plate for 3 min to cure the thin film. This procedure was repeated three times to achieve the desired thickness of ZrO_x thin film. The sample was processed by UV/ozone treatment for 30 min in atmosphere. In order to reduce the indium diffusion and miscibility phenomenon brought by the annealing treatment of In₂O₃ channel layers, we conducted the annealing process for ZrO_x dielectric at 300 °C for 1 h.

2.3 Characterization

Thermogravimetric analysis (TGA, Pyris1) was used to investigate the thermal behavior of the dried In₂O₃ precursor solution at a heating rate of 10 °C/min from room temperature to 550 °C under ambient condition. The crystal structures of In₂O₃ thin films were investigated by X-ray diffractometer (XRD, X'Pert-PRO MPD and MRD, PANalytical) with a Cu K α 1 radiation. For Fourier transform infrared (FT-IR, Nicolet 5700) measurements, the thin films were prepared on silicon substrates and annealed at various temperatures. X-ray photoelectron spectroscopy (XPS, ESCALAB 250) was used to investigate the chemical binding states of the thin films. The surface morphologies of the thin films were examined by atomic force microscopy (AFM, SPA-400, Seiko). The thicknesses of films were measured by ellipsometry (ESS01, Sofn Instrument). The current voltage (I–V) characteristics of the thin films were carried out using a semiconductor parameter analyzer (Keithley 2634B) under ambient conditions in a dark box.

3. Results and discussion

To analyse the thermal behaviour of In_2O_3 thin films, TGA was performed with a heating rate of $10\text{ }^\circ\text{C}/\text{min}$. As shown in Fig. 2, the conversion of the oxide thin film is completed at around $290\text{ }^\circ\text{C}$. Most of the weight loss below $290\text{ }^\circ\text{C}$ is attributed to the evaporation of the solvent, hydrolysis, and dehydroxylation from the precursor.²⁴ The boiling point of 2-methoxyethanol is $147\text{ }^\circ\text{C}$, which contributes to the dramatic weight loss in the initial stage. Ligand exchange started between the nitrate precursor and 2-methoxyethanol at low temperatures, and metal alkoxide condensation occurred to form a partial network of metal-oxide bonding at elevated temperatures.¹⁶ Moreover, the thin films still need a slow densification process to form oxidation state. The processes can be distinguished according to the temperature at which they occur: volatilization and hydrolysis, dehydroxylation, alloying and densification. On the basis of the thermal behaviours, the annealing condition for In_2O_3 thin films was optimized to be between 250 and $350\text{ }^\circ\text{C}$. To verify the chemical reactions in the thin films annealed at various temperatures, XRD, FT-IR, and XPS measurements were performed.

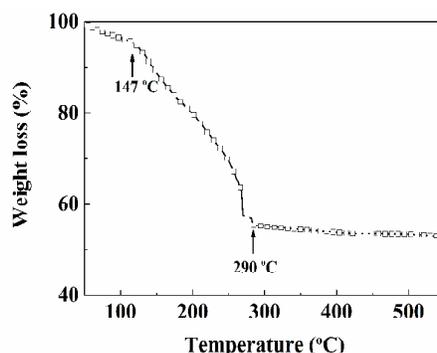


Fig. 2 Thermogravimetric analysis of the dried In_2O_3 precursor solution.

The XRD measurements were taken as a function of annealing temperature to clarify the crystalline state of the thin films and the results are shown in Fig. 3. The In_2O_3 thin films annealed at 250 and $300\text{ }^\circ\text{C}$ show amorphous nature. However, when the annealing temperature was increased to $350\text{ }^\circ\text{C}$, several diffraction peaks are observed. This demonstrates that the In_2O_3 thin film annealed at $350\text{ }^\circ\text{C}$ is crystallized. The In_2O_3 thin film annealed at $350\text{ }^\circ\text{C}$ (JCPDS, No. 65–3170) shows (200), (222),

(400), and (440) orientations located at 21.5, 30.6, 35.5, and 50.94 °, respectively. The sharp peak at around 33 ° is attributed to the silicon substrate. This suggests that the decomposition and the densification of the In_2O_3 thin film occur at higher annealing temperatures, leading to a growth of the grain. It is known that the amorphous thin film has the advantage of large-area uniformity, which is crucial for commercial applications. Moreover, amorphous thin films exhibit other advantages, including smooth surface, high stability, and low interface state density.^{18, 25}

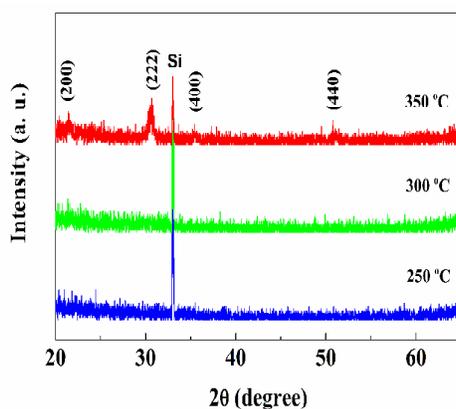


Fig. 3 XRD patterns of the In_2O_3 thin films on silicon substrates annealed at different temperatures.

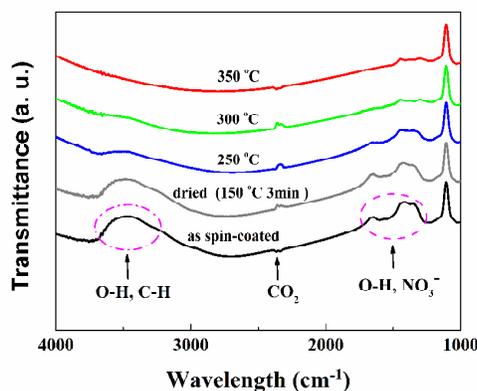


Fig. 4 FT-IR analysis of the In_2O_3 thin films under various annealing conditions.

To better understand the formation of the In_2O_3 thin films, FT-IR measurements were carried out. The O-H and C-H stretching vibration shows a broad peak in the range of 3300-3700 cm^{-1} . Peaks in the 700-1600 cm^{-1} range indicate O-H and NO_3^- deformation vibration. These bondings suppress the condensation of the metal oxide gel films by chelating with coordination bonding to the metal ions.²⁶ The thin films

also show peaks at $\sim 2350\text{ cm}^{-1}$, which may be due to the absorption of CO_2 on the surfaces.²⁷ As shown in Fig. 4, a large number of groups are remained in the cases of the as-spun and dried thin films. With increasing annealing temperature, the groups were gradually separated and decomposed. When the annealing temperature is higher than $350\text{ }^\circ\text{C}$, only trace amount of vibration peaks can be observed.

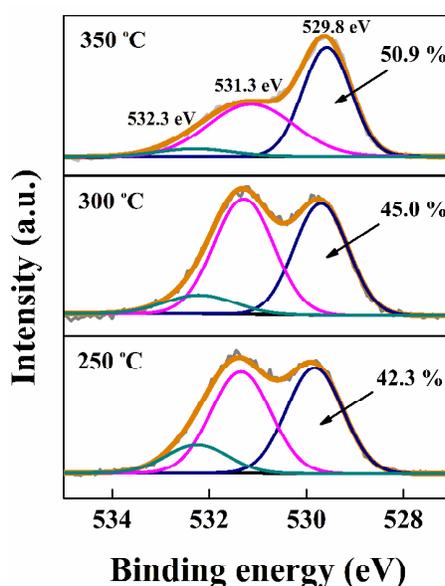


Fig. 5 XPS O 1s analysis of the In_2O_3 thin films annealed at different temperatures.

The chemical states of In_2O_3 thin films annealed at various temperatures were investigated using XPS and shown in Fig. 5. The XPS O 1s peaks are fitted, using a Gaussian method, into three peaks of 529.8, 531.3, and 532.3 eV, respectively.^{16, 28, 29} The dominant peak located at 529.8 eV is due to the lattice oxygen in a fully-coordinated environment (M-O); while the peak located at 531.3 eV is attributed to oxygen in the vicinity of an oxygen vacancy. The peak at 532.3 eV can be attributed to hydroxyl species (M-OH). With the increase of the annealing temperature, the fraction of M-O bonding is increased from 42.3% to 50.9%, whereas the fraction of oxygen vacancies and bounded hydroxyl is decreased. These results agree well with the FT-IR and XRD analysis. This indicates that more M-O bondings are formed at elevated temperatures. The evident M-OH feature at low annealing temperature also confirms the incomplete formation of the oxide lattice. The increase of In_2O_3 lattice will make the electron transition from valence band to conduction band easier

due to the special electron configuration of $4d^{10}5s^0$ as an electron transport channel. The transformation from M-OH to M-O lattice will definitely affect the electrical performance of the In_2O_3 TFTs.³⁰

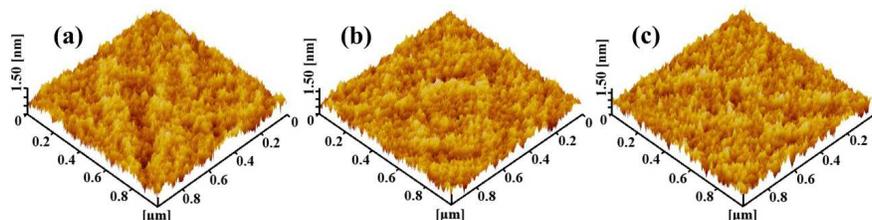


Fig. 6 AFM morphologies of the In_2O_3 thin films on silicon substrates annealed at (a) 250, (b) 300, and (c) 350 °C.

The surface morphologies of the In_2O_3 thin films annealed at various temperatures are shown in Fig. 6. The root-mean-square (RMS) roughnesses are 0.15, 0.16, and 0.19 nm for the thin films annealed at 250, 300, and 350 °C, respectively. This indicates that the solution-processed In_2O_3 thin films are quite smooth and uniform. Meanwhile, the grain size increases slightly with increasing annealing temperature. This can be explained as a result of few residual ligands incorporating into the lattice at higher annealing temperatures. The residual ligands suppress the growth of the grain, which is consistent with the results of XRD analysis.

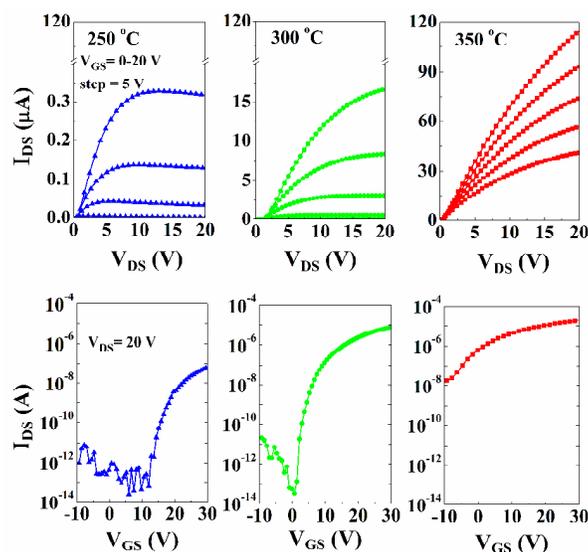


Fig. 7 Output and transfer characteristics of In_2O_3 TFTs annealed at various temperatures.

Table 1 The electrical performances of In_2O_3 TFTs annealed at various annealing temperatures.

Temperature (°C)	μ_{sat} ($\text{cm}^2 \text{v}^{-1} \text{s}^{-1}$)	$I_{\text{on}}/I_{\text{off}}$	V_{TH} (V)	SS (V/dec)	D_{it} ($\times 10^{13} \text{cm}^{-2}$)	I_{on} (A)
250°C	0.36	1.44×10^6	20.3	2.51	1.49	6.44×10^{-8}
300°C	3.08	1.04×10^8	12.7	1.49	0.87	7.31×10^{-6}
350°C	4.67	1.12×10^3	3.2	9.04	5.46	1.93×10^{-5}

To evaluate the possibility of the In_2O_3 thin films as channel layers, the electrical performance of In_2O_3 TFTs based on thermally-grown SiO_2 with thickness of 100 nm were investigated. All the TFT devices were integrated at the same conditions, except for the annealing temperature. The output and transfer characteristics of the In_2O_3 TFTs annealed at various temperatures are shown in Fig. 7. It is found that all the TFTs show n-type behaviors and work in an enhancement mode. The output curves show clear pinch-off and current saturation, the corresponding electrical parameters of the In_2O_3 TFTs annealed at various temperatures are summarized in Table 1.

The saturation mobility (μ_{sat}) and the threshold voltage (V_{TH}) are calculated from the slope of $I_{\text{DS, sat}}^{1/2}$ vs V_{GS} according to the conventional thin film transistor model in the saturation region,³¹

$$\mu_{\text{sat}} = \frac{2L}{WC_i} \left(\frac{\partial \sqrt{I_{\text{DS}}}}{\partial V_{\text{GS}}} \right)^2 \quad (1)$$

where I_{D} is the saturation current, C_i is the areal capacitance of the dielectric, V_{G} is the source-gate voltage, and W and L are the channel width and length, respectively. The μ_{sat} are in the range of 0.36-4.67 $\text{cm}^2 \text{v}^{-1} \text{s}^{-1}$ as the annealing temperature was increased from 250 to 350 °C. From the FT-IR and XPS analysis, the In_2O_3 thin films annealed at low temperatures contain a large amount of organic groups, which can degrade the electrical performance of the TFT devices. With the increase of the annealing temperature further, the amount of organic groups was decreased and more metal-oxygen-metal frame was formed. It is well known that In_2O_3 can exhibit a variety of electrical performance, including conducting, semiconducting, and insulating characteristics depending on the stoichiometry and the defects in the material.⁷ The gradual enhancement of μ_{sat} can be explained by the decomposition of organic groups and the formation of the metal-oxygen-metal frame. Meanwhile, the

V_{TH} values of In_2O_3 TFTs annealed at 250, 300, 350 °C are 20.3, 12.7, 3.2 V, respectively. The negative shift of the V_{TH} is due to the high intrinsic carrier concentrations for the thin films annealed at high temperature and few lattice defects acting as carrier traps. Consequently, a small gate voltage is required to induce carriers to prefill the traps, leading to a decrease of V_{TH} .

Generally, SS is directly related to the traps located in the bulk channel and/or the interface between the channel and dielectric. The subthreshold swings (SS) is given by the following equation,

$$SS = \left(\frac{d \log(I_{DS})}{dV_{GS}} \right)^{-1} \quad (2)$$

Consequently, trap density D_{it} can be estimated from SS using the equation,

$$D_{it} = \left[\frac{SS \log(e)}{kT/q} - 1 \right] \frac{C_i}{q} \quad (3)$$

where k , T , and q are Boltzmann's constant, absolute temperature, and charge quantity, respectively. The D_{it} values are calculated to be 1.49×10^{13} , 0.87×10^{13} , and 5.46×10^{13} cm^{-2} for the TFTs annealed at 250, 300, and 350 °C, respectively. It can be seen that the 300 °C-annealed TFT has the smallest D_{it} value. A large trap density is observed for the TFT annealed at 250 °C due to the incomplete decomposition of residual organic groups. However, a large trap density for 350 °C-annealed TFT is believed to be due to the nanocrystalline structure of the channel layer. As observed in Fig. 3, the 100-nm-thick In_2O_3 thin film was crystallized at 350 °C. The grain boundaries existing in the thin film act as powerful scattering centers. In this report, two kinds of traps, lattice defects and grain boundaries, are involved. The first one is generated due to the non-decomposed impurities in the thin films, which act as the trap centers. The other one is attributed to the existence of the grains, which can block the carrier transport.

The number of carriers and traps has great effects on the performance of the TFT devices. As the annealing temperature was increased from 250 to 300 °C, the on-current (I_{on}) was increased from 6.44×10^{-8} A to 7.31×10^{-6} A, whereas the off-current (I_{off}) was kept unchanged ($\sim 5 \times 10^{-14}$ A). When the annealing temperature

was increased further (up to 350 °C), the I_{on} was increased from 7.31×10^{-6} A to 1.93×10^{-5} A and the I_{off} was increased up to 1.73×10^{-8} A. The abrupt increase of the I_{on} and I_{off} are due to the excess carriers flowing through the limited defects. In other words, the significant evolution of electrical performance is due to the unbalance between stoichiometry and defects. With the trade-off between carriers and traps, the In_2O_3 TFT annealed at 300 °C exhibits excellent device performance, which shows μ_{sat} of $3.08 \text{ cm}^2 \text{ v}^{-1} \text{ s}^{-1}$, $I_{\text{on}}/I_{\text{off}}$ of 1.04×10^8 , V_{TH} of 12.7 V, and SS of 1.49 V. Therefore, we can achieve the desirable performance of the TFT by adjusting the amount of carriers and/or traps at an optimized annealing temperature.

Apart from the effect of the annealing temperature, the channel thickness also plays an important role in the electrical performance of the TFTs. The thickness dependence of the electrical performance of In_2O_3 TFTs was also investigated and the transfer curves are shown in Fig. 8. The I_{on} value was found to increase with increasing channel thickness at a fixed annealing temperature. The thicker the channel layer, the more carriers to be dragged at a same gate voltage. This will certainly result in an increase of the on-current. The electrical performances of the TFTs were thoroughly investigated.

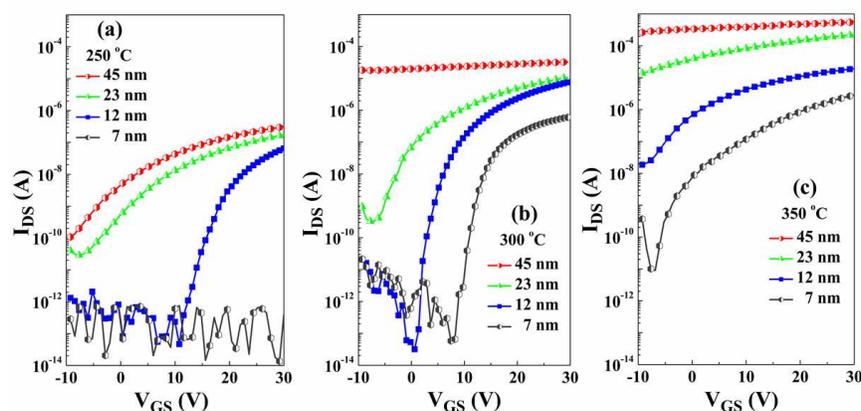


Fig. 8 The transfer characteristics of In_2O_3 TFTs with various channel layer thicknesses and annealed at (a) 250 °C, (b) 300 °C, and (c) 350 °C.

Table 2 The electrical performance of In_2O_3 TFTs annealed at 300 °C as a function of thin film thickness.

Thickness (nm)	μ ($\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$)	$I_{\text{on}}/I_{\text{off}}$	V_{TH} (V)	SS (V/decade)
7	1.24	1.91×10^7	13.6	1.34
12	3.08	1.04×10^8	12.7	1.49
23	4.61	3.32×10^4	6.2	5.12
45		conductive		

For clearance, the electrical performance of In_2O_3 TFT annealed at 300 °C with various channel thickness was calculated and summarized in Table 2. The mobility was found to be 1.24, 3.08, and 4.61 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ for the In_2O_3 TFT with the channel thickness of 7, 12, and 23 nm, respectively. Meanwhile, the In_2O_3 TFT exhibits ‘always-on’ state as the channel thickness is increased to 45 nm. This is mainly attributed to large number of free carriers in the channel. The I_{off} was observed to be constant initially and then increased further with increasing channel thickness. Under the gate bias, the carriers were accumulated near the channel/dielectric interface. The interface defects will trap the carriers and have a further impact on the carrier transport. When the channel thickness is small, the interface defects play the most important role in prohibiting the current flow. A relatively low off current could be achieved. However, with the further increase of the channel thickness, more carriers would make contribution to the current flow, which lead to a higher off current. This is due to the limited number of the interface trap states in the thin films. To better understand the mechanism, the simplified cross-sectional views of devices with thin and thick channel layers are illustrated in Fig. 9.

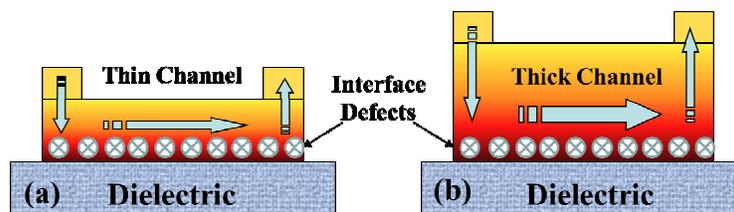


Fig. 9 Schematic cross-section view of In_2O_3 TFTs with (a) thin channel and (b) thick channel.

Meanwhile, we investigated the thickness dependence of the electrical performance of In_2O_3 TFTs annealed at 250 and 350 °C. The corresponding transfer characteristics of the TFTs are shown in Fig. 8, respectively. The same trend as the In_2O_3 TFTs annealed at 300 °C was observed. It is demonstrated that the channel

thickness plays an important role on the electrical performance of the In_2O_3 TFTs.

To investigate the possibility of the improved features of the In_2O_3 TFT based on the high-k dielectric, ZrO_x dielectric thin film was fabricated by solution process and fully solution-processed In_2O_3 TFT based on ZrO_x was integrated. In our previous reports, we made detailed description and characterization for the ultra-thin (~ 7 nm) ZrO_x dielectrics.^{22,23,37} The ZrO_x dielectric thin film exhibits a smooth surface with a roughness of 0.2 nm and pinholes free. The low leakage-current density (1×10^{-9} A/cm² at 2.0 MV/cm) and high breakdown electric field (7.2 MV/cm) were observed, not only due to the smooth surface, dense structure, and high oxidation states of the ZrO_x thin film, but also due to its amorphous nature. The effective dielectric constant, estimated using a series capacitor model ($1/C_{\text{SiO}_2} + 1/C_{\text{ZrO}_x} = 1/C_{\text{total}}$), was calculated to be around 12.5. All of the electrical properties suggest that the solution-processed ultra-thin ZrO_x dielectric have great potential for fabricating the low-voltage, high-performance oxide TFTs. Fig. 10 shows the output and transfer curves of the $\text{In}_2\text{O}_3/\text{ZrO}_x$ TFT. The as-fabricated TFT device exhibits high performance, including a μ_{sat} of $13.01 \text{ cm}^2 \text{ v}^{-1} \text{ s}^{-1}$, a V_{TH} of 1.2 V, an $I_{\text{on}}/I_{\text{off}}$ of 1.09×10^7 , and an SS of 100 mV/dec. The $\text{In}_2\text{O}_3/\text{ZrO}_x$ TFT shows good switching characteristics and reasonable mobility. Generally, the SS values directly correlate with the switching speed and the power consumption of the TFT devices. The small SS values for ZrO_x based TFTs were beneficial from the large areal capacitance of the ZrO_x dielectric and the electronic-clean interface between In_2O_3 and ZrO_x .^{23, 42} More importantly, it can be seen that the operating voltage is only 2 V, which is important for low-power electronic devices. It is noted that the field effect mobility of the In_2O_3 TFT based on ZrO_x dielectric is 3 times larger than that based on SiO_2 dielectric. The origin of the performance enhancement may originate from the enhanced dielectric/channel interface, smooth surface, and/or large areal capacitance of the ZrO_x film.^{17, 32, 33} Presently, fully solution-processed In_2O_3 TFT based on high-k dielectric has seldom been investigated. Based on the results of $\text{In}_2\text{O}_3/\text{ZrO}_x$ TFT, we propose that solution-processed In_2O_3 channel layer with a high-k ZrO_x dielectric is promising for

fabricating low-temperature high-performance TFTs.

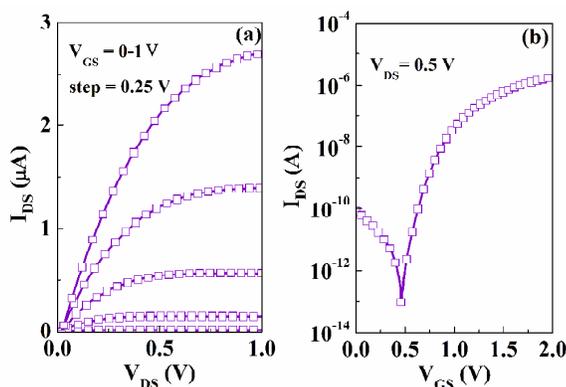


Fig. 10 (a) Output and (b) transfer curves of solution-processed $\text{In}_2\text{O}_3/\text{ZrO}_x$ TFT.

4. Conclusion

In summary, low-temperature high-performance solution-processed In_2O_3 TFTs were successfully fabricated. The annealing temperature dependence and the channel thickness dependence of the electrical performance of In_2O_3 TFTs were investigated. The TFT exhibits enhanced performance for 12-nm-thick In_2O_3 channel layer annealed at 300 °C, including a μ_{sat} of $3.08 \text{ cm}^2 \text{ v}^{-1} \text{ s}^{-1}$, an $I_{\text{on}}/I_{\text{off}}$ of 1.04×10^8 , a V_{TH} of 12.7 V, and an SS of 1.49 V/dec. Finally, a fully solution-processed $\text{In}_2\text{O}_3/\text{ZrO}_x$ TFT was integrated, which exhibits a μ_{sat} of $13.01 \text{ cm}^2 \text{ v}^{-1} \text{ s}^{-1}$, a V_{TH} of 1.2 V, an $I_{\text{on}}/I_{\text{off}}$ of 1.09×10^7 , and an SS of 100 mV/dec. It is demonstrated that solution-processed In_2O_3 TFTs could potentially be used for low-cost, low-temperature, and high-performance electronic devices.

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