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# Direct patterning of sol-gel metal oxide semiconductor and dielectric films via selective surface wetting

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**We report the simple, photolithography-free, direct patterning of both solution-processed metal oxide semiconductors and dielectrics via selective surface wetting. This technique was directly applied to fabrication of low-voltage all-solution metal oxide thin-film transistors with minimal channel and gate leakage currents.**

Recently, metal oxide semiconductors have received considerable attention because of their excellent optical transparency, high carrier mobility, and decent environmental stability.[1,2] Intense research efforts have been concentrated on developing solution-phase deposition techniques that facilitate large-area fabrication of metal oxide-based circuits at reduced cost.[3,4,5,6] Once these economic and scalable processes are generalized for various sol-gel metal oxide conductors, semiconductors, and dielectrics, it is envisioned that high-throughput printing processes can replace a variety of high-cost vacuum deposition methods such as sputtering, e-beam evaporation, chemical vapor deposition, and so on.

Patterning thin films is of central importance for constructing high-performance integrated circuits.[7,8] For example, semiconducting and dielectric layers are patterned in order to eliminate parasitic channel leakage and device-to-device crosstalk, leading to reduction in the off-state current and overall power consumption. Particularly, photolithography has been a standard method used in micro-fabrication of thin film devices.[9] Despite several obvious advantages including high-resolution patterning and compatibility with conventional film deposition methods, photoresist patterning and subsequent sol-gel metal oxide etching typically involve complicated and time-consuming multi-step processes. Moreover, partial delamination and unintentional degradation of as-deposited sol-gel metal oxide films may occur in the course of conventional photolithography processes on top of these sol-gel oxide films.[10] Therefore, a relatively simple and time-saving patterning technique compatible with various sol-gel metal oxide films needs to be developed to realize all-solution low-cost metal oxide electronics with reduced power consumption and minimized device-to-device interference.

There have been intensive research efforts to develop photolithography-free patterning methods, mainly targeting at solution-processed metal oxide films, including inkjet printing, slot-die printing, photo-responsive sol-gel chemistry, or PDMS passivation.[11,12,13,14,15] Although these alternative methods were successfully demonstrated for printing and patterning metal oxide semiconductors, their application to sol-gel metal oxide dielectrics is still in question. The lack of simple generalized patterning protocols available for both sol-gel oxide semiconductor and dielectric materials could be associated with difficulty in fine control of the resultant film thickness and near complete removal of chemical additives necessary for patterning, if any. Note that these issues are more critical for dielectric than semiconducting films because patterned film thickness, density, and material purity need to be under fine control to guarantee high areal capacitance and low leakage current. This also explains why none of the previous works have ever reported direct patterning of both sol-gel metal oxide semiconductors and dielectrics on the same substrate. Therefore, a generalized patterning method needs to meet the following criteria: facile film thiness control, compatibility with known sol-gel dielectric and semiconductor recipes, and possibly large-area processability.

In this report, we demonstrate a simple, photolithography-free, direct patterning method for various sol-gel metal oxide films based on selective surface wetting. The conditions for surface passivation and selective activation were examined by using two types of self-assembled monolayers (SAMs), i.e., alkylsilane and alkylphosphonic acid, and applying plasma treatment through a shadow mask, respectively.[16,17,18,19] Finally, all-solution metal oxide thin film transistors composed of patterned indium-gallium-zinc oxide (IGZO) and patterned aluminum oxide ($AlO_x$) layers were presented as a proof-of-principle for manufacturing large-area high-performance solution-processed metal-oxide electronics with low operation voltage and minimal channel leakage at an affordable cost.

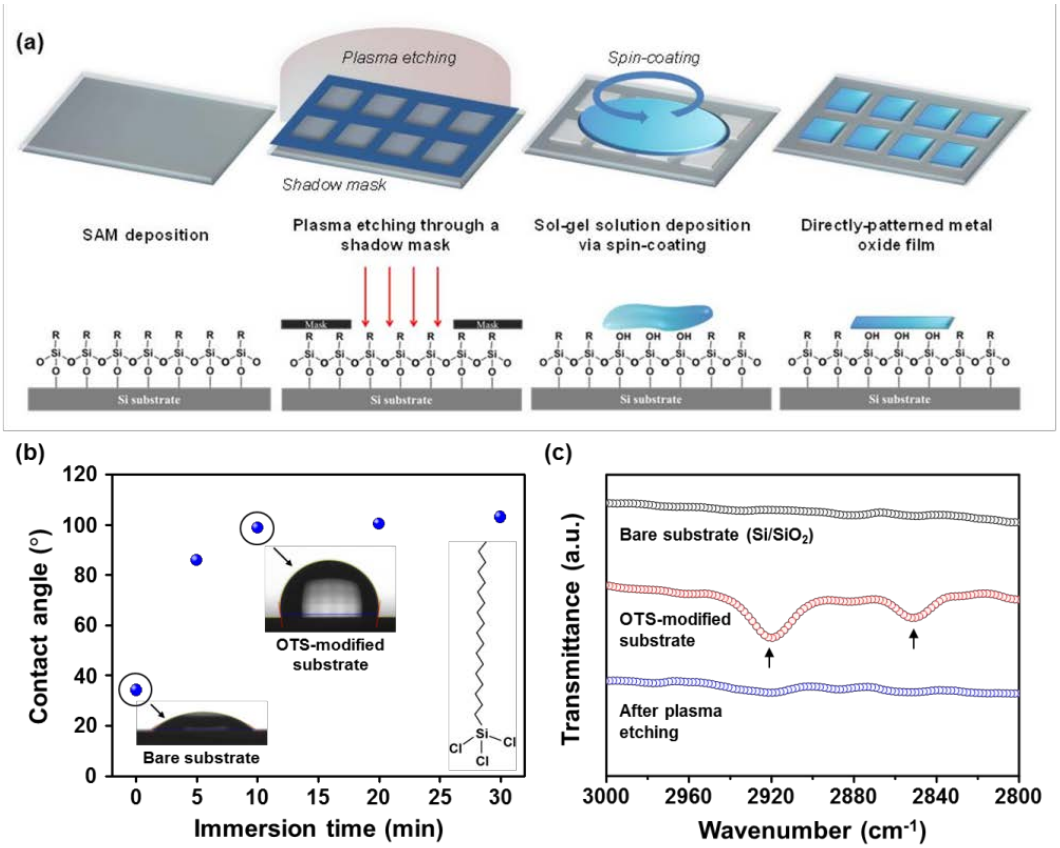


**Fig. 1** (a) Schematic illustrating direct patterning of sol-gel metal oxide films via selective surface wetting. (b) Variation of water contact angle on $SiO_2$ with increased immersion time in an OTS solution (inset: chemical structure of OTS). (c) ATR-FTIR spectra of bare, OTS-modified, and plasma-treated silicon substrates.

Fig. 1(a) illustrates the overall schematic of the sol-gel metal oxide patterning via selective surface wetting. Our technique is based on simple chemical modification for controlling substrate wettability. As most precursor solutions for sol-gel metal oxide films are prepared using hydrophilic solutions based on water or alcohol (e.g., 2-methoxyethanol), selective surface wetting by hydrophilic solutions could be achieved on hydrophilic spatial patterns surrounded by hydrophobically passivated surface. In this study, surface passivation for hydrophobicity and spatial patterning for hydrophilicity were carried out with SAM treatment and plasma exposure through a shadow mask, respectively. Two different molecules, i.e., silane-based OTS and phosphonic acid-based ODPA were employed depending on the chemical nature of the top surface material onto which the SAMs are deposited. It is well known that a silane functional group is reactive toward native silicon dioxide, whereas phosphonic acid is more suitable for metal oxide films such as $AlO_x$.[20,21] After plasma treatment, the openings under a shadow mask become hydrophilic due to the localized stripping of alkyl SAM and wetted by precursor solutions during sol-gel oxide film deposition while intact hydrophobic regions are repulsive to these solutions. The final result is the formation of selectively-patterned wet film which is transformed to densified oxide islands after thermal annealing.

Fig. 1(b) shows the variation of water contact angle on the SAM-passivated surface depending on the immersion time in an OTS solution. After 10 min of SAM treatment, water contact angles essentially reached the maximum value close to 100 degree. The attenuated total reflectance Fourier transform infrared spectroscopy (ATR-FTIR) spectra of OTS-treated $SiO_2$ substrates clearly show the broad absorption bands at 2851 and 2921 $cm^{-1}$, which are ascribed to $CH_2$ asymmetric and symmetric stretching modes, respectively (Fig. 1(c)).[22] The disappearance of these bands after oxygen plasma treatment verifies the effective removal of hydrophobic alkyl functionality out of surface, as also confirmed by the recovery of very low contact angle.

For the general compatibility with various sol-gel precursor recipes for improving semiconductor mobility, lowering annealing temperature, granting photo-reactivity, spin-coating was adopted as an film deposition method. For the best patterning result, a number of experimental parameters such as plasma power, exposure time, and spinning condition were optimized. First, an IGZO precursor solution was spin-coated with different plasma powers and exposure times. Each experimental condition was quantitatively evaluated by measuring the actually deposited IGZO area (see Supplementary Information, Fig. S1) in comparison with the shadow mask opening area. As shown in Fig. 2(a), the patterns become substantially larger than the shadow mask opening (1.2×1.2 $mm^2$) with the prolonged plasma treatment. We argue that plasma can penetrate into the narrow vertical gaps between mask and substrate and etch SAM larger than the original mask pattern above a certain exposure time.

 

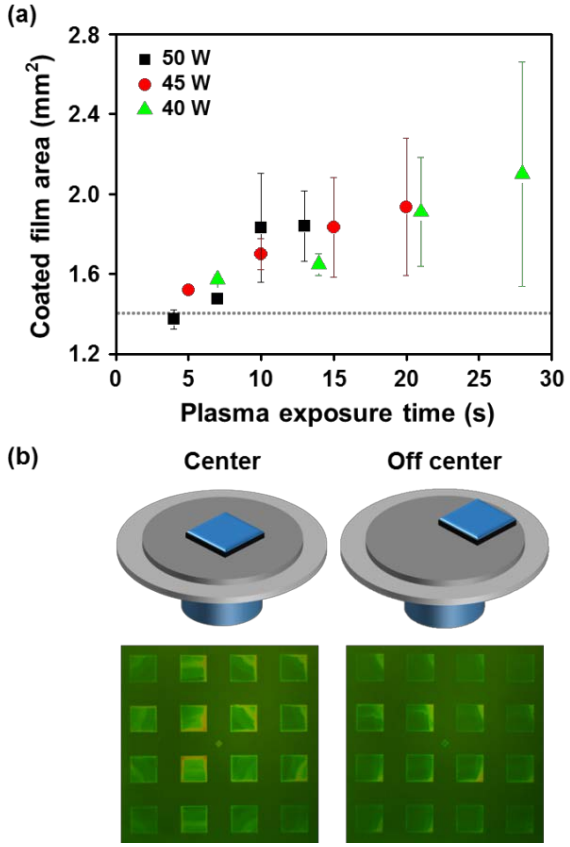


**Fig. 2** Optimization of experimental variables (i.e., plasma power, exposure time, and spin coating conditions) for selective surface wetting: (a) Effect of plasma treatment time on the actual IGZO film area. The dotted line indicates the shadow mask opening area (1.44 $mm^2$). (b) Optical micrographs of the directly patterned IGZO film arrays spin-coated at the center (left) or off-center position (right) of the chuck. Spinning rate was set at 4000 rpm for 30 sec.

Considering that the over-etching becomes prominent after 10 sec and that shorter exposure time requires larger plasma power to grant the same plasma energy, the optimal plasma exposure time was set between 4 and 7 sec at the power of 50 W.

Next, various spinning conditions were also tested for uniform film deposition on selectively plasma-etched areas. It is noteworthy that the uniformity of coated sol-gel oxide film is typically hampered by edge-bead formation, which is an inevitable phenomenon at spin-coating, due to the surface tension-induced recoiling that competes with centrifugal force during spin-coating.[23] Fig. 2(b) shows the optical images of directly-patterned IGZO films positioned at the chuck center and off-center while the whole chuck was spun at the rate of 4000 rpm for 30 sec. We found that film uniformity with marginal edge-bead formation can be significantly improved by positioning the substrate at the off-center rather than at the center of the spinning chuck because the centrifugal force is proportional to the overall distance from the spinning center.[24] With this result, all the film coatings in the following were performed at the off-center for further device fabrication.

Metal oxide TFTs were constructed using directly-patterned metal oxide films as an active channel in order to minimize

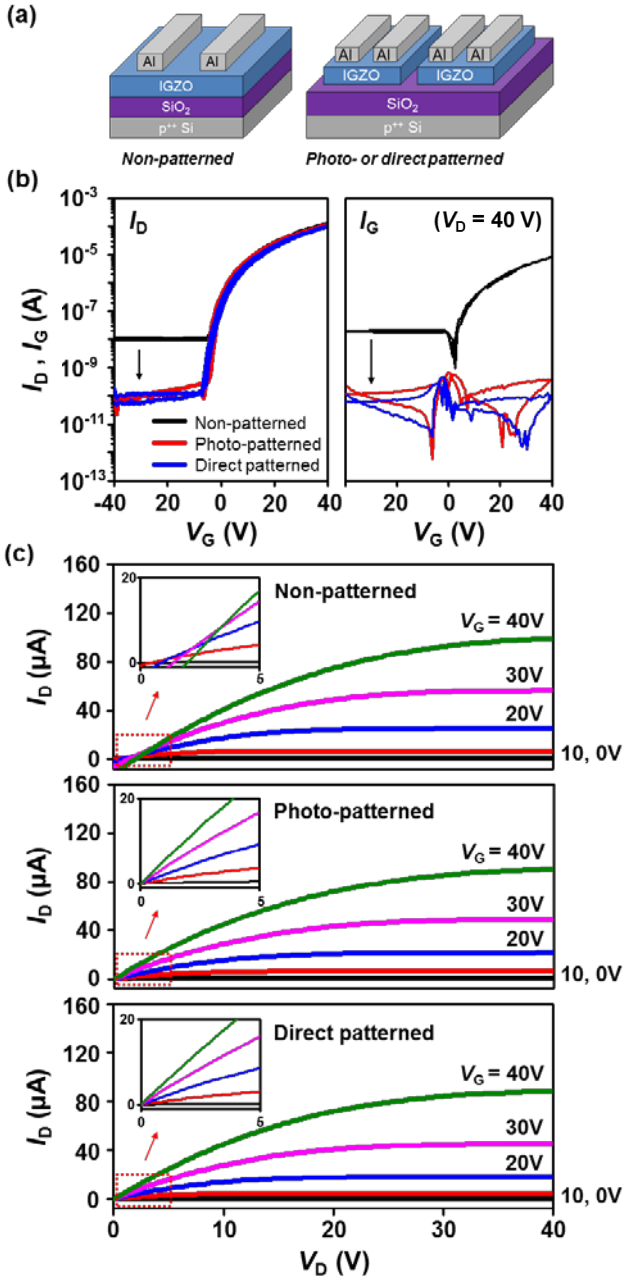


**Fig. 3** (a) Schematic structures of non-patterned (left) and photo- or direct patterned (right) IGZO TFTs. (b) Representative TFT characteristics showing the drain current ($I_D$, left) and the gate leakage current ($I_G$, right) in TFTs with a non-patterned (black), photolithographically-patterned (red), and directly-patterned (blue) IGZO layer. Applied $V_D$ was 40 V. (c) Output characteristics of the non-patterned (upper), photo-patterned (middle), and directly-patterned (lower) IGZO TFTs.

undesired leakage and off-state channel currents via device-to-device isolation. Sol-gel IGZO films were deposited on top of a $p^{++}$-Si substrate with a thermally grown 300-nm $SiO_2$ layer as a gate dielectric. Fig. 3(a) illustrates the three types of IGZO TFTs: *non-patterned*, *photo-patterned*, or *directly-patterned* indicates IGZO TFTs with a metal oxide layer coated over the whole substrate, isolated from other devices by the conventional photolithography, or direct-patterning, respectively. Fig. 3(b)

**Table 1** Device performance parameters of the IGZO TFTs with 300-nm $SiO_2$ dielectric (extracted from the transfer plots in Fig. 3(b)).

| | $\mu$ ($cm^2$ $V^{-1}s^{-1}$) | $V_T$ (V) | $SS$ (V $dec^{-1}$) | $I_{on}/I_{off}$ |
|---|---|---|---|---|
| Non-patterned | 1.87 | 6.22 | 4.87 | ~$10^4$ |
| Photo-patterned | 1.34 | 2.24 | 2.51 | ~$10^6$ |
| Direct patterned | 1.32 | 3.69 | 2.93 | ~$10^6$ |

displays transfer characteristics of these three types of IGZO TFTs. All TFTs exhibit electron-accumulation mode at positive gate voltages, indicative of a typical n-type field-effect behavior. Compared with non-patterned IGZO TFTs from which significant parasitic leakage current is present in the transfer and output plots (Fig. 3(b) and (c)), patterned IGZO TFTs show substantial reduction in the off-state channel and gate leakage currents. The insets of Fig. 3(c) display that unlike the channel-patterned TFTs the output curves severely deviate from the origin showing more negative $I_D$ at $V_D$ = 0 V with higher $V_G$ due to the leakage current in the case of non-pattered device.[25] Furthermore, the device performance of the directly-patterned TFT is comparable to that of the photo-patterned TFT (Table 1), thus emphasizing that despite its simplicity our method can successfully replace the conventional photolithography. A fringing electric field can create parasitic pathways in source-drain conduction at the vicinity of the electrode edges.[26,27] Channel layer patterning effectively removes the undesired contribution to channel current, thus slightly decreasing the resultant on-state current and field-effect mobility, as manifested by the slightly reduced mobility values in the patterned devices.

Although device operational voltage, gate leakage current, and device-to-device crosstalk are mainly determined by gate dielectric properties and its patterning, searching for novel patterning methods for solution-processed electronic materials has been concentrated mainly on semiconducting films. As high dielectric constant and thin insulator layer become more and more important for low voltage operation and reduced power consumption of TFT devices, it is unavoidable to spatially pattern gate dielectric film and reduce device-to-device crosstalk. Patterning of $AlO_x$ gate dielectric layer was performed by using OTS on $n^{++}$-Si. Subsequently, metal-insulator-semiconductor (MIS) devices with a top Au electrode were fabricated for electrical characterization of patterned dielectric films. Fig. 4(a) presents the representative plots of current density-voltage ($J$-$V$) and areal capacitance-frequency ($C_i$-$f$) obtained from MIS devices incorporated with a patterned 7-nm $AlO_x$ film. We confirmed that the capacitors with patterned and non-patterned $AlO_x$ behave similarly showing low leakage current density of ~$10^9$ A $cm^{-2}$ at 1 MV $cm^{-1}$ and large areal capacitance of 360 nF $cm^{-2}$ at 10 kHz.

Finally, all solution-processed metal oxide TFTs containing directly-patterned semiconductor and dielectric layers were successfully fabricated. To realize the bottom gate configuration,

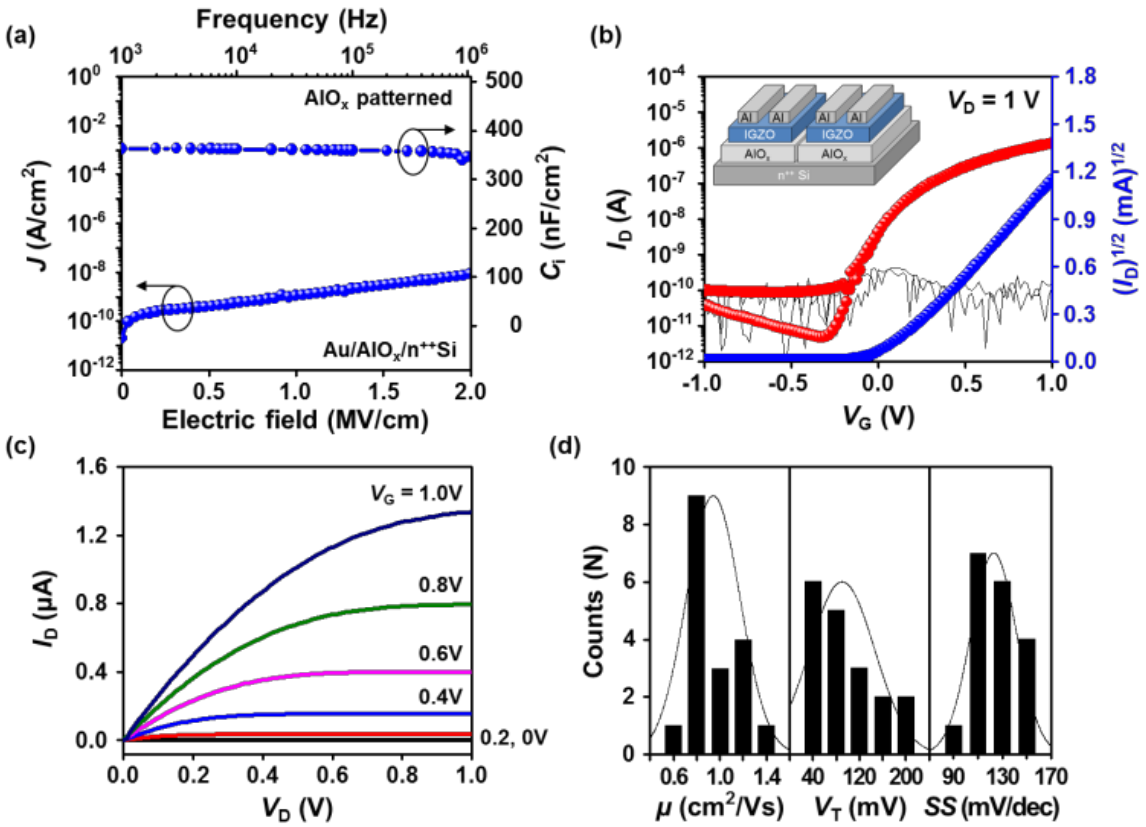


**Fig. 4** (a) Representative current density ($J$) vs. electric field ($E$) and areal capacitance ($C_i$) vs. frequency ($f$) plots of the MIS devices using a directly patterned $AlO_x$ film as an insulating layer. (b) Transfer and (c) output characteristics of a low-voltage IGZO-$AlO_x$ TFT fabricated by two successive direct-patterning processes. (d) Statistical variations of field-effect mobility ($\mu$), threshold voltage ($V_T$), and subthreshold swing ($SS$) of the resultant TFT devices. (The solid lines indicate normal distributions.)

$AlO_x$ layer was directly patterned first on $n^{++}$-Si substrates using OTS. Subsequently, IGZO patterning was performed after selective ODPA passivation on the patterned-$AlO_x/n^{++}$-Si substrate (see Supplementary Information, Fig. S2). The film thickness (~10 nm) of IGZO was controlled by precursor concentration and spinning rate, and confirmed by ellipsometry measurements. The double-patterned TFT devices with top-contact Al source/drain electrodes were fully operative with very low voltage (below 1 V), benefiting from the high capacitance of thin $AlO_x$ dielectric. The off-state drain current and the gate leakage currents were substantially reduced by using the patterned IGZO channel layer (Fig. 4(b) and (c)). From device characterization statistics (Fig. 4(c)), the fully patterned TFTs show average field-effect mobility ($\mu$) of 0.94 ± 0.22 $cm^2 V^{-1}s^{-1}$, current on/off ratio of ~$10^5$, threshold voltage ($V_T$) of 90 ± 54 mV, and sub-threshold swing (*SS*) of 122 ± 18 mV per decade. To the best of our knowledge, our work is the first demonstration of universal direct-patterning method that is successfully applied to both metal oxide semiconducting and dielectric films on the same substrate in a sequential way for constructing all solution-processed low-voltage $MO_x$ TFTs.

In summary, we have developed a simple and scalable method for directly patterning metal oxide semiconductors and dielectrics via selective surface wetting. OTS and ODPA SAMs were utilized for hydrophobic surface passivation, and plasma treatment through shadow mask was proven very effective for etching specific hydrophobic areas. Directly-patterned IGZO TFTs were fabricated by spin-coating on pre-patterned $AlO_x/n^{++}$-Si substrates, leading to high-performance all-solution metal oxide TFT with low operation voltage and low leakage current. Our method is expected to be generalized for other solution-processable metal oxide devices, thus opening up a new possibility for low-cost manufacturing of high-performance metal oxide electronics.

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## Notes and references

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† Electronic Supplementary Information (ESI) available: Experimental details, images of the patterned IGZO films, water contact angle on $AlO_x$. See DOI: 10.1039/c000000x/

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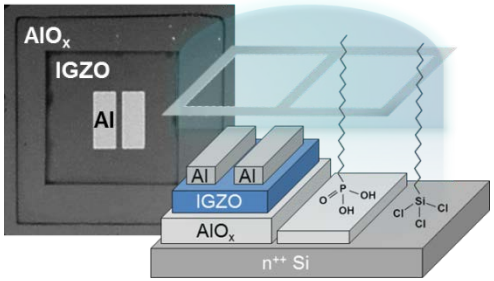
# Table of Contents Graphic




***Simple, photolithography-free, direct patterning of solution-processed metal oxide materials was developed for fabricating all-solution low-voltage metal oxide thin-film transistor arrays.***