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Paste-Type Thin-Film Transistors Based On Self-Supported Chitosan Membranes

Guodong Wu^{1,2*}, Hui Xiao²

1) School of Electronic Science and Engineering, Nanjing University, Nanjing 210093, People's Republic of China

2) Ningbo Institute of Material Technology and Engineering, Chinese Academy of Sciences, Ningbo 315201, People's Republic of China

Abstract

Chitosan is a most common biopolysaccharide and has been widely used for bio- or medical-materials. In this work, chitosan was prepared in the form of self-supported proton-conducting membranes with high proton conductivity of 2.3×10^{-3} S/cm by protonic acid doping at room temperature. These chitosan-based self-supported membranes were then used as both flexible substrates and gate dielectrics for fabricating paste-type thin-film transistors (TFTs). The feature of these paste-type TFTs is all the electrodes (gate/source/drain electrodes) and channels are located on the same one side of chitosan dielectric membranes, which is very convenient for TFTs to be transferred and stuck on various places in a wide variety of applications. Due to the huge lateral electric-double-layer (EDL) capacitive coupling induced by spatial movement of protons in chitosan-based proton-conducting membranes, these TFTs showed a low-voltage operation of only 1.5 V with a large field-effect mobility of $20.2 \text{ cm}^2/\text{V}\cdot\text{s}$. Furthermore, AND logic operation was also demonstrated on these TFTs. Our results indicate these chitosan-based paste-type TFTs have great potential for broadening their applications on wearable electronic products and biocompatible

electronics.

Keywords: Self-supported chitosan-based proton conductors; paste-type thin-film transistors; lateral electric-double-layer capacitive coupling; AND logic.

* Corresponding author. Tel: +86 25 8359 6644.

E-mail address: wuguodong110110@163.com

Introduction

Thin-film transistors (TFTs) are the key electronic components which have been widely applied in active matrix liquid crystal display (AMLCD), radio frequency identification (RFID) cards, field-effect sensors and so on.¹⁻³ Recently, a new type of TFTs, named electric-double-layer (EDL) TFTs, was proposed and attracted much attention.⁴⁻⁵ The feature of EDL TFTs is involving solid electrolytes as gate dielectrics to create enhanced functionality in devices. Compared to conventional dielectrics, these solid electrolyte gate dielectrics can support very high field-induced charge densities, and the formation of a highly charged EDL enhances greatly capacitive coupling.⁶ Not only do these TFTs operate at low voltage as a result of greatly enhanced capacitive coupling, but they also has potential application in monitoring and sensing biologic ionic signals.⁷ For EDL TFTs, the materials of solid electrolyte gate dielectrics occupy the most crucial part. Up to now, a series of solid electrolytes, such as polyelectrolytes, ionic gels, nanogranular oxide proton conductors, etc., have been employed as the gate dielectrics for EDL TFTs.⁸⁻¹¹ For example, Frisbie group reported P3HT-based TFTs gated by ion gel composed of [EMI][TFSA], showing a low operation voltage of 1.0 V and a high current on/off ratio of 10^5 .¹² Wan's group

has developed nanogranular oxide (SiO_2 , Al_2O_3) films with a high EDL capacitance ($>1.0 \mu\text{F}/\text{cm}^2$). Thanks to the huge EDL capacitance, simple-structure oxide-based TFTs (e.g. Junctionless TFTs) were easily self-aligned for low-cost TFTs applications.¹³⁻¹⁴ However, these devices are always fabricated on substrates such as glass, Si, plastic and so on. To break through the substrates limitation and apply conveniently in various occasions, the exploration of suitable materials as gate dielectrics and development of novel structure are of great importance.

Chitosan is a biodegradable, biocompatible, nontoxic, and low-cost polymer. They have been widely used for bio- or medical-materials, such as a tissue engineering material, surgical tape, and artificial skin.¹⁵⁻¹⁷ Besides, due to its high proton conductivity by acid doping, chitosan has also attracted great attention as solid electrolyte membrane in fuel cells and synaptic transistors.¹⁸⁻²⁰ In this work, in order to reduce the dependence on substrates, chitosan-based biopolysaccharide membranes in self-supported form with high proton conductivity were used as both flexible substrates and gate dielectrics for fabricating paste-type TFTs. These paste-type TFTs feature that all the electrodes (gate/source/drain electrodes) and channels are located on the same one side, which is also treated as special free-standing TFTs. Due to the huge lateral EDL capacitive coupling induced by spatial movement of protons in chitosan-based proton-conducting membranes, these TFTs showed only 1.5 V operating voltage and high-performance electric characteristics. Furthermore, AND logic operation was also demonstrated with double-planar-gate structure on these TFTs.

Experimental

All the device fabrication process is illustrated in Fig.1(a) and 1(b). Fig.1(a) shows the schematic diagram of self-supported chitosan-based proton-conducting membranes fabrication process. The process is listed as follows: (1) Coating: chitosan solution (4 wt% in acetic acid) was drop-casted onto a glass substrate with a fixable square silicone mask. (2) Drying: the obtained chitosan-based coating was dried at 30 °C in a ventilated oven for 24 hours. (3) Peeling: the silicone mask was taken away after drying and then the chitosan-based membrane was peeled off from the glass substrate. Thus, the self-supported chitosan-based membrane was prepared. Then, the as-prepared self-supported chitosan-based membrane was used as both the flexible substrate and gate dielectric for fabricating paste-type TFTs. Here, in order to simplify the structure of device, we introduce junctionless structure of TFTs in our device. As shown in Fig.1(b), IZO films arrays were deposited on the self-supported chitosan-based membrane by RF magnetron sputtering and patterned using a metal shadow mask. The length and width of the patterned IZO films is 1000 μm and 150 μm , respectively. In such junctionless TFTs, channels and source/drain electrodes are integrated in one patterned IZO film without any channel/source or channel/drain junction. The actual length of channel is decided by the distance of two tungsten probes pressured on the source/drain electrodes.²¹ Here, the length and width of channel is 100 μm and 150 μm , respectively. Field-emission scanning electron microscope (FESEM, Hitachi S-4800) was used to analyze the cross-sectional images of chitosan-based proton-conducting films. Solartron 1260 impedance analyzer was

used to measure complex impedance of chitosan-based proton-conducting membranes with sandwich structure (ITO/chitosan-based proton-conducting membrane/IZO). Keithley 4200 semiconductor parameter analyzer was used to test the electrical characteristics. Both the complex impedance analysis and electrical characteristics were performed at room temperature in air ambient at the relative humidity of 60%.

Results and discussion

Fig.1(c) shows the schematic diagram of these free-standing junctionless TFT arrays. Each pair of patterned IZO layers is a planar-gate junctionless TFT. One patterned IZO layer is used as planar gate electrode, and the other integrates channel and source/drain electrodes. All the electrodes (gate/source/drain electrodes) and channels are located on the same one side of chitosan dielectric membranes in our device, which is very convenient for TFTs to be transferred and stuck on various places in a wide variety of applications. Therefore, they can be considered as paste-type TFTs. Fig.1(d) shows a photo of these paste-type TFTs, which indicating its flexible nature.

In general, the ionic conductivity of chitosan in natural state is as low as 10^{-9} S/cm⁻¹ though abundant amino and hydroxyl functional groups exist in chitosan. These groups graft on the polysaccharide framework with strong chemical bonds and they can not work as the mobile ions. However, when the chitosan is doped by acetic acid, the protonation process occurs in chitosan molecules.²² The proton (H⁺) is dissociated from acetic acid and results free amino group in the chitosan backbone in protonation ($-\text{NH}_2 + \text{HAc} \leftrightarrow -\text{NH}_3^+ + \text{Ac}^-$). At the same time, the water molecules

absorbed in the chitosan chains can form hydrogen-bond sites for the proton transferring from amino groups to water molecules ($-\text{NH}_3^+ + \text{H}_2\text{O} \leftrightarrow -\text{NH}_2 + \text{H}_3\text{O}^+$).²³ The specific mechanism of protonation process for chitosan in the acetic acid solution can be seen in our previous report.²⁰ In order to evaluate the proton conductivity of as-prepared self-supported chitosan-based membrane, the Cole-Cole plot was characterized in Fig.2. Impedance spectroscopy data are collected as real ($\text{Re } Z'$) and imaginary ($\text{Im } Z''$) components of the complex impedance. The impedance real value (R) of $740 \text{ } \Omega$ is obtained with the impedance imaginary value equal to zero. The conductivity (σ) could be obtained from the relation below:²⁴

$$\sigma = \frac{D}{(R - R_0)A}$$

where D , A and R_0 are the thickness of as-prepared self-supported chitosan-based membrane, electrode surface area, and the resistance of the electrodes, respectively. The thickness D is $\sim 25 \text{ } \mu\text{m}$ (as shown in Fig.3(a)), A is $\sim 1.5 \times 10^{-3} \text{ cm}^2$, while R_0 is measured to be $\sim 30 \text{ } \Omega$. Therefore, the conductivity (σ) is estimated to be $\sim 2.3 \times 10^{-3} \text{ S/cm}$, indicating that the as-prepared self-supported chitosan-based membrane shows high proton conductivity at room temperature. Here, we should point out the water absorption can create plenty of proton-conducting hydrogen-bond chains which serve as proton wires for proton transfer to occur, protons originated from the protonated amino groups can move along the hydrated molecule hydrogen-bond network following the Grotthum mechanism.^{20,25} Abundant mobile protons are essential for high proton conductivity in our self-supported chitosan-based proton-conducting membrane.

Fig.3(a) shows the cross-sectional SEM image of the self-supported chitosan-based proton-conducting membrane. Loose microstructure with nanopores is observed, which is favor for proton migration. Insert image in Fig. 3(a) is the higher magnification SEM image. It clearly shows the diameter of the nanopores is ~ 300 nm. It is known that the capacitance of dielectrics is a crucial factor for high performance of TFTs.²⁶ In previous studies, vertical sandwich capacitive structure was adopted because bottom-gate or top-gate configuration was always employed in conventional TFTs. Here, in our case, the planar capacitive structure is performed for exploring planar TFTs. As shown in Fig.3(b), using an planar structure of IZO/chitosan-based proton-conducting membrane/IZO (the distance between coplanar IZO electrodes is $300 \mu\text{m}$), the lateral specific capacitance as a function of frequency in the range between 0.1 Hz and 1.0 M Hz was measured. It can be seen that the specific capacitance increases with frequency decreasing. The specific gate capacitance is $\sim 7.6 \mu\text{F}/\text{cm}^2$ at 1.0 Hz. For conventional dielectrics, the lateral capacitive coupling is extremely weak in this $300 \mu\text{m}$ long distance. Therefore, such huge lateral capacitance is mainly attributed to the lateral movement of protons in chitosan-based proton-conducting membrane and the formation of EDL at the chitosan/IZO electrode interface, as shown in Fig.3(c).²⁷ The large lateral specific capacitance in self-supported chitosan-based proton-conducting membrane can provide a strong capacitive coupling effect even the long planar distance existed, which is meaningful for fabricating low-voltage and high-performance free-standing planar TFTs. Fig. 3(d) shows that the self-supported chitosan-based membrane has a leakage current below

50 pA with the bias voltage between -1.6 V and 1.6 V, indicating the as-prepared chitosan-based membrane is an electronically insulating but proton-conducting membrane. At the same time, it ensures the leakage current is too small to influence the operation of the as-fabricated TFTs.

Previously, there were a few reports on free-standing TFTs. However, these free-standing TFTs still employed conventional bottom- or top-gate configuration which the gate electrodes and channel layers are separated on the two sides of gate dielectrics.²⁸ Here, making use of the large lateral EDL capacitance in self-supported chitosan-based proton-conducting membrane, free-standing planar TFTs based on the lateral capacitive coupling were fabricated, as shown in Fig.1(b). Fig. 4 (a) shows the output characteristics (I_{ds} - V_{ds}) of these TFTs. The V_{gs} was varied from -0.4 to 0.6 V in 0.2 V steps. A small hysteresis at high gate voltage is observed due to the mobile protons in self-supported chitosan-based proton-conducting membrane. The I_{ds} - V_{ds} curves of such device have well-defined linear regimes at low V_{ds} biases and saturation regimes at high V_{ds} biases, which is in good agreement with the standard theory of field-effect transistors. It also indicates a good Ohmic contact between W probe and IZO source/drain electrodes. Fig. 4(b) shows the corresponding transfer (I_{ds} - V_{gs}) curves of the device measured on a flat surface and on a convex surface with a bending radius of 20 mm. In the flat state, the curves shows a low off current of ~ 0.025 nA with a on/off ratio of 6×10^6 . The subthreshold swing was found to be 98 mV/decade. The threshold voltage (V_{th}) is calculated to be -0.16 V from the x-axis intercept of $(I_{ds})^{1/2}$ - V_{gs} curve ($V_{ds}=1.5$ V). The field-effect mobility (μ) can be

extracted from the equation in saturation region ($V_{ds} > V_{gs} - V_{th}$): $I_{ds} = WC_i \mu (V_{gs} - V_{th})^2 / 2L$,²⁹ where $L = 100 \mu\text{m}$ is the channel length (the distance of two tungsten probes that as the source/drain electrodes), $W = 150 \mu\text{m}$ is the channel width, and $C_i = 7.6 \mu\text{F}/\text{cm}^2$ is the specific gate capacitance. Therefore, saturation field-effect mobility (μ) is estimated to be $20.2 \text{ cm}^2/\text{V}\cdot\text{s}$. The influence of the bending to the electrical properties of the flexible junctionless TFTs is also investigated. The current on/off ratio, subthreshold swing, and field-effect mobility are estimated to be 7×10^6 , $100 \text{ mV}/\text{decade}$, and $18.1 \text{ cm}^2/\text{V}\cdot\text{s}$, respectively. Saturation mobility shows a small reduction of 10.3% , and other electrical parameters were almost unchanged. Our results indicate the device exhibits a good electrical stability under applied tensile strains with a convex radius of 20 mm . For conventional TFTs, the channel current is general controlled by vertical capacitive coupling. In our case, the gate voltage directly coupled to the semiconductor channel laterally by only one lateral EDL capacitor. The reason was attribute to the proton lateral hopping between hydroxyl groups and water molecules under applied electric field on planar gate. The static stability measurements on these free-standing planar TFTs were also investigated. Fig.4(c) the transient response of these TFTs to a square-shaped V_{gs} with a pulsed amplitude of $V_+ = 1.5 \text{ V}$ and $V_- = -1.5 \text{ V}$, under a constant bias of $V_{ds} = 1.5 \text{ V}$. The device exhibits a good reproducibility because the off current was almost unchanged and the current on/off ratio nearly kept to be a constant ($> 10^5$). This indicates that protons in the chitosan-based electrolyte have not penetrated into the IZO channel and no obvious electrochemical doping occurs at the IZO channel and chitosan-based

electrolyte interface when the gate potential is biased. Notably, in polyelectrolyte-gated field-effect transistors previously reported, the humidity in the atmosphere has an impact on the proton conductivity of chitosan and the response speed of TFT devices.³⁰ Here, in our device, we will further systematically study the polarization mechanism of chitosan-based electrolyte films under different humidity and their influence on the performance of TFT devices in the next step.

Further, with introducing another planar gate, AND logic operation was realized on the free-standing double-planar-gate TFTs. The double-planar-gate configuration was shown in Fig. 1(b), where the two planar gates (G_1 and G_2) are equivalent and symmetrical. Fig. 5(a) shows the equivalent logic principle of the double-planar-gate TFTs. Different fixed biases applied on two planar gates are characterized as Input 1 and Input 2, while the drain currents are regarded as Output. Fig. 5(b) illustrates the logic performance. HIGH input voltage bias (1.5 V) and LOW input voltage bias (-1.5 V) are denoted as state “1” and state “0”, respectively. The detected HIGH current ($>100 \mu\text{A}$) and LOW current ($<1 \text{ nA}$) are denoted as state “1” and state (“0”), respectively. When both Input 1 and Input 2 are “0”, the Output shows “0”. When both Input 1 and Input 2 are “1”, the Output shows “1”. However, when Input 1 is “1” and Input 2 is “0”, or Input 1 is “0” and Input 2 is “1”, the Output shows “0”. The results strongly indicate that such free-standing double-planar-gate TFTs realize AND logic operation with high ON/OFF ratio of $>10^5$ at the range of only 1.5 V.

Conclusions

In summary, self-supported chitosan-based proton-conducting membranes with

high proton conductivity of 2.3×10^{-3} S/cm were used as both flexible substrates and gate dielectrics for fabricating paste-type TFTs. Due to the huge lateral EDL capacitive coupling induced by spatial movement of protons in chitosan-based proton-conducting membranes, these paste-type TFTs showed only one-battery-driven (1.5 V) operation voltage and a large field-effect mobility of $20.2 \text{ cm}^2/\text{V}\cdot\text{s}$. Furthermore, AND logic operation was also demonstrated with double-planar-gate structure on these TFTs. These chitosan-based paste-type TFTs, that all the electrodes (gate/source/drain electrodes) and channels are located on the same one side, are very convenient to be transferred and stuck on various places, and have great potential for broadening their applications on biosensors and biocompatible electronics.

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References

1. C. D. Dimitrakopoulos and P. R. L. Malenfant, *Adv. Mater.*, 2002, **14** (2), 99.
2. H. Klauk, *Chem. Soc. Rev.* 2010, **39**(7), 2643.
3. J. T. Mabeck and G. G. Malliaras, *Analytical and Bioanalytical Chemistry*, 2006, **384** (2), 343.
4. T. Ozel, A. Gaur, J. A. Rogers and M. Shim, *Nano Lett.*, 2005, **5** (5), 905.
5. E. Said, X. Crispin, L. Herlogsson, S. Elhag, N. D. Robinson and M. Berggren, *Appl. Phys. Lett.*, 2006, **89** (14), 143507.
6. A. Malti, E. O. Gabrielsson, M. Berggren, X. Crispin, *Appl. Phys. Lett.*, 2011, **99** (6),

063305.

7. M. J. Panzer, C. D. Frisbie, *Adv. Mater.*, 2008, **20** (16), 3177.

8. J. H. Cho, J. Lee, Y. He, B. Kim, T. P. Lodge and C. D. Frisbie, *Adv. Mater.*, 2008, **20** (4), 686.

9. L. Herlogsson, Y. Y. Noh, N. Zhao, X. Crispin, H. Siringhaus and M. Berggren, *Adv. Mater.*, 2008, **20** (24), 4708.

10. J. Jiang, Q. Wan, J. Sun, A. X. Lu, *Appl. Phys. Lett.*, 2009, **95** (15), 152114.

11. B. J. Kim, H. Jang, S. K. Lee, B.H. Hong, J.H. Ahn and J. H. Cho, *Nano Lett.*, 2005, **10** (9), 3464.

12. J. H. Cho, J. Lee, Y. Xia, B. Kim, Y. Y. He, M. J. Renn, T. P. Lodge, C. D. Frisbie, *Nature Mater.*, 2008, **7** (11), 900.

13. G. D. Wu, H. L. Zhang, L. Q. Zhu, M. Z. Dai, P. Cui and Q. Wan, *IEEE Electron Device Lett.*, 2012, **33** (4), 531.

14. J. Jiang, J. Sun, W. Dou and Q. Wan, *IEEE Electron Device Lett.*, 2011, **33** (1), 65.

15. A. A. Aldana, R. Toselli, M. C. Strumia and M. Martinelli, *J. Mater. Chem.*, 2012, **22**(42), 22670.

16. J. K. F. Suh and H. W. T. Matthew, *Biomaterials*, 2000, **21**(24), 2589.

17. I. V. Yannas, J. F. Burke, D. P. Orgill and E. M. Skrabut, *Science*, 1982, **215**(4529), 174.

18. J. A. Seo, J. H. Koh, D. K. Roh and J. H. Kim, *Solid State Ionics*, 2009, **180**(14-16), 998.

19. B. Zhou, J. Sun, X. Han, J. Jiang and Q. Wan, *IEEE Electron Device Lett.*, 2011, **32** (11), 1549.
20. G. D. Wu, J. Zhang, X. Wan, Y. Yang and S. H. Jiang, *J. Mater. Chem. C*, 2014, **2**, 6249.
21. J. M. Zhou, G. D. Wu, L. Q. Guo, L. Q. Zhu and Q. Wan, *IEEE Electron Device Lett.*, 2013, **34** (7), 888.
22. J. Brugnerotto, J. Lizardi and F. M. Goycoolea, *Polymer*, 2001, **42**(8), 3569.
23. J. F. Nagle, M. Mille and H. J. Morowitz, *J. Chem. Phys.*, 1980, **72**(7), 3959.
24. G. D. Wu, H. L. Zhang, J. M. Zhou, A. S. Huang and Q. Wan, *J. Mater. Chem. C*, 2014, **2**, 6249.
25. C. Zhong, Y. X. Deng, A. F. Roudsari, A. Kapetanovic, M. P. Anantram and M. Rolandi, *Nat. Commun.*, 2011, **2**, 476.
26. T. Fujimoto and K. Awaga, *Phys. Chem. Chem. Phys.*, 2013, **15** (23), 8983.
27. L. Q. Zhu, C. J. Wan, L. Q. Guo, Y. Shi and Q. Wan, *Nat. Commun.*, 2014, **5**, 3158.
28. N. J. Kaihovirta, C. J. Wikman, T. Makela, C. E. Wilen and R. Osterbacka, *Adv. Mater.*, 2009, **21**(24), 2520.
29. Y. M. Sun, Y. Q. Liu and D. B. Zhu, *J. Mater. Chem.*, 2005, **15**(1), 53.
30. O. Larsson, E. Said, M. Berggren, X. Crispin, *Adv. Funct. Mater.*, 2009, **19**(20), 3334.

Figure captions

Fig.1 (a) The schematic diagram of the fabrication process for self-supported chitosan-based proton-conducting membranes. (b) The schematic diagram of the free-standing planar junctionless TFTs fabricated by one-shadow-mask technology. (c) The schematic diagram of the free-standing planar junctionless TFT arrays which can be considered as paste-type TFTs. (d) A photo of free-standing planar TFTs based on the self-supported chitosan-based proton-conducting membrane.

Fig.2 Cole-Cole plots of the self-supported chitosan-based proton-conducting membrane.

Fig.3 (a) The cross-sectional SEM image of the self-supported chitosan-based proton-conducting membrane. Inset: the higher magnification SEM image. (b) Schematic diagram of the planar test structure and the proton hopping mechanism under an applied electric field. (c) Specific capacitance of the planar test structure in the frequency range from 0.1 Hz and 1.0 M Hz (d) Leakage curve of the free-standing chitosan films.

Fig.4 (a) Output characteristics of these free-standing planar TFTs. (b) Transfer characteristics of these free-standing planar TFTs. (c) The transient response of these free-standing planar TFTs to a square-shaped V_{gs} with a pulsed amplitude of $V_+=1.5$ V and $V_-=-1.5$ V, under a constant bias of $V_{ds}=1.5$ V.

Fig.5 (a) Logic circuit diagram of the free-standing planar TFT with double-planar-gate configuration (b) Input-output characteristics of the AND logic.

Fig.1

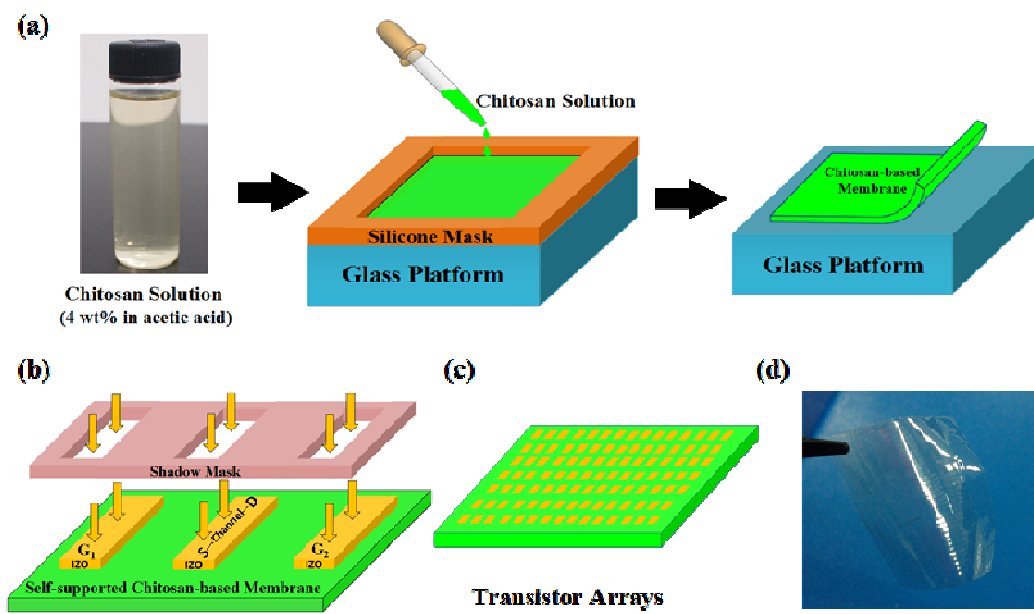


Fig.2

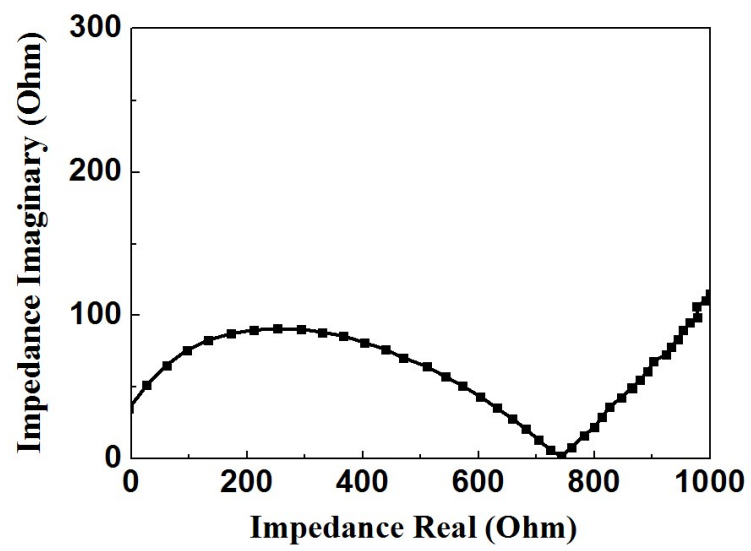


Fig.3

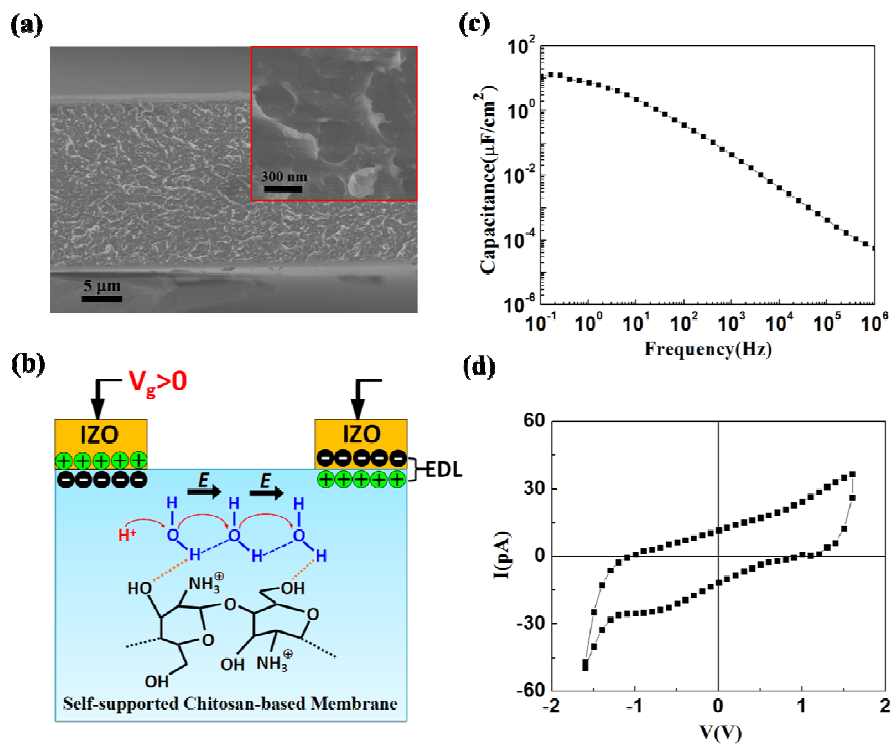


Fig.4

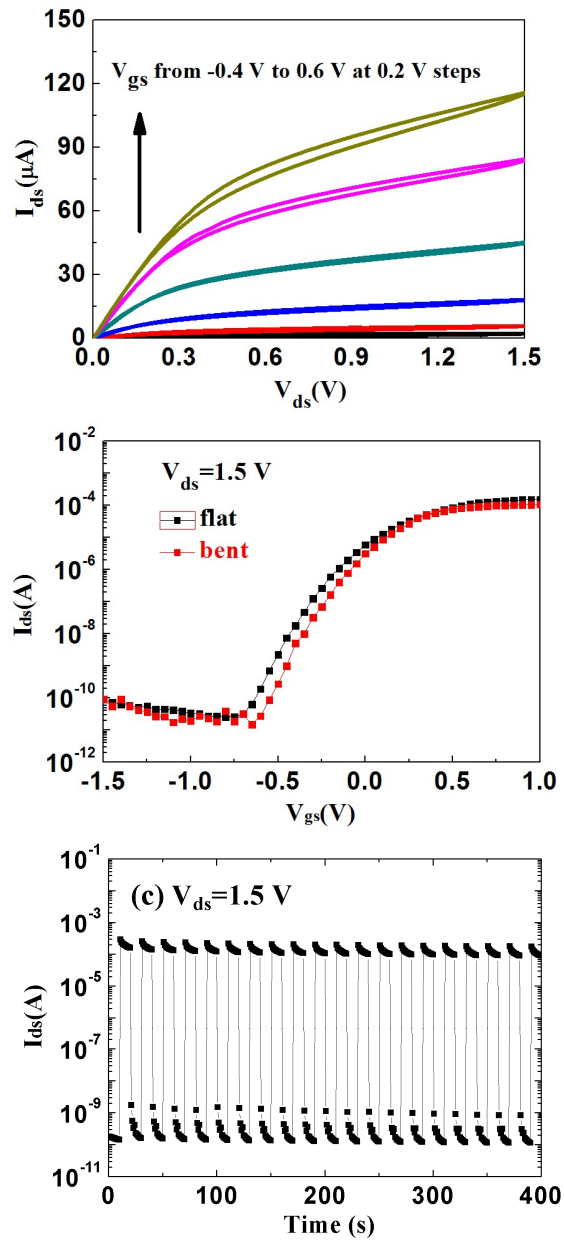


Fig.5

