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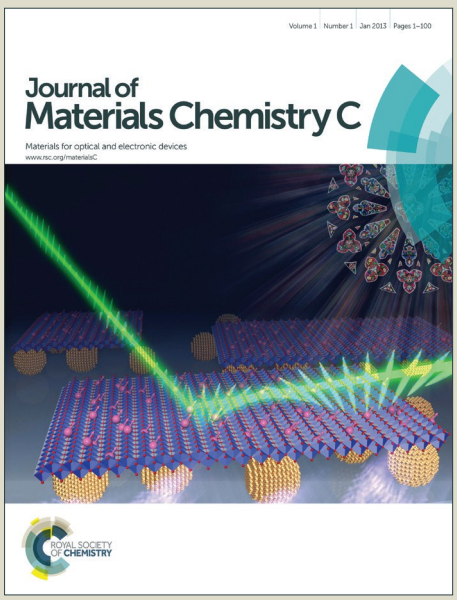

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Low Operating Voltage and Low Bias Stress in Top-Contact $SnCl_2Pc$/ CuPc Heterostructure based Bilayer Ambipolar Organic Field-effect Transistors

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Abstract: Herein, a symmetrical Ag top contact- bottom gate (TC-BG) bilayer ambipolar organic field-effect transistor based on heterojunction of vacuum-deposited small molecules, tin(IV) phthalocyanine dichloride ($SnCl_2Pc$) (n-channel) and copper phthalocyanine (CuPc) (p-channel), has been demonstrated. A hydroxyl-free poly (methyl methacrylate) (PMMA) with aluminum oxide (Al_2O_3) bilayer dielectric exhibits low operating voltage (~10 V) and low bias stress (relaxation time $\tau\sim 10^5$s) for both n-channel and p-channel cases. The optimized $SnCl_2Pc$/CuPc heterostructure exhibits balanced carrier mobility and the both type of charge carriers, electron and holes, are facilitated from the same low work function Ag contacts, depending on the bias conditions, from the TC-BG architecture. The Ag contact also exhibits Ohmic injection of charge carriers with low contact resistance in the n-channel region under optimal heterostructure configuration. The contact resistances for electron and hole-injection are strongly dependent on the thickness of the $SnCl_2Pc$ and CuPc layers, respectively. The bias stress stability is modeled using stretched exponential fitting. Our results demonstrate that the ambipolar device characteristics and performance can be controlled by adjusting the thickness of the molecular layer, which is highly desirable. Such simple heterostructure engineering with

utilization of organic molecular semiconductors can truly enable the promising low-cost and flexible organic electronics for extensive applications.

1. Introduction

Ambipolar organic field-effect transistors (OFETs) have attracted enormous attention due to their unique operation, which allows both electrons and holes to be injected and transported in the same devices, i.e., devices can operate in unipolar mode as well as in an ambipolar mode.[1-4] These devices find active applications in organic complementary logic circuits, double carrier devices like light emitting field-effect transistors for organic active matrix displays, organic photovoltaic cells (OPVs), sensors, radio frequency identification components, e-papers, and inverters.[5-9] High-performance inverters are the building blocks of the integrated circuits (ICs). Complementary metal-oxide semiconductor (CMOS) technology is desirable for the preparation of ICs because it provides straightforward circuit design, good noise margins, low power consumption, and robust operation. Organic CMOS technology requires the use of p- and n-type transistors on the same substrate.[10, 11] In addition, both hole and electron can transport within the same device (depending upon the bias condition) and recombination of opposite charge carriers within the transistor channel can result in light emission, namely light emitting field-effect transistor, which has a potential to be at heart of the next generation of light emitting devices.[12-14] For these, it needs to inject efficient balanced chage carriers (both types, electon and hole) in the channel of the device. To achieve this goal, several groups have followed different approaches: i) ambipolar OTFTs featuring symmetric or asymmetric source and drain electrodes for single or double channel organic semiconductors,[15-17] ii) bilayer heterojunction structures consisting of electron- and hole-transporting organic layers,[18-20] and iii) blending two organic semiconductors

with different charge carriers.[21-23] They all have particular characteristics and advantages as well as challenges to overcome.

In a single semiconductor, the main difficulty to achieve ambipolar transistor operation is the injection of holes and electrons into a single semiconductor from the same electrode. This electrode needs to have a work function that allows injection of holes in the highest occupied molecular orbital (HOMO) of the semiconductor, and the injection of electrons in the lowest unoccupied molecular orbital (LUMO). Consequently, this will result in an injection barrier of at least half of the band gap energy for one of the carriers (either electron or hole, as most of the standard semiconductors have band gap of ~2-3 eV). To overcome the problem of injection due to this barrier, in double-carrier devices, such as light emitting diodes and photovoltaic cells, two dissimilar, i.e. high- and low-work-function metal electrodes are used to enable injection or collection of holes and electrons.[15] Unfortunately, this approach makes circuit fabrication complex and potentially expensive. Alternatively, a single low-cost electrode material can be used in combination with two different semiconductors, where one has its HOMO level and the other its LUMO level aligned with the metal work function. Recently, Long *et al.* reported a mixed contact interlayer of transition-metal oxides that control the efficient charge injection in ambipolar diketopyrrolopyrrole-thieno[3,2-b]thiophene copolymer (DPPT-TT) organic transistors with using low-cost molybdenum (Mo)-source/drain electrodes.[24] To reduce the contact effect one can introduce a self-assembled monolayer (SAM) to lessen injection barrier, and it results into the efficient injection of electrons and holes.[25, 26]Another important challenge is the trapping of one or both type of carrier in the defects/impurities, especially electrons are likely to be trapped by impurities at certain chemical moieties at the semiconductor-dielectric interfaces and/or semiconductor surfaces. We have found that the particular choice of hydroxyl-

free low-cost PMMA buffer polymer dielectric layers (as compared to fluorinated polymer dielectric layer, CYTOP) and low work function Ag electrodes can exhibit superior performances in terms of low gate-bias stress and efficient injection.[27] Takahashi *et al*. reported rubrene single crystal ambipolar OFETS with Ag paste electrode to inject charge carriers and PMMA buffer layer to terminate the interfacial electron traps.[17] Most of the ambipolar characteristics reported in the literature are based on bottom contact SiO_2 gate dielectric and heavily doped Si wafer serving as a gate electrode. Such a rigid substrate requirement limits the flexibility of the composed circuits. Further, SiO_2 layer may contain high density of hydroxyl-groups known as electron traps, which significantly suppress the n-type device characteristics. Therefore, the majority of the OFETs have reported p-type transistors with high work function Au- electrode that serve as a hole injection layer and these devices are highly gate-bias stress sensible (i.e., drain source current I_{DS} decays substantially under biased condition for a prolonged time). Low bias stress devices are highly desirable for future commercial applications.

Among all organic semiconductors, vacuum deposited small molecules exhibit certain advantages over polymeric-thin film in terms of morphology, as demonstrated in this study, A solution processed field-effect transistor (FET) is of interest because of its potential contributions to low-cost fabrication of circuits thorough manufacturing roll-to-roll processes using conventional coating and printing techniques. Recently, Cheng *et al.* reported balanced carrier mobilities in 2-(4-n-octylphenyl) benzo[*d,d'*] thieno[3,2-b;4,5-b'] dithiophene (OP-BTDT)-based fused-thiophene derivative with small-molecule, fullerene (C_{60}), bulk heterojunction ambipolar transistors.[22] Further, due to molecular weight distribution (polydispersity), regio- and stereo-irregularity, and end-group contaminations of polymeric materials, performance of polymer-

based OTFTs could exhibit relatively large batch-to-batch variations. The lack of ambipolar transport in binary blends of polymers for most of the compositions is due to the fact that controlling the thin film morphology is a crucial factor for obtaining continuous path for both type of charge carriers. Further, a limited number of polymer blends are available due to lack of high performing solution processable n-type polymers. On the other hand, small molecule materials are easier to synthesize and high chemical purity can be achieved using techniques such as vacuum sublimation. Therefore impurities are low, which can be considered as intrinsic semiconductor and can greatly improve reproducibility of fabricated devices as compared to that of polymeric materials. Small molecules can easily be purified by various methods of chromatography, sublimation, and recrystallization, while polymers can only be purified by recrystallization.

Therefore, bilayer heterojunction structure appears to be one of the very promising approaches for device fabrication, as they are readily deposited on the same substrate without breaking the vacuum. Unfortunately, carrier mobility in these devices rarely exceeds the order of 10^{-3} cm^2 V^{-1} s^{-1} because of poor control over molecular packing. In general, organic-based large electronic circuit may need >1800 transistors and as the number of transistors per circuit increases, there is an increasing need for circuits characterized by low power dissipation, high noise margin, and greater operation stability.[6] So, the high operating voltage and environmental stability of ambipolar OFETs are still major challenges for their commercial applications.

To reduce the operating voltage, herein, we used an anodized Al_2O_3, modified with PMMA, as a buffer gate dielectric layer instead of commonly used SiO_2 layer. The optimized $SnCl_2Pc$/CuPc

heterostructure ambipolar OFETs with operating voltages down to 10 V and carrier mobilities of 1.8×10^{-4} $cm^2\ V^{-1}\ s^{-1}$ and 2.1×10^{-4} $cm^2\ V^{-1}\ s^{-1}$ for hole and electron, respectively, are demonstrated here. The heterojunction OFET's consisting of p-type CuPc and n-type $SnCl_2Pc$ have been chosen for the following reasons: i) they possess almost identical molecular shapes, and very similar crystal packing structures and grain sizes under the same deposition conditions, so it may be convenient to produce a heterojunction with nearly perfect crystalline interface, ii) the field-effect mobility (μ_{FE}) of carriers in these two materials is very similar at a level of 10^{-1} $cm^2\ V^{-1}\ s^{-1}$ in unipolar case.[28, 29] So, it may be easier to get the balance ambipolar characteristics with engineering of small molecules. Several groups reported that low band gap organic semiconductors, especially small molecules based semiconductors are promising candidates for ambipolar OFET's.[18, 30, 31] Most studies reported on ambipolar OFETs focus on the hole and electron field-effect mobilities (μ_h and μ_e, respectively), while the issues of the bias stress effect (drain current (I_{DS}) instability with prolonged operation of time) and contact resistance (R_C) have been addressed rarely, except in a few reports, especially for bilayer heterostructure ambipolar OFETs. As the gate-bias stress effect and R_C effect can be critical factors to limit the practical applications of ambipolar OFETs, it is essential to investigate the contact resistance as well as gate-bias stress effects for both holes and electrons in the organic bilayer structure.[19, 32, 33]

2. Result and discussions

In the bilayer heterostructure, depending on the device configuration and on the materials used, charge accumulation and transport of electrons and holes can occur in different layers. However, at least one of the two accumulation zones will form at the interface and therefore charge transport will depend on the quality of this interface. Consequently, an accurate control of the

growth conditions of the evaporated film is necessary. The top contact-bottom gate (TC-BG) ambipolar bilayer device structure with silver (Ag) as source/drain (S/D) electrodes and the chemical structures of small band-gap molecules tin(IV) phthalocyanine ($SnCl_2Pc$) and copper phthalocyanine (CuPc) are shown in **Fig.1(**a). In general, top contact OFETs exhibit the lowest contact resistance, at least two orders of magnitude lower, because of the increased metal-semiconductor contact area in this configuration.[34] Details of fabrication procedures for devices are provided in the experimental section. CuPc was deposited as the first active layer on the top of the insulator PMMA/Al_2O_3 and $SnCl_2Pc$ was deposited as a second active layer on the top of CuPc layer. The bilayer dielectrics PMMA/Al_2O_3 enable low voltage operation. PMMA as a polymer dielectric is chosen since no chemical groups (-OH) are present at its surface that may act as electron traps, and shows very low bias stress effect, low contact resistance and is of low cost compared to other hydroxyl-free flouro polymer, like CYTOP.[27, 35] The same device structure is reported to show the low bias stress (time constant ~10^5 s) and low operating voltage (10 V). Herein, we used Ag electrodes as a top-contact source/drain (*S/D*) electrodes, instead of the usual gold electrodes, which facilitate the electron injection due to their low work function. In addition, top contact-bottom gate (TC-BG)-OFET behaves as inverted-staggered and TC-BG transistor is affected by current crowding effect, in which contact resistance, R_c is lower than the channel sheet resistance R_{ch}.[36] The schematic energy level diagram of $SnCl_2Pc$ and CuPc – heterostructure with symmetric Ag-contact is shown in **Fig.1(**b) (under zero bias condition). The lowest unoccupied molecular orbital (LUMO) level of $SnCl_2Pc$ is at 4.0 eV,[37] which has a very small difference with Fermi energy level (E_F) of silver (Ag) (work function $\Phi \approx 4.3$ eV), and it results in an Ohmic electron injection (i.e., an output drain-source current initially increase and finally saturated) into the LUMO level of $SnCl_2Pc$ layer. It is known that a good Ohmic contact

can be achieved when the work function of metal is closely matching with the LUMO or HOMO energy level of the semiconductor. On the other hand, the difference between HOMO level of CuPc and Fermi energy of Ag is quite large (≈ 0.9 eV). When the gate bias is applied, the band-bending occurs at the metal/semiconductor interface and reduce the energy barriers and will allow tunneling of charge carriers from the electrode to the semiconductor. Note that we did not find any ambipolar signature for CuPc/$SnCl_2Pc$ (top/bottom) bilayer heterostructures for CuPc(60nm)/$SnCl_2Pc$(12nm) device, though it may be possible to obtain ambipolar behavior for thinner layer combinations. Therefore, $SnCl_2Pc$/CuPc (top/bottom) heterostructure pair is found to be an excellent choice for obtaining ambipolar characteristics.

The performance of electronic devices depends crucially on depletion width, film thickness, and in particular the spatial location of trap states, either in organic/organic or organic/dielectric interface. In addition, an energy land scape at organic-organic interface is complicated due to several electrostatic phenomena, such as charge transfer, dipole generation and/or dipole orientation, and doping, which are related to the feature of molecular structure (orientation), crystallinity, inter-diffusion, and domain size. Therefore, it is necessary to track the evolution of device characteristics with film thickness.[30, 38]

In order to investigate the crystalline quality of the $SnCl_2Pc$/CuPc heterostructure, we carried out X-ray diffraction (XRD) analysis with Cu-K_α radiation (λ= 1.54056Å). The XRD pattern of $SnCl_2Pc$ thin film of thickness 60 nm grown on CuPc bottom layer of different thicknesses (4, 12 and 16 nm) is shown in Fig.S1 (Supporting Information). $SnCl_2Pc$ layer without the CuPc layer shows XRD peaks at 2θ= 10.48˚ and 12.18˚ corresponding to (010) and (100) crystalline planes,

respectively, of $SnCl_2Pc$. With the introduction of CuPc bottom layer, the intensity of the XRD peaks related to $SnCl_2Pc$ decreases and a new peak appears at $2\theta = 6.84^{\circ}$ for the 12 nm and 16 nm CuPc films. The peak at $2\theta = 6.84^{\circ}$ results from (200) lattice planes of CuPc, where the inter-stacking distance is $d \approx 12.9$Å. It implies that the trace of herring bone pattern is parallel to the substrate.[18] The presence of distinct peaks in the XRD pattern for SnCl2Pc film implies the formation of the crystalline film and inter-molecular π- π stacking parallel to the substrate. This feature implies that the crystalline quality of thin film is appropriate to expect good transport of charge carriers in the OFET geometry.[29]

We used an atomic force microscope (AFM) to study the surface features of the as-deposited films that have influence on the ambipolar behavior of the fabricated transistors, and to investigate whether the CuPc to $SnCl_2Pc$ thickness variation have any influence on the phase-separated network. **Fig.2**(a-c) shows the AFM images in tapping mode of the $SnCl_2Pc$ thin film (60 nm) grown over the CuPc layer with different thicknesses (4, 12 and 16 nm) at a substrate temperature 60 ºC. It is noticeable that the root-mean-square roughness (R_q) of $SnCl_2Pc$ thin film becomes higher at higher thickness of CuPc ($R_q \approx 1.7$ to 2.2 nm). The thickness of the CuPc film is controlled by building up of separate single layers. At a very low thickness deposited at 60 ºC, voids may appear in the film, since all grains are not fully connected with each other, and it provides the location upon which the second layer can grow. Thus, the $SnCl_2Pc$/CuPc heterojunction interface is expected to be smooth with the ultra-thin CuPc layer, but it may become little rougher at higher CuPc thickness.

A typical unipolar OFET based on vacuum-deposited $SnCl_2Pc$ exhibited carrier mobility of 0.01 $cm^2\ V^{-1}\ s^{-1}$, as reported in the previous work.[27] The bilayer heterostructure ambipolar OFET device charateristics are shown in **Fig.3**(a)-(f) and in **Fig.4**(a)-(c) with optimal 60-nm thick $SnCl_2Pc$ and x-nm (x = 4, 12, and 16 nm) thick CuPc bilayer heterostructure. Fig.3(a), 3(d) and 4(a) shows the output characteristics (I_{DS} -V_{DS}), Fig.3(b-c), 3(e-f) are the transfer characteristics in p-channel and n-channel region for CuPc-thickness of 4 nm and 12 nm, respectively. The bilayer heterostructure OFETs show V-shape transfer characteristics typical of ambipolar transistors of n-channel and p-channel ambipolar OFET under low vacuum (~10^{-3} mbar) and in dark condition with electron and hole mobility of 5×10^{-4} and 3×10^{-4} $cm^2\ V^{-1}\ s^{-1}$ for n-channel and p-channel, repectively. In the case of thick CuPc with corresponding rough heterojunction interface, hole- current dominates I_{DS} and while the electron-dominant I_{DS} is supressed. The device parameters are summarized in **Table 1**, $V_{Th,e}$, and $V_{Th,h}$ are threshold voltages for the top n-channel and bottom p-channel, respectively. A noticeable hysteresis in the output characteristics of p-channel regime may be due to hole scattering and/or trapping at CuPc/PMMA interface (as the thin CuPc layer may have formed interconnected grains, not fully covered on the dielectric surface). Sinc the gowth of heterostructure was sequential and performed under the vacuum condition, measurement of surface roughness of only CuPc layer was not possible. The mechanism of charge carrier transport in the present heterostructure (SnCl2Pc/CuPc) transistor is schematically illustrated in Fig. 5(a) and (b) for n-channel and p-channel cases, respectively. With $V_{DS}>0$ and $V_{GS}>0$, electron conduction takes place from source to drain mainly through the $SnCl_2Pc$ layer due to the particular positions of the Fermi level and the LUMO level, as explained in Fig. 1(b). Similarly, under $V_{DS}<0$ and $V_{GS}<0$, the hole

conduction takes place through the CuPc layer only. In this way, ambipolar characteristic is obtained in the hererostructure device.

Note that at higher thickness of CuPc, μ_e is reduced marginally (see **Fig.6(**a)) that may be due to the enhanced electron scattering and/or electron trapping owing to the increased roughness of heterojunction at the $SnCl_2Pc$/CuPc interface. It is evident that the ambipolar OFETs can work well with the CuPc layer as thin as 4 nm and gives almost balanced electron and hole mobilities (~ 2×10^{-4} cm^2 V^{-1} s^{-1}), which is an interesting feature and it is crucial for applications in circuits and light emitting OFET. μ_h and μ_e in this devices are ~10^{-4} cm^2 V^{-1} s^{-1}, which is comparable to the literature reports on other CuPc based ambipolar devices.[18, 30] A number of devices (4-7) were tested for obtaining the device parameters. **Fig. S2** (supporting information) shows distribution of mobilities for representative devices with different CuPc thickness (4, 12 and 16 nm) for p-channel (left panel) and n-channel (right panel) cases. Average μ and its standard deviation for each case are mentioned in the inset. Note that the commonly reported mobility for unipolar devices is comparatively higher (~10^{-2} cm^2 V^{-1} s^{-1}) than that of the ambipolar devices. It has been generally attributed to low conductivity of evaporated CuPc and $SnCl_2Pc$ that exhibit disorder of dipole at the heterojunction interface.[31] At low values of V_{GS}, the bilayer heterojunction ambipolar transistors exhibited diode-like (super-linear) behavior, which are frequently observed for typical ambipolar transistors due to the presence of both charge carriers (electron and hole) in the active channel of the device. We attribute this behaviour to the highly negative threshold voltage $V_{Th,h}$, for p-channel operation and /or the positive threshold voltage for n-channel operation. The relatively high threshold voltages imply electron and hole trapping

at the interface between the p- and n- channel materials in the phase separated network (see Table 1).

Table 1 shows that the threshold voltages, $V_{Th,e}$ and $V_{Th,h}$, shifts oppositely towards negative and positive sides, respectively, when the roughness of the heterojunction is higher. A possible mechanism of the shift in $V_{Th,e}$ and $V_{Th,h}$ may be due to charge transfer to some extent (electrons from HOMO level of CuPc to the LUMO level of $SnCl_2Pc$) at the $SnCl_2Pc$/CuPc interface, which could be facilitated at the rough interface due to an increased interfacial area.[19] For higher thickness of CuPc layer, both the electron and the hole threshold voltages shift oppositely to more negative and positive values, respectively. In an n-channel device, threshold voltage shows a less shift $\Delta V_{Th,e} \approx 0.87$ V when the CuPc thickness is changed from 4 nm to 16 nm, and consequently the p- channel threshold shows a larger shift $\Delta V_{Th,h} \approx 3.43$ V to more positive voltages ($V_{Th,h}$ down from - 6.84 V to - 3.41 V). Thus, the shift of threshold voltage in n-channel is much smaller compared to that of p-channel device. This may occur due to the larger contact area of Ag with CuPc film with high thickness. At higher thickness of the CuPc layer, the diffusion of noble metals Ag is high in organic semiconductor. These diffused Ag impurity can create deep trap centers in $SnCl_2Pc$/CuPc layers which may affect the long term stability of the device. Note that most of the deep trap states are located directly under the metal contact layer. However, some trap states may extend to the underneath of semiconductor layer.[36, 39]

To further investigate the degree of charge trapping, we extracted the density of traps for CuPc (4nm), N_{tr} (= $C_i \Delta V_{Th}/q$, where, C_i capacitance per unit area, ΔV_{Th} is shift of threshold voltage). The trap density derived from the trans-conductance curves are 6.31×10^{11} cm^{-2} and 9.69×10^{10}

cm^{-2} at $|V_{DS}|$ = ± 4V in p-channel and n-channel, respectively. It has been proposed that deep traps are usually responsible for the shift of threshold voltage and its density is higher at the CuPc/PMMA interface than the $SnCl_2Pc$/CuPc interface. The deep trap states may be generated at both metal/organic interfaces in the contact region due to the diffusion of Ag atoms.[39] To further confirm the modulated charge injection, we analyzed the contact resistance. **Fig.6**b shows the channel width (W)- normalized contact resistance (R_c) as a function of CuPc thickness, in the *n*-channel regime (for electrons) as well as p-channel regime (for holes) of the OFETs. In an n-channel regime, the normalized contact resistance of 1.60×10^9 Ω cm for $SnCl_2Pc$ (60 nm)/CuPc (4 nm) is the smallest when compared with larger thickness CuPc layer cases. Here, R_c is extracted by the Y-function method (YFM) for individual $SnCl_2Pc$/CuPc OFETs (channel width/ channel length (W/L) of 780 μm/30 μm) using the following equation,[40]

$$R_c = \frac{V_{DS}}{I_{DS}} - \frac{1}{G_m\left(V_{GS} - V_{Th}\right)}, \qquad (1)$$

where $G_m=(W/L)\mu_0 C_i$, is the trans conductance parameters. This is in contrast to the transfer line method (TLM) used to estimate contact resistance for the amorphous silicon transistors, where one can obtain only an average R_c from the set of different channel lengths of transistors. This gives rise to scattering of data in the plot, as R_c varies from transistor to transistor. Again, this method cannot be used if contact resistance is nonlinear (i.e. departs from Ohms law), as it is applicable in linear regime. YFM offers a straightforward way to obtain the R_c in a single transistor and thereby it accesses the evolution of charge injection induced by different combination of heterostructures with same channel length, L. In devices with thickness combination, the R_cW ($R_{c,e}$) for electron injection systematically increases from 1.6×10^9 Ω-cm to 115×10^9 Ω-cm, while the R_cW ($R_{c,h}$) for hole injection does not change significantly. This is due to the importance of diffusion at the contact. As the thickness of CuPc increases, diffusion is no

longer sufficient to derive the current through the bulk of the semiconductor, since for a given number of charges induced by the gate voltage, a sizeable concentration gradient can only be maintained over a finite distance and this results in the increase in contact resistance, $R_{c,e}$ for electron conduction. Furthermore, the V_{GS} dependence of normalized R_c shown in **Fig.6(**c-d) supports the above analysis. It is noticeable that the contact resistance R_c for hole is one order of magnitude higher than that of electron for $SnCl_2Pc$/CuPc heterostructure reflecting a finite Schottky barrier at Ag/CuPc interface. It is clear that R_c decreases with increasing V_{GS} for both hole and electron injection, and it is due to the fact that higher V_{GS} induces more accumulated charges, which will increase the conductivity of contact region and follow the current crowding model.[41]

In staggered TC-BG OFETs (where contact and accumulation layer are formed at opposite sides of the semiconducting layer), the gate-voltage dependent R_c has been observed to mainly arise from current crowding. At a small gate bias, the bulk semiconductor between contacts and channel would be highly resistive if the injected charges are limited, and the injection is confined in a small contact area close to the channel. At higher gate bias, charges accumulate in the channel and also spread far from the channel interface and thus increase the bulk conductivity at contacts. Meanwhile, charge injection extends to larger contact area, as injection current gets more and more crowded and consequently R_c will be less. It has also been found that in staggered device, R_c does not change significantly. Thus, the optimized $SnCl_2Pc$/CuPc heterostructures result in gate-voltage independent R_c and signifies Ohmic contacts.

Besides the static device characteristics, the dynamic device characteristics are correlated significantly to the $SnCl_2Pc$/CuPc heterojunction. **Fig.7(**a) shows the bias stress results at positive V_{GS} and V_{DS} ($V_{GS} = V_{DS} = 8$ V) in the ambipolar OFETs, i.e., the operational instability of electron-dominant drain-source current, $I_{DS}(t)$, normalized by $I_{DS}(0)$, where $I_{DS}(0)$ *is the* initial maximum source-drain current established right after the transistor is on (in n-channel and p-channel regime) for $SnCl_2Pc$ (60 nm)/CuPc(4 nm). In $SnCl_2Pc$/CuPc bilayer heterojunction OFETs, the bias stress effect under dark condition is very small; the current decreases by only 5–7 % after a continuous bias-stressing for 1 h at $V_{GS} = V_{DS} = 8$ V for n-channel (Fig.7(a)) and in p-channel regime ($V_{GS} = V_{DS} = -8$V) it shows a similar small decay (<10%, see **Fig.7(**b)). It is noticeable that initially (t<50 s) I_{DS} increases to some extend and then it decays for longer time for both n-channel and p-channel devices. It is believed to be caused by dipoles that can be oriented at the PMMA/Al_2O_3 interface or at Al_2O_3 bulk.[42] Although the $SnCl_2Pc$-based unipolar OFETs show good bias stress stability, the bias stress effect for electron-dominant I_{DS} in the ambipolar OFETs is generally significant.

The bias stress-induced decay of drain-source current, I_{DS}, in OFETs can be described by a stretched-exponential time (t) dependent formula applicable to wide variety of disordered systems and can be written as (when field effect mobility, μ_{FE}, is almost constant),[43, 44]

$$I_{DS}(t) = I_{DS}(0)\exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right], \qquad (2)$$

where β is the stretching parameter (temperature dependent) related to the barrier energy height for charge trapping ($0 < \beta \leq 1$), • is the relaxation time, and $I_{DS}(0)$ is the initial maximum drain-source current measured at the beginning of stressing. Although this model was originally

developed to describe the bias-stress effect in amorphous silicon transistors considering the time-dependent evolution of trap states due to hydrogen migration, we employ similar formalism to describe dispersive trapping process in OFETs. A stretched exponential function (eqn. 2) provides a perfect fit to the data in both n-channel and p-channel systems. **Fig.6(**a-b), shows the data points (symbols) as well as fitted line using eqn. 2. The values of • at room temperature, extracted from the fitting are 4.28×10^5 s and 1.58×10^5 s in n-channel and p-channel device, respectively. The corresponding exponent values are β=0.57 and 0.67, respectively. The large • values imply a long term stability of the device, which is very much desirable for practical applications. Considering that the interfacial chemistry at the heterojunction remains identical, the bias stress effect is primarily attributed to structural defects at the $SnCl_2Pc$/CuPc interface, which may generate deep traps for electron in the n-channel. It has been proposed that the time-dependent charge trapping in deep traps is responsible for the bias stress effect in OFETs and thus, charge traps at organic heterojunction can be the source of the small bias-stress instability in the n-channel device.[45]

As for the bias stress effect in the p-channel device shown in Fig.7(b), it has less dependence on the $SnCl_2Pc$/CuPc heterointerface, since the p-channel is close to the CuPc/PMMA dielectric interface rather than to the $SnCl_2Pc$/CuPc heterointerface. Therefore, both the organic/dielectric and organic/organic interfaces influence the bias stress effect in bilayer ambipolar OFETs.[1, 45]

To study the influence of gate bias on the cyclic bias stress behavior, we measured the drain-source current, I_{DS} of bilayer ambipolar OFET applying gate-source voltage V_{DS} = 6 V while changing V_{GS} = 6V for "ON" state (for 180 s) and V_{GS}= 0 V for "OFF" state (for 180 s). It is plotted as function of time in **Fig.7(**c). During the "OFF" state, the drain current slowly

decreases with time and in the "ON" state it sharply raises to its maximum value. It is noticeable from Fig.7(c) that negligible decay of maximum drain current ("ON" state) occurs after repeated "ON" and "OFF" states during 3600 s of operation at room temperature under low vacuum. The time constant for decay of current during "OFF" state is ~333 s. We acquired the transconductance curves before and after cyclic bias stress of 1 hr for both channels and it shows no shift of threshold voltage (Fig.S3, in supporting information) after the bias stress. Thus, the devices are very stable under low vacuum conditions.

3. Conclusion

In conclusion, we have demonstrated an ambipolar OFET based on low band gap $SnCl_2Pc$ and CuPc small molecules heterojunction that exhibits ambipolar conduction depending on the applied gate bias, either an accumulation layer of holes (negative gate bias) is formed in the CuPc layer or an accumulation layer of electrons (positive gate bias) is formed in the $SnCl_2Pc$ layer of the heterostructure device. The change in operation mode was attributed to the proper choice of organic/organic heterojunction and contact electrode metal work function. The change in layer thickness resulted in evolution of the field-effect mobility values and an optimized thickness $SnCl_2Pc$/CuPc heterostructure yielded balanced carrier mobility (~10^{-4} cm^2 V^{-1} s^{-1}). The bias stress effect and contact behavior in the bilayer ambipolar OFETs have been investigated. For the top $SnCl_2Pc$ n-channel, a smooth and continuous organic heterojunction enabled not only high bias stress stability (τ ~10^5 s) but also optimal contact resistance (R_C) for efficient carrier injection. For the bottom CuPc p-channel, the hole injection may be realized by the Ag penetration into $SnCl_2Pc$ to form local direct contact to CuPc, and the bias stress stability is dependent on the CuPc/dielectric interface rather than on the organic heterojunction. Using

low work function Ag as a top contacts and a hydroxyl-free PMMA gate dielectric, the electron injection is greatly enhanced, leading to an improvement of both the electron and hole currents at saturation region. We believe that the present results are significant to develop further understanding on the carrier transportation process in organic-organic (p-n) heterojunction, and will be helpful to develop the fabrication of stable ambipolar OFETs, which will be superior candidate for organic complementary circuits, organic light emitting field-effect transistors and organic lasers.

4. Experimental Section

Materials: Tin (IV) phthalocyanine dichloride ($SnCl_2Pc$) ($C_{32}H_{16}Cl_2N_8Sn$) and copper phthalocyanine (CuPc) ($C_{32}H_{16}CuN_8$) served as organic semiconductor in all devices are purchased from Alfa Aesar, UK. Poly (methyl methacrylate) (Alfa Aesar, PMMA, M_w~550000 kg/mol, 25 mg/ml in anisole) was used as polymer gate dielectric. A silver (Ag) wire (Alfa Aesar, 97%) is used for evaporation of source/drain (*S/D*) contacts. All materials were used as received without any further purification.

Heterostructure Device Fabrication:

To form the control gate, about 150 nm thick layer of aluminum (Al) (Alfa Aesar, 99.9% pure) was vacuum deposited at a rate 30 $Å s^{-1}$ on to clean glass substrates. The Al layer is anodized by immersing in citric acid solution prepared with ultra-pure (18.2 MΩ cm) de-ionized water as a solvent, $1mML^{-1}$. A constant current density of 0.3 mA cm^{-2} is maintained until the voltage reaches 10 V, and the voltage is then maintained at 10 V until the current density drops to 0.015 mA cm^{-2}. The thickness of the Al_2O_3 is estimated to be 13 nm, given the anodization ratio (c_{Al}

≈1.3 nm/V).[27] A thin buffer layer of PMMA was coated at 5000 rpm for 60s to deposit a very thin and uniform layer on Al_2O_3 surface and annealed at 80°C for 30 minutes under low vacuum to remove residual solvents. The morphological analysis is carried out with an AFM (Agilent-5500) in the tapping mode. Fig. S4(a) shows the AFM image of PMMA deposited on Al_2O_3/Al/glass substrate. PMMA can provide a high-quality hydroxyl free interface to the organic semiconductor with high dielectric breakdown strength (~1 MV/cm). The optimized thickness of PMMA layer was 100 nm, as measured by surface profilometer (Veeco Dektak-150). The root-mean-square (RMS) roughness (R_q) of PMMA is 0.231 nm as measured from AFM, which is much lower than the thickness of the anodized Al_2O_3 layer (≈5 nm). A 60-nm-thick $SnCl_2Pc$ film was deposited on CuPc layer (of different thicknesses) on to the PMMA/Al_2O_3 dielectrics under identical conditions at a rate 0.8 Å/s using thermal evaporation at a base pressure ~10^{-6} mbar. The substrate temperature was kept at 60 °C during all depositions. Finally, using a thermal vacuum deposition chamber, a >50 nm silver (Ag) top electrode drain/source (*S/D*) were deposited and patterned through a shadow mask on substrate to complete the device structure, where the device channel length (L) and channel width (W) are defined as 30 μm and 780 μm, respectively. The surface morphology of the organic thin films was characterized in ambient condition by AFM in tapping mode.

Device Characterization:

We fabricated $SnCl_2Pc$ top-contact OFETs on PMMA/Al_2O_3 substrate. The capacitance density C_i (nF/cm^2) was measured from a metal-insulator-metal structure of parallel plate capacitor with different contact areas. The buffer layer PMMA on Al_2O_3 gives the capacitance density C_i ~ 31 nF cm^{-2}. The leakage current density, J (A/cm^2) through the gate dielectrics was very small (~10^{-}

^{7} A/cm^{2}) [see Fig. S4(b), supporting information]. The electrical characteristics including the voltage-current relationship and capacitance are measured with a Keithley 4200-SCS system at room temperature in a probe station (Lake shore, USA) under low vacuum (~10^{-3} mbar). The field-effect mobility (μ_{FE}) was calculated in the saturation regime using equation, $|I_{DS}| = (WC_i/2L)\mu_e(V_{GS} - V_{Th,e})^2$ and $|I_{DS}| = (WC_i/2L)\mu_h [V_{DS} - (V_{GS} - V_{Th,e})]^2$ for electron and hole transport, respectively (where W is the channel width (780 μm) and L is the channel length (30 μm), C_i is the capacitance of PMMA/Al_2O_3 gate dielectrics (~ 31 nF cm^{-2}).

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Table1. TC/BG OFET (Ag-contact) electrical parameters for $SnCl_2Pc$/CuPc heterostructure with different CuPc thicknesses grown at substrate temperature 60 ºC.

$SnCl_2Pc$-thickness[a] [nm]	CuPc-thickness[b] [nm]	n-channel OFET			p-channel OFET		
		μ_e [$cm^2 V^{-1}s^{-1}$]	$V_{Th,e}$ [V]	$R_{c,e}$ [$\times 10^9$ Ω-cm]	μ_h [$cm^2 V^{-1}s^{-1}$]	$V_{Th,h}$ [V]	$R_{c,h}$ [$\times 10^9$ Ω-cm]
60	4	1.8×10^{-4}	2.53	1.60	2.1×10^{-4}	-6.84	7.19
	12	2.4×10^{-4}	4.22	15.6	1.2×10^{-3}	-2.88	9.78
	16	1.4×10^{-4}	3.40	115.15	4.2×10^{-4}	-3.41	10.70

a) active layer (n-channel), b) active layer (p-channel)

Figures with captions:

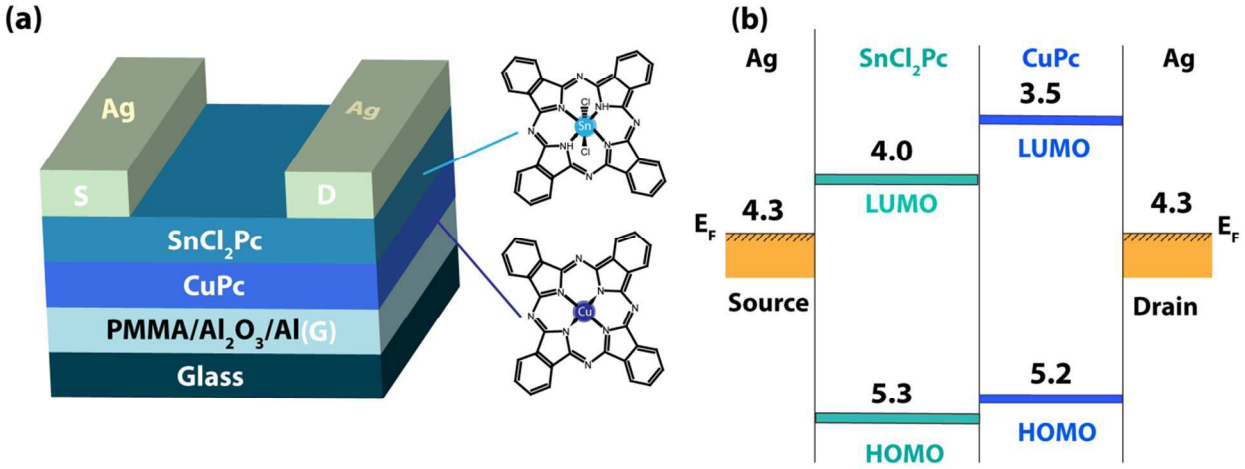

Fig.1 (a) Schematic of the top-contact (Ag) bottom-gate (Al) device configuration employed in this study, with chemical structures of the small molecules $SnCl_2Pc$ and CuPc. (b) Schematic of the energy band diagram of $SnCl_2Pc$/CuPc heterostructures with Ag electrodes without any external bias.

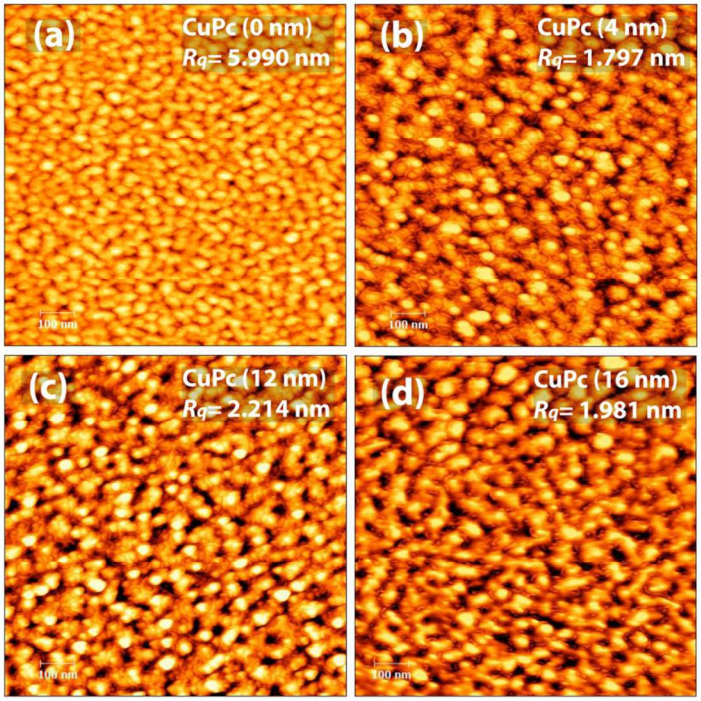

Fig. 2. Tapping-mode AFM images (1 μm × 1 μm) of 60-nm-thick $SnCl_2Pc$ layer grown on CuPc bottom layer of differnt thicknesses: (a) 0 nm, (b) 4 nm, (c) 12 nm, and (d) 16 nm. The measured RMS roughness (R_q) of the $SnCl_2Pc$ surface is indicated in each case.

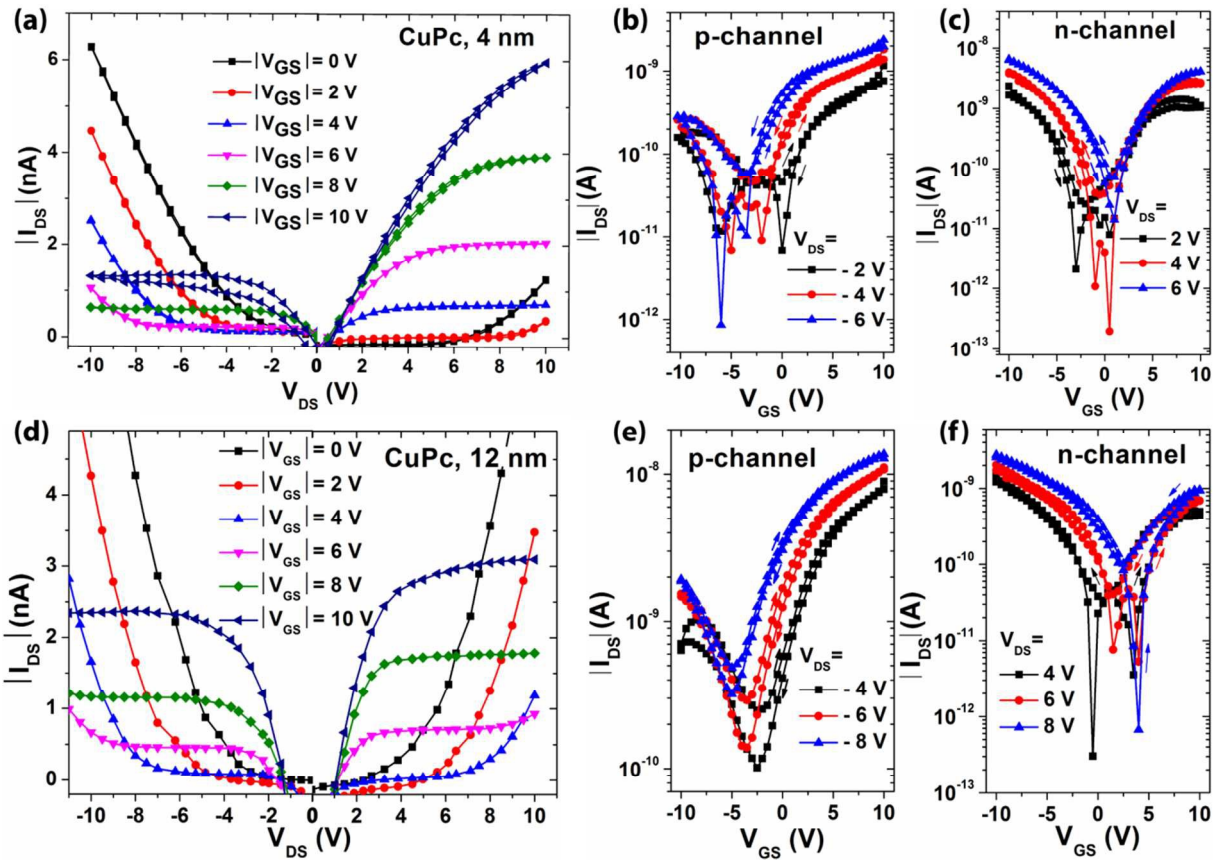

Fig. 3. (a) Typical output characteristics (I_{DS}-V_{DS}) and (b)-(c) transfer characteristics (I_{DS}-V_{GS}) (for p-channel and n-channel, respectively) of the heterostructure ambipolar OFET for CuPc thickness of 4 nm. (d) Output characteristics (I_{DS}-V_{DS}) and (e)-(f) transfer characteristics (I_{DS}-V_{GS}) (for p-channel and n-channel, respectively) of the heterostructure ambipolar OFET for CuPc thickness 12 nm. Note that the thickness of top $SnCl_2Pc$ layer was kept constant (60 nm) for both cases.

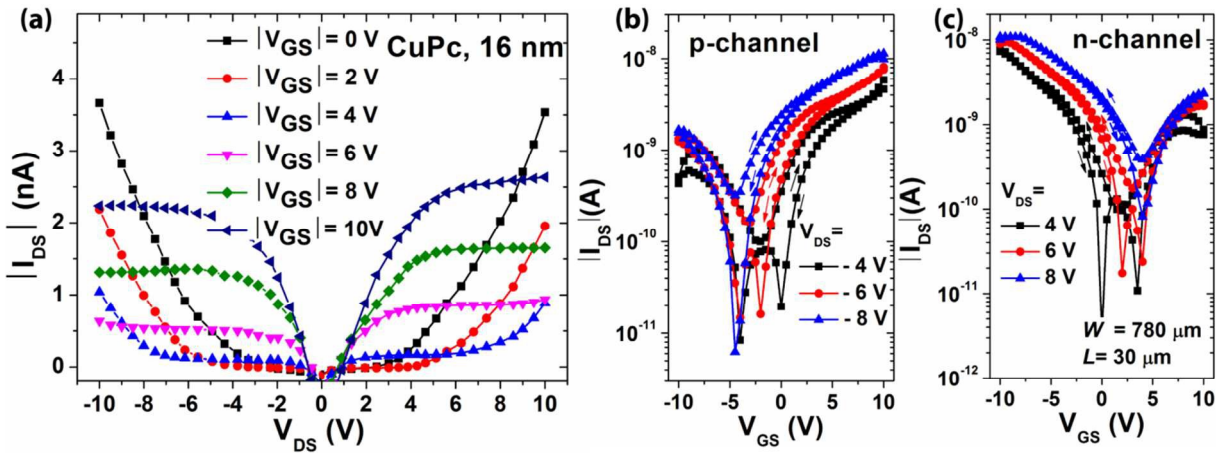

Fig. 4. (a) Typical output characteristics (I_{DS} - V_{DS}) and (b)-(c) transfer characteristics (I_{DS}-V_{GS}) (for p-channel and n-channel, respectively) of the heterostructure ambipolar OFET for CuPc thickness 16 nm, whlie the thickness of top $SnCl_2Pc$ layer was 60 nm.

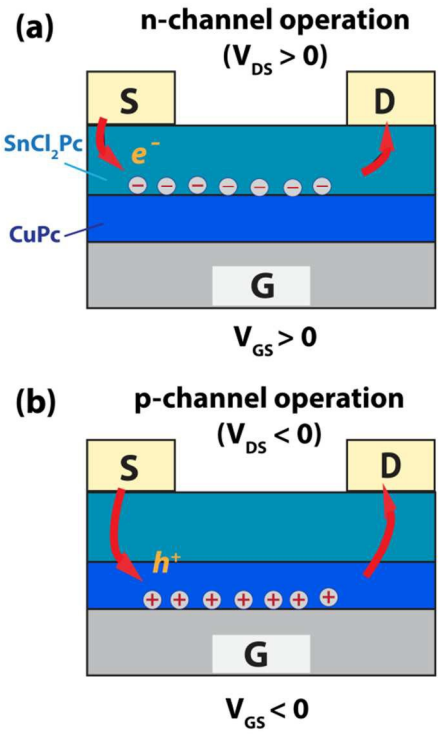

Fig. 5. Schematic of conduction process in TC-BG $SnCl_2Pc$/CuPc heterostructure transistor for (a) n-channel, (b) p-channel operations under different bias conditions. Flow of electrons and holes are indicated with arrow in respective cases.

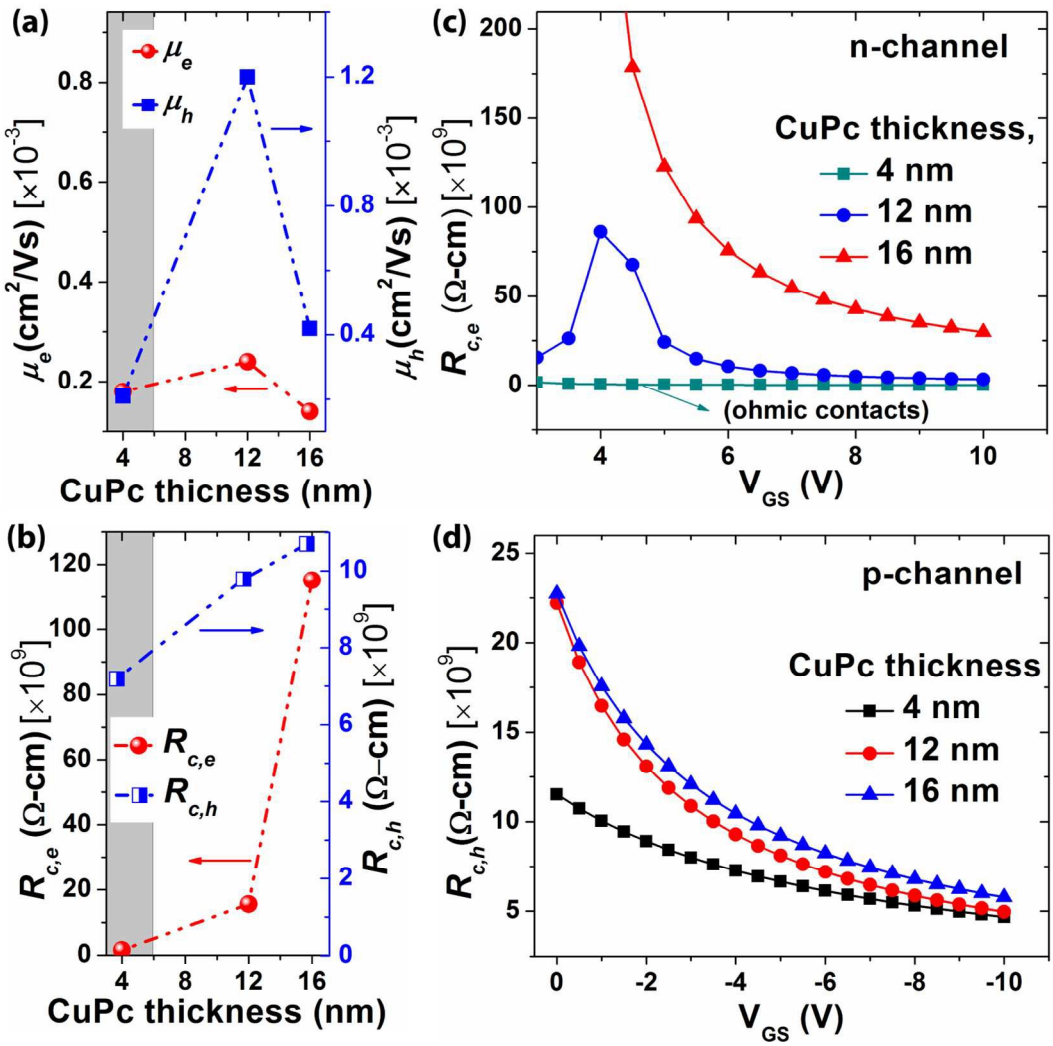

Fig. 6. (a) Electron (μ_e), and hole-mobility (μ_h) in $SnCl_2Pc$/CuPc bilayer heterostructure OFETs using Ag electrodes as a function of thickness of CuPc bottom layer with a fixed thickness (60 nm) of $SnCl_2Pc$ top layer. (b) Contact resistance for n-channel region ($R_{c,e}$) and p-channel region ($R_{c,h}$) of the corresponding devices extracted from from the Y-function method. (c)- (d) Gate bias dependence of channel width normalized contact resistance for the TC-BG devices based on $SnCl_2Pc$ (60 nm)/CuPc (x nm, x = 4, 12 and 16) for n-channel and p-channel region, respectively.

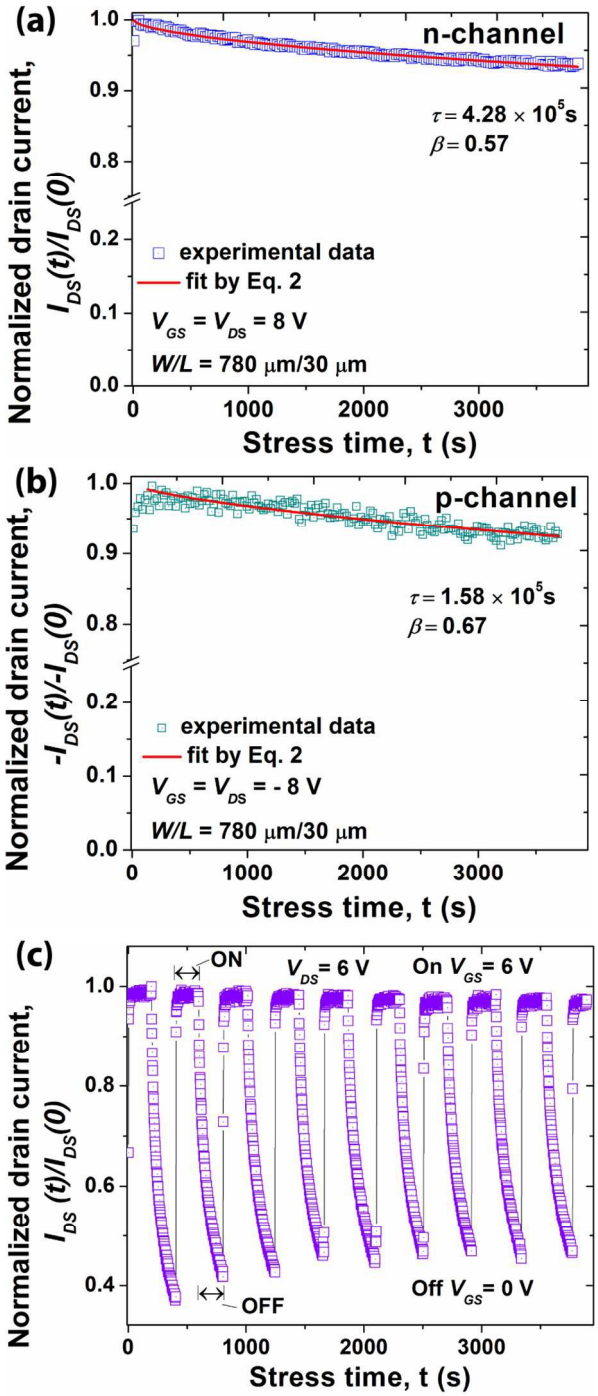

Fig. 7. (a)-(b) Normalized drain-source current decay $I_{DS}(t)/I_{DS}(0)$ as a function of time in n-channel ($SnCl_2Pc$=60nm) at electron accumulation state and $I_{DS}(t)/I_{DS}(0)$ in p-channel (CuPc=4nm) at hole accumulation state. (c) Cyclic stability with the "ON" and "OFF" cycles up to 3600 s for TC-BG heterostructure ambipolar OFET device based on $SnCl_2Pc$ (60 nm)/CuPc (4 nm).

TOC Abastract:

Low operating voltage (~10 V) top contact-bottom gate ambipolar organic field-effect transistors (OFET) fabricated with vacuum-deposited small molecules, $SnCl_2Pc$ and CuPc. The ambipolar OFET exhibits balance carrier mobility and low bias-stress (characteristics time constant ~10^5 s) for both n-channel and p-channels. It also shows negligible decay of drain-source current during cyclic bias stress for 1 hour.

TOC image: