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Nanoscale CuO Solid-electrolyte-based Conductive-bridging-random-access-memory Cell Operating Multi-level-cell and 1Selector1Resistor

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Nanoscale (~28 nm) non-volatile multi-level conductive-bridging-random-access-memory (CBRAM) cells are developed by using a CuO solid-electrolyte, providing a Vset of ~0.96 V, a Vreset of ~-1.5 V, a ~1×10^2 memory margin, ~3×10^6 write/erase endurance cycles with 100-µs AC pulse, ~6.63-years retention time at 85 °C, ~100 ns writing speed, and multi-level (four-level) cell operation. Their non-volatile memory cell performance characteristics are intensively determined by studying material properties such as crystallinity and poly grain size of the CuO solid-electrolyte and are found to be independent of nanoscale memory cell size. In particular, the CuO solid-electrolyte-based CBRAM cell vertically connecting with p/n/p-type oxide (CuO/IGZO/CuO) selector shows the operation of 1S(selector)1R(resistor), demonstrating a possibility of cross-bar memory-cell array for realizing terabit-integration non-volatile memory cells.

1. Introduction

Recently, resistive random access memories (ReRAMs) have been intensively researched to replace current NAND flash memory because of their non-volatile memory characteristic, minimum $4F^2$ memory cell size, large memory margin of more than 10^2, and fast write/erase speed of less than several hundred nanoseconds (ns). Particularly widespread research attention has been received by transition metal oxide (TMO)-based ReRAMs, which are classified by oxygen-vacancy-filament[1-6] or interface-type.[7-12] Although TMO-based ReRAMs have demonstrated good non-volatile memory cell performance characteristics such as 10 years retention time, 10^6 write/erase endurance cycles, and ~100 ns writing speed,[13, 14] the overall performance has shown a strong dependency on memory cell size; i.e., it rapidly degrades when the memory cell size is decreased since the oxygen vacancy amount or the interface area greatly decreased when the memory-cell size is decreased. [15-25] Otherwise, conductive bridging random access memory (CBRAM) cell has been considered as an alternative to TMO-based ReRAM since CBRAM cells showed less dependency of non-volatile memory performance on the memory cell size than that of TMO-based ReRAMs. [26, 27]

A CBRAM cell with a top metal electrode/ solid or polymer electrolyte/ bottom inert metal electrode structure is operated by switching nanoscale metal filaments in the solid or polymer electrolyte.[28, 29] The materials used for top electrodes supplying metal ions to form metal filaments have been Cu,[30-34] CuTe,[35] and Ag.[28, 36-38] The electrolyte materials that have been used are Al_2O_3,[30, 31, 35] a-Si,[36, 37] Ag-Ge-S,[38] Cu_2S,[32, 33] TaO_x,[33] and polymer.[34, 39] The materials used for inert bottom electrodes not supplying metal ions have been Pt[28, 32, 33] and TiN.[30] Although these CBRAMs showed a bipolar switching behavior at nanoscale cell size, fast writing (or set) speed, or multi-level-cell (MLC) operation for 1-transistor and 1-resistor (1T1R),[31] their non-volatile memory characteristics such as retention time and write/erase endurance cycles were not sufficient for a commercial non-volatile memory cell.[30, 33, 36, 38]

In particular, it have not yet been reported that a CBRAM cell satisfies non-volatile memory characteristics for terabit-integration such as sub-30nm cell size, ~ ns writing speed, MLC operation, retention time of > 10 year, write/erase endurance cycles of > 10^6, and cell-size scaling-down immunity. Furthermore, a CBRAM cell fabricated with 1T1R structure would not be a proper for realizing a terabit-integration non-volatile memory-cell, since its cell size is greater than $4F^2$ where F is the minimum feature size of a memory cell. Thus, a CBRAM cell fabricated with 1-selector (p/n/p-type oxide selector or ovonic threshold switch) and 1-resistor structure (1S1R) would be essentially developed, since its cell size is $4F^2$.[40]

To address these issues, we developed a CuO solid-electrolyte-based CBRAM demonstrating excellent non-volatile memory performance, multi-level-cell operation, and fast writing (set) speed of ~100 ns. In the work reported in this paper, we thoroughly investigated the CBRAM's multi-level non-volatile memory cell performance characteristics, i.e., bipolar current (*I*) vs. voltage (*V*) curve, retention time, write(set)/erase(reset)

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endurance cycles, multi-level-cell operation, and writing (set) speed. In addition, we tested the performance's dependency on nanoscale memory cell size and a possibility of 1S1R operation. Finally, we reviewed in detail the mechanism by which the CBRAM performs bipolar switching.

2. Results and discussion

2.1. Dependency of crystalline structure and electrical properties on N_2 post-annealing temperature for CuO solid-electrolyte

In our experiments, we used a CuO (cupric oxide) or Cu_2O (cuprous oxide) solid-electrolyte for the nanoscale CBRAM cells. It has been reported that a CuO solid-electrolyte has a monoclinic crystalline structure and a 1.0 ~2.1 eV energy band gap while a Cu_2O electrolyte has a cubic crystalline structure and a 2.1 ~ 2.6 eV energy band gap.[41-43] Both CuO and Cu_2O are known as transparent p-type semiconductors, producing negatively charged Cu vacancies (V_{cu}^{2-}) having an acceptor energy level of ~ 0.3 eV above the valance energy band.[42] In particular, the presence of V_{cu}^{2-} produces Ag filaments in the CuO or Cu_2O solid-electrolyte via the ionic conduction process as a positive bias is applied between the top Ag electrode and bottom inert TiN electrode, called a set process (program). Conversely, it breaks Ag filaments in the CuO or Cu_2O solid-electrolyte via the ionic conduction process as a negative bias is applied between the Top Ag electrode and bottom TiN electrodes, called a reset process (erase).

To confirm the crystalline structure of CuO and Cu_2O solid-electrolytes, 70-nm thick CuO and Cu_2O solid-electrolytes were characterized by X-ray diffraction (XRD). The as-sputtered CuO and Cu_2O solid-electrolytes were subjected to N_2 annealing at 250, 300, 400, and 500 °C for 30 min. The CuO solid-electrolyte showed XRD peaks at $[\bar{1}11]$ and [111] with 2 theta (2θ) of ~35.6 and ~38.8 (JCDPS card number: 03-6433) regardless of annealing temperature, which is a typical crystalline structure of monoclinic CuO, as shown in Fig. 1a.[44-46] In addition, the XRD peak intensity at $[\bar{1}11]$ was higher than that at [111] for all N_2 post-annealing temperatures. In contrast, the Cu_2O solid-electrolyte exhibited the XRD peak only at [111] with 2θ of ~36.7 (JCDPS card number: 08-8215) at the annealing temperature of 250 °C, which is a typical crystalline structure of cubic Cu_2O, as shown Fig. 1b. At N_2 post-annealing temperatures above 300 °C, however, the crystalline structure of the Cu_2O solid-electrolyte was converted to that of monoclinic CuO, presenting XRD peaks at $[\bar{1}11]$ and [111] with 2θ of ~35.8 and ~38.8 (JCDPS card number: 03-6433), as shown in Fig. 1b.[44-46] In addition, the XRD peak intensity at $[\bar{1}11]$ was similar to that at [111] for all N_2 post-annealing temperatures above 300 °C. The XRD peak ratio of $[\bar{1}11]$ to [111] was higher for the CuO solid-electrolyte than for the Cu_2O solid-electrolyte.

To understand how the crystalline structures of the CuO and Cu_2O solid-electrolytes influence the electrical properties, the solid-electrolyte's resistance was estimated as a function of

the N_2 post-annealing temperature, as shown in Fig. 1c. Note that the CuO and Cu_2O solid-electrolyte films inserted between the top and bottom Pt electrodes were subjected to an N_2 post-annealing annealing and then their resistance values were estimated by using a four-point probe. For both electrolytes, the resistance decreased with an increase in the N_2 post-annealing temperature. In addition, the CuO solid-electrolyte had 10^2~10^3 times lower resistance than that of the Cu_2O solid-electrolyte. To ascertain the resistance dependency on the N_2 post-annealing temperature, we estimated the dependency of the average poly grain size of the solid-electrolytes on the N_2 post-annealing temperature. Note that the average size was obtained from XRD measurement and calculation by Scherrer equation.[44, 46] The average size of the CuO solid-electrolyte increased from 16.03 to 18.13 nm when the N_2 post-annealing temperature was increased from 250 to 500 °C, which was well correlated with the dependency of the CuO electrolyte resistance on the N_2 post-annealing temperature; i.e., a lager poly-grain size led to a lower resistance. However, the average grain size of the Cu_2O solid-electrolyte rapidly decreased from ~16.73 to 14.03 when the N_2 post-annealing temperature was elevated from 250 to 300 °C, since the crystalline structure of the Cu_2O solid-electrolyte was converted to that of the CuO electrolyte, compare Fig. 1b with Fig. 1c. Then, it increased from 14.03 to 16.19 nm when the N_2 post-annealing temperature was increased from 300 to 500 °C, which was also well correlated with the dependency of the CuO electrolyte resistance on the N_2 post-annealing temperature. Since the CuO solid-electrolyte had larger average grain size than the Cu_2O solid-electrolyte, the former's resistance was lower than the latter's, which correlated well with the former's having a higher XRD peak ratio of $[\bar{1}11]$ to [111]. Thus, both electrolytes' resistance was well correlated with the crystalline structure and the average grain size of a solid-electrolyte.

2.2. Nanoscale (~19 nm in diameter) Ag filament in the Cu_2O solid-electrolyte-based CBRAM cell

The Cu_2O solid-electrolyte-based CBRAM cell was fabricated with the device structure of the bottom line shaped Pt electrode with ~28 nm width, a ~25-nm thick Cu_2O solid-electrolyte, a ~200-nm thick top Ag electrode, as shown in Fig. 2a. After a program (set) of 1.0 V for 60 ms, the memory-cell's cross-sectional TEM image and Energy-dispersive X-ray spectroscopy (EDS) analysis were performed. The shape of an Ag filament in the Cu_2O solid-electrolyte looked like an inversely conical,[47-49] indicating that the Ag filament in the Cu_2O solid-electrolyte would be formed by Ag diffusion and drift following reduction process mechanism,[30, 50-55] as shown in Fig. 2b. The size of an Ag filament in the Cu_2O solid-electrolyte was 19 nm in diameter, implying that this CBRAM cell would be independent of the scaling-down of the memory cell size. The map of Ag ions for the cross-sectional Cu_2O based CBRAM cell analysed by EDS explained that an Ag filament in the Cu_2O solid-electrolyte was formed by the

diffusion of Ag ions from the top Ag electrode and the drift following reduction process of Ag ions via Cu vacancies (V_{cu}^{2-}) in the Cu_2O solid-electrolyte when the positive bias was applied to the top Ag electrode, as shown in Fig. 2c. In addition, the map of Pt ions for the cross-sectional Cu_2O based CBRAM cell showed that there was no diffusion of Pt ions in the Cu_2O solid-electrolyte when the negative bias was applied to the bottom Pt electrode, confirming the program (set) mechanism via Ag filament formation in a CBRAM cell, as shown in Fig. 2d.

2.3. Non-volatile memory cell characteristics for the CuO solid-electrolyte-based CBRAM cells

The CuO solid-electrolyte-based CBRAM cells were fabricated with the device structure of the bottom cylindrical shaped TiN electrodes with ~28 nm diameter, a ~25-nm thick CuO solid-electrolyte, a ~200-nm thick top Ag electrode, and a ~20-nm thick TiN capping layer, as shown in Fig. 3a and 3b. The solid-electrolyte, Ag electrode, and TiN capping layer were ~60 um in diameter. The bottom cylindrical shaped TiN electrodes with cell-size of ranging 28 nm to ~2 um were well isolated from each other with SiO_2 film. Note that the non-volatile memory performance of these CBRAM cells greatly depended on the CuO solid-electrolyte thickness; i.e., the best non-volatile memory performance was obtained a specific CuO solid-electrolyte thickness (~25nm), see Fig. S1. A CuO solid-electrolyte-based CBRAM cell showed a typical bipolar bi-stable current (I) vs. voltage (V) curve when the top electrode is only used by Ag and a positive bias is applied to the top Ag electrode for the forming process of Ag filaments in the CuO solid-electrolyte (see Figs. S2 and S3), as shown in Fig. 3c. The current gradually reached a compliance level (~10^{-3} A) when a positive bias was applied from 0 to 1.5 V, called a set (or write) process, at ~0.96 V, implying Ag bridging filaments were formed by moving Ag ions toward the bottom TiN electrode. Then, the current rapidly reduced from the compliance level to 0 A when the bias was applied from 1.5 to 0 V, called a low resistance state (LRS), where the LRS could be read at a ~0.1 V reading voltage after applying a set voltage (V_{set}: ~0.96 V). Afterward, the current rapidly increased and then slightly decreased when the bias was applied from 0 to V_{NDR} (~-0.4) and V_{reset} (~-1.5 V), showing a negative differential resistance (NDR) region and called a reset (or erase) process at reset voltage (V_{reset}: ~-1.5 V), implying the Ag-ion bridging filaments were broken by moving Ag ions toward the top Ag electrode. Then, the current gradually decreased as the bias was applied from -1.5 to 0 V, where the high resistance state (HRS) could be read at a ~0.1 V reading voltage after applying a reset voltage (V_{reset}: ~-1.5 V). Thus, the CBRAM cell in Fig. 3a demonstrates a bipolar type ReRAM. Since the shape of Ag-ion bridging filaments is intensively determined by the set voltage pulse (set time), we investigated the V_{set} dependency on pulse width (writing speed), as shown in Fig. 3d. The set time exponentially decreased with an increase in the set voltage. In particular, the set voltage increased linearly from ~0.96 V (at 60 ms set time) to 1.45 V (at 100 ns set time), and 1.51 V (at 10

ns set time). Surprisingly, the CuO solid-electrolyte-based CBRAM cell could write (set) at a set voltage of less than ~1.5 V with a set time of several tens of ns. The consumption energy for set process was ~145 pJ at the 100-ns pulse width, the 1-mA set current, and the 1.45-V set voltage from Fig. 4d. In addition, the CuO solid-electrolyte-based CBRAM cell presented ~10^5 AC set/reset endurance cycles with 100-μs AC pulse width by sustaining a 1.27×10^2 memory margin (Ion/Ioff), as shown in Fig. 3e. To improve the AC set/reset endurance cycles, we inserted the TiN diffusion barrier of 0.1 nm between the CuO solid-electrolyte and the top Ag electrode, resulting in ~3×10^6 AC set/reset endurance cycles by with 100-μs AC pulse width by sustaining a 1.31×10^2 memory margin (I_{on}/I_{off}), as shown in Fig. 3e. Note that the TiN diffusion barrier plays a role of controlling the formation of Ag filaments in CuO solid-electrolyte via adjusting the diffusion amount of Ag ions from Ag electrode after a N_2 annealing. In particular, it was found that there was a specific TiN diffusion barrier thickness to achieve the highest set/reset endurance cycles; i.e., ~3×10^6 cycles at 0.1 nm. Furthermore, it demonstrated ~6.63-years retention time at 85 °C by sustaining a 3.63×10^2 memory margin (I_{on}/I_{off}), as shown in Fig. 3f. The endurance-cycle and retention-time results indicated that the CuO solid-electrolyte-based CBRAM cell could be a terabit-level non-volatile memory cell. In summary, the CuO solid-electrolyte-based CBRAM cell with ~28-nm hole diameter demonstrated the non-volatile memory characteristics having V_{set} of ~0.96 V, V_{reset} of ~-1.5 V, ~3×10^6 AC set/reset endurance cycles with 100-μs AC pulse width by sustaining a 1.31×10^2 memory margin (I_{on}/I_{off}), and ~6.63-years retention time at 85 °C by sustaining a 3.63×10^2 memory margin (I_{on}/I_{off}), which satisfy terabit-integration non-volatile memory-cell characteristics.

Dependency of bi-stable I-V characteristic on nanoscale memory cell size for the CuO solid-electrolyte-based CBRAM cells: We investigated the dependencies of bipolar bi-stable I-V curves on the N_2 annealing temperature and memory cell size for the CuO solid-electrolyte-based CBRAM cells; the results are shown in Fig. 4a, b, and c. In the N_2 post-annealing at 250 °C, memory cells of three different sizes (34, 56, and 113 nm) showed an insulator characteristic, as shown in Fig. 4a. In the N_2 post-annealing at 400 °C, the 113-nm cell showed a bi-stable I-V curve having a ~2.67×10^2 memory margin (Ion/Ioff), which slightly increased current and rapidly reached a compliance current (CC) level (~10^{-3} A) at V_{set} (~1.1 V) when a positive bias was applied and showed a NDR region when a negative bias was applied, as shown in Fig. 4b. However, the 56-nm cell exhibited only a resistance characteristic while the 34-nm one showed an insulator characteristic. Note that the N_2 post-annealing the CuO solid-electrolyte at 400 °C or less could not sufficiently supply V_{cu}^{2-} and thus could not achieve a bipolar bi-stable I-V curve, as shown in Fig. 4a-b. In the N_2 post-annealing at 500 °C, the memory cells for all diameters (34, 56, and 113 nm) presented a bi-stable I-V curve having a ~3.06×10^2 memory margin (Ion/Ioff) and showing no dependency on memory cell size. This curve gradually increased current when the positive bias was applied and presented a NDR region, as

shown in Fig. 4c. These results imply that the N_2 post-annealing the CuO solid-electrolyte at 500 °C produced sufficiently negatively charged copper vacancies (V_{cu}^{2-}) so that enough Ag-ion bridging filaments were formed to reach a CC level as a positive bias was applied. It should be noted that the N_2 post-annealing at 500 °C not only sufficiently produced V_{cu}^{2-} but also enhanced the Ag ion diffusion into the switching layer, see Fig. S4. In addition, the filaments in these CuO-based CBRAM cells for all memory-cell size could be easily produced and the conduction current level were limited by a limited current level (the CC level) so that the bipolar bi-stable I-V curves of these CBRAM cells showed independency of the memory-cell size, which would be a strong merit of this CBRAM cell, as shown in Fig. 4c. Bear in mind that ReRAM cells are strongly dependent the memory cell size.[15-25] We next investigated the dependencies of bipolar bi-stable I-V curves on N_2 post-annealing temperature and memory cell size for the Cu_2O solid-electrolyte-based CBRAM cells; the results are given in Fig. 4d-f. In the N_2 post-annealing at 250 °C, the memory cells for all sizes (34, 56, and 113 nm) showed an insulator characteristic like the CuO solid-electrolyte, as shown in Fig. 4d. In the N_2 post-annealing at 400 °C, the 113-nm cell showed a bipolar bi-stable I-V curve having a ~1.45 × 10^3 memory margin, which slightly increased current and rapidly reached a CC level at a 10^{-3} A at V_{set} (~1.05V) when the positive bias was applied. In addition, it slightly decreased current and then rapidly decreased at ~4.26 × 10^{-6} A at V_{reset} (~-1.5 V) like a typical ReRAM cell (no NDR region) when the negative bias was applied, as shown in Fig. 4e. In particular, the bipolar bi-stable I-V curve for the Cu_2O solid-electrolyte-based CBRAM cell was different from that for the CuO solid-electrolyte-based CBRAM, as compared Fig. 4b with 4e. However, the 56-nm cell exhibited only a resistance characteristic while the 34-nm one showed an insulator characteristic similar to that for the CuO solid-electrolyte based CBRAM cell that was N_2-annealed at 400 °C. In the N_2 annealing at 500 °C, the 113-nm cell showed a bipolar bistable I-V curve having a ~4.74 × 10^3 memory margin, ~1.24 V V_{set}, and -1.06 V V_{reset}, which slightly increased current and rapidly reached a CC level (~ 10^3 A) at V_{set} when the positive bias was applied and rapidly decreased current (2.52 × 10^{-6} A) at V_{reset} when the negative bias was applied, as shown in Fig. 4f. The 56-nm cell showed a bipolar bi-stable I-V curve having a ~5.28 × 10^4 memory margin, V_{set} of ~1.62 V and V_{reset} of ~-0.62 V. However, the V_{set} (~1.62 V) for the 56-nm cell was higher than that (~1.24 V) for the 113-nm cell. In addition, the high-resistance state (HRS) (1.24 × 10^{-8} A) for the 56-nm cell was lower than that (2.11 × 10^{-7} A) for 113-nm cell, which is like a typical bipolar bi-stable I-V curve depending on the memory cell size for a ReRAM cell operated by oxygen-vacancy-filament or interface-type. However, the 34-nm showed a resistance characteristic since the concentration of negatively charged Cu vacancies in the Cu_2O solid electrolyte was probably not enough for producing Ag filaments in the switching layer compared to the CuO solid-electrolyte, as discussed in Fig.1c. Thus, the bipolar bi-stable I-V curve of Cu_2O solid-electrolyte-based cells is strongly dependent on the memory cell size. We next investigated in detail the

dependency of bipolar bi-stable I-V curves on the memory cell size for the CuO solid-electrolyte-based CBRAM cells. Almost the same I-V curves were obtained although the memory cell size was increased from 34 to 1414 nm, as shown Fig. 5a. Thus, V_{set}, HRS, and low-resistance state (LRS) were sustained at ~0.8 V, ~5 × 10^{-7} A, and 2 × 10^{-4} A, respectively, although the memory cell diameter was increased from 34 to 1414 nm, as shown in Fig. 5b. In summary, the non-volatile memory characteristic (bipolar bi-stable I-V curve) for the CuO solid-electrolyte-based CBRAM cells N_2-post-annealed at 500 °C showed no dependency on the nanoscale memory cell size, while that for the Cu_2O solid-electrolyte-based CBRAM cells N_2-post-annealed at 500 °C exhibited a strong dependency on the cell size. These results indicate that the CuO solid-electrolyte-based CBRAM cells would be good nanoscale non-volatile memory cells if their diameters were scaled down to less than 20 nm.

2.4. Non-volatile memory cell characteristics for the CuO solid-electrolyte-based CBRAM cells connected with a p/n/p-type oxide selector (1S1R)

A nanoscale (~28 nm) CuO solid-electrolyte-based CBRAM was connected with a micro-scale (~100 um) p/n/p-type oxide selector, called 1S1R, as shown in Fig. 6a. A p/n/p-type oxide selector (1S) was fabricated with a vertical stacking structure of p-type cobalt-oxide (CoO)/n-type indium-gallium-zinc oxide (IGZO)/ p-type cobalt-oxide (CoO). I-V curves of 1S (p/n/p-type oxide selector) and 1R (CuO solid-electrolyte-based CBRAM) correspond to the red line and black line in Fig. 6b, respectively. The p/n/p-type oxide selector showed a non-linear I-V curve which was consisted of a high resistance region (called dead region) from 0 to 0.95 V (V_T) and a low resistance region (called turn-on region) over 0.95 V (V_T), resulting in the non-linear fact of 1.88 × 10^3 . In addition, it presented a symmetrical non-linear I-V curve when the bias was applied from 0, to 3, 0, - 3, and 0 V. Otherwise, the CuO solid-electrolyte presented a bi-stable bipolar I-V curve having V_{set} of ~0.96 V and V_{reset} of ~-1.5 V, as shown in Fig. 6b. As a result, 1S1R exhibited a symmetrical non-linear I-V curve having a positive dead region between 0 and ~0.90 V (V_T) under the application of a positive bias and the negative dead region between 0 and ~-0.80 V (V_T) under the application of a negative bias. In addition, 1S1R showed the V_{set} of ~2.4 V and the V_{reset} of ~-2.5 V by sustaining a 3.1 × 10^1 memory margin (I_{on}/I_{off}). In particular, both V_{set} (2.4 V) and V_{reset} (-2.5 V) for 1S1R were shifted into higher voltage level compared to both V_{set} (0.96 V) and V_{reset} (-1.5 V) for 1R, compare Fig. 3c with Fig. 6c, originated from the load equation that a p/n/p-type oxide selector was serially connected with a CBRAM cell. For realizing terabit integration non-volatile memory-cells, $4F^2$ cross-bar memory-cell array should be developed, requiring a half voltage scheme in which the selected memory cell for set or reset are biased with V_{set} or V_{reset} but near unselected memory-cells are biased with $\pm V_{set}/2$ or $\pm V_{reset}/2$. In particular, $\pm V_{set}/2$ or $\pm V_{reset}/2$ should be within the positive or negative

dead region. The $\pm V_{set}/2$ (1.2 V) or $\pm V_{reset}/2$ (-1.25 V) for this 1S1R in Fig. 6c were located slightly above the positive (1.0 V) or negative dead (-1.0 V) so that the non-linear factor of 1S is necessary to be increased. Thus, the 1S1R in Fig. 6c demonstrates a possibility of $4F^2$ cross-bar memory-cell array. In addition, this 1S1R presented the non-volatile memory characteristics having $\sim 1 \times 10^3$ dc set/reset endurance cycles with 100-ms pulse width by sustaining $\sim 2.57 \times 10^1$ memory margin (I_{on}/I_{off}) and $\sim 1 \times 10^5$ sec retention time at room temperature by sustaining a $\sim 2.27 \times 10^1$ memory margin (I_{on}/I_{off}), as shown in Fig. 6d and 6e.

2.5. Multi-level CuO electrolyte-based CBRAM cells.

The CuO solid-electrolyte-based CBRAM-cells have a NDR region when a negative bias is applied, which is extremely useful for multi-level-cell operation. Multi-level resistance states were achieved by varying the reset voltages after forming Ag-ion filaments, resulting from the stable NDR region at the negative bias, as shown Fig. 7. First of all, the current followed from ~ 0 A to the compliance level, I_{on}, and ~ 0 A when the applied bias was scanned from 0 to 1.5, and 0 V, corresponding to forming Ag-ion filaments where the current was limited to the compliance level, as shown in the (red) *I-V* curve in Fig. 7a. Afterward, the I_{on} (LRS: 1.6×10^{-4} A) could be read at a ~ 0.1 V reading voltage. Second, the current followed from ~ 0 A, I_{reset1}, 0 A, I_{on}, and 0 A when the applied bias was scanned from 0 V, V_{reset1} (~ -0.4 V), 0, 1.5, and 0 V, as shown in the (green) *I-V* curve in Fig. 7a. Afterward, the I_{int1} (3.5×10^{-5} A) could be read at a ~ 0.1 V reading voltage. Third, the current followed from ~ 0 A, I_{reset2}, 0 A, I_{on}, and 0 A when the applied bias was scanned from 0 V, V_{reset2} (~ -0.8 V), 0, 1.5, and 0 V, as shown in the (blue) *I-V curve* in Fig. 7a. Afterward, the I_{int2} (1.6×10^{-5} A) could be read at a ~ 0.1 V reading voltage. Finally, the current followed from ~ 0 A to I_{reset3}, 0 A, Ion, and 0 A when the applied bias was scanned from 0 to V_{reset3} (~ -1.2 V), 0, 1.5, and 0 V, as shown in the (black) *I-V curve* in Fig. 7a. Afterward, the I_{off} (HRS: 4.4×10^{-6} A) could be read at a ~ 0.1 V reading voltage. Thus, four-level current (I_{on}, I_{int1}, I_{int2}, and I_{off}) could be read by reading at ~ 0.1 V after applying V_{set} (~ 1.5 V), V_{reset1} (~ -0.4 V), V_{reset2} (~ -0.8 V), and V_{reset3} (~ -1.2 V). These results indicate that multi-level (four-level) cell operation was achieved since the applied bias determined the inversely conical shape of Ag-ion bridging filaments affecting the breaking current level.[49] The AC program/erase endurance cycles with 100-μs pulse width are shown in Fig. 7b. Four-level current of I_{on} (1.6×10^{-5} A), I_{int1} (3.5×10^{-5} A), I_{int2} (1.6×10^{-5} A), and I_{off} (4.4×10^{-6} A), with ~ 100 write/erase cycles was obtained by reading at ~ 0.1 V after applying V_{set} (~ 1.5 V), V_{reset1} (~ -0.4 V), V_{reset2} (~ -0.8 V), and V_{reset3} (~ -1.2 V). In addition, four-level current of I_{on} (1.5×10^{-5} A), I_{int1} (3.9×10^{-5} A), I_{int2} (1.5×10^{-5} A), and I_{off} (3.9×10^{-6} A) was sustained for $\sim 10^5$ sec dc retention time by reading at ~ 0.1 V after applying V_{set} (~ 1.5 V), V_{reset1} (~ -0.4 V), V_{reset2} (~ -0.8 V), and V_{reset3} (~ -1.2 V), as shown in Fig. 7c. This demonstration of multi-level AC program/erase endurance cycles and dc retention time for the

CuO solid-electrolyte-based CBRAM cells suggests the possibility that terabit-integration non-volatile memory cells with a fast write time of $\sim$ several tens of ns can be achieved.

2.6. Non-volatile memory cell operation mechanism

To investigate mechanism with which nanoscale (~ 28 nm) CuO solid-electrolyte CBRAM cells perform non-volatile memory cell operation, the *I-V c*urves were fitted with the current conduction mechanisms. The current conduction mechanism between 0 and 0.48 V (HRS) at room temperature (black line) was well fitted by ionic conduction (Equation 1) with a 1.24 slope, as shown in Fig. 8a, which is defined by

$$Ln\,J \propto Ln\,V - \left(Ln\,T + \frac{d'}{T}\right) \quad (1)$$

where *J*, *V*, *T* and *d'* are a current density, the applied voltage, the temperature, and a constant.[50-53, 56] This fitting means that Ag ions drifted following reduction process from the top Ag electrode to the TiN electrode to form Ag-ion filaments in a CuO solid-electrolyte via the ionic conduction process between negatively charged Cu vacancies. The current conduction mechanism between 0.48 V and V_{set} (~ 1.02 V) at room temperature (red line) was also well fitted by ionic conduction with a 7.66 slope, as shown in Fig. 8a. This fitting implies that the diameter of the inversely conical shaped Ag-ion filaments become thicker so that the current rapidly increased and was limited to the CC level. Note that the slope in ionic conduction from ~ 0.48 V to V_{set} (~ 1.02 V) was higher than that from 0 to 0.48 V. The current conduction mechanism from ~ 0.54 to 0V at room temperature (blue line) was well fitted with the Ohmic conduction mechanism (Equation 2) with a 1.11 slope since Ag-ion filaments remained in the CuO solid-electrolyte, as shown in Fig. 8b. The Ohmic conduction mechanism is defined by

$$ln\,(J) \propto ln(V) - \frac{c}{T} \quad (2)$$

where *J*, *c*, *V*, and *T* are a current density, a constant, the applied voltage, and the temperature. The current conduction from 0 to V_{NDR} (~ -0.4 V) at room temperature (green line) also was well fitted with Ohmic conduction with a 1.09 slope since the bias applied from 0 to V_{NDR} was not enough to break the Ag-ion filaments in the CuO solid-electrolyte, as shown in Fig. 8c. Note that the slope in Ohmic conduction from 0 to V_{NDR} (~ -0.4 V) was similar to that from 0.54 to 0 V. The current conduction from V_{NDR} (~ -0.4 V) to V_{reset} (~ -1.5 V) at room temperature (pink line) was well fitted with ionic conduction with a -0.36 slope to break Ag-ion filaments in the CuO solid-electrolyte, as shown in Fig. 8d. The current conduction from V_{reset} (~ -1.5 V) to 0 V at room temperature (purple line) was

also well fitted with ionic conduction with a 2.05 slope since Ag-ions drifted following reduction process from Ag-ion filaments to top Ag electrode after breaking the Ag-ion filaments, as shown in Fig. 8d. Note that the slope from V_{NDR} (~-0.4 V) to V_{reset} (~-1.5 V) had a negative value (-0.36), while that from 0.48 V to V_{set} (~1.02 V) had a positive value (7.66). Thus, six regions were present in the *I-V* curve for the CuO solid-electrolyte-based CBRAM cell, which well described the formation and breakage of Ag-ion filaments via ionic conduction and the current conduction of remaining Ag-ion filaments via Ohmic conduction. In particular, the current conduction mechanisms at the six regions well indicate that the CuO solid-electrolyte CBRAM cell is able to perform a non-volatile memory operation by reading the current with (after write or set) or without (after erase or reset) Ag-ion filaments in the electrolyte. The presence of a NDR region in the *I-V* curve also enables multi-level non-volatile memory operation to be performed. Furthermore, since the current conduction in the CBRAM cells via ionic conduction strongly depends on temperature, as described in equation (1), we investigated the dependency of *I-V* curves on temperature (180, 210, 240, 270, and 300 K) and the results are shown in Fig. 8e.[56] When the temperature decreased, the current decreased and V_{set} increased, indicating that Ag-ion drift following reduction process between negatively charged Cu vacancies via ionic conduction became slower when the temperature became lower, as described in equation (1). The y-intercept of *Ln(J)* vs. *Ln(V)* decreased with a decrease in temperature since it was inversely proportional to temperature (see Fig. S5), as described in equation (1) and Fig. 8f. Therefore, the dependency of *I-V* curves on temperature evidently proves that the formation or breakage of Ag-ion filaments in the CuO solid-electrolyte is performed via ionic conduction.

3. Conclusions

We have developed CuO solid-electrolyte-based CBRAM cells with 28-nm memory cell size that demonstrated good non-volatile memory characteristics such as a $~1.23 \times 10^2$ memory margin (I_{on}/I_{off}), $~3 \times 10^6$ AC set/reset endurance cycles by with 100-μs AC pulse width by sustaining a 1.31×10^2 memory margin, ~6.63-years retention time at 85 °C by sustaining a 3.63×10^2 memory margin, 100 ns program speed, and multi-level (four level) cell operation, and 1S1R operation. Unlike typical ReRAM cells, these cells' non-volatile memory characteristic showed no dependency on nanoscale memory cell size. These results imply that the newly developed cells can be terabit-integration non-volatile memory cells if the cell size is less than 20 nm. In addition, it was found that the Ag-ion filament in the CuO solid-electrolyte showed an inversely conical shape. This result indicates that Ag-ions are diffused from the top electrode and are drifted following reduction process via negatively charged vacancies in the CuO solid-electrolyte to form Ag-ion filaments. Furthermore, the current

conduction mechanism evidently explained that the cells perform non-volatile memory cell operation by forming (write or set) or breaking (erase or reset) Ag-ions in the CuO solid-electrolyte via ionic conduction of Ag-ion between negatively charged Cu vacancies in the electrolyte. In particular, the non-volatile memory cell performance of the CuO solid-electrolyte memory cells strongly depended on the material properties of the CuO solid-electrolyte such as crystallinity, poly grain size, and carrier mobility, which were determined by sputtering RF power, O_2 flow rate during sputtering, and N_2 post-annealing temperature. Thus, optimizing the sputtering process and the subsequent post-annealing process would be a key step toward achieving terabit-integration CuO solid-electrolyte-based CBRAM cells. Since 1S1R cell make it possible to achieve a cross bar structure with $4F^2$ memory cell size, it is essential to design a technique for stacking a CBRAM cell vertically on a p/n/p-type oxide selector. It is also essential to develop a design for three-dimensional stacking of cross-bar 1S1R structure with CBRAM cells to achieve terabit-level non-volatile memory cell integration.

4. Experimental Section

A ~29-nm thick SiO_2 film was deposited by chemical vapor deposition (CVD) on a SiNx/W/SiO_2 wafer and nano-holes ranging from ~28 to 1921 nm were patterned by photo lithography and dry etching. Plug-type TiN bottom electrodes with ~50-nm thickness were fabricated by TiN-film deposition on the nano-holes and subsequent chemical mechanical polishing (CMP). Then, ~25-nm thick CuO or Cu_2O solid electrolytes were deposited by RF magnetron sputtering at 90-W RF power, 40-sccm Ar flow rate, and 3-sccm O_2 flow rate for a CuO ceramic target, and 40-W RF power, 40-sccm Ar flow rate, 0-sccm O_2 flow rate for a Cu_2O ceramic target, respectively. Afterward, the top Ag electrode was thermally evaporated at a 1.0 Å/s evaporation rate under 10^{-5} Pa, followed by N_2-annealing at 500 °C for 30 min. A TiN capping layer was deposited on the top Ag electrode prior to the N_2 annealing to prevent Ag migration.[35, 57] Thus, the CBRAM cells have a sandwich device structure of bottom nanoscale (~28 ~ 1921 nm) TiN electrode, CuO solid electrolyte, top Ag electrode, and TiN capping layer. In addition, for fabricating a p/n/p-type oxide selector, 200-nm thick SiO_2 was thermally grown on a silicon wafer. The 100-nm thick bottom Pt electrode was deposited by RF magnetron sputter. ~30-nm thick p-type oxide (CoO) was deposited by RF magnetron sputtering at 90-W RF power, 40-sccm Ar flow rate, and 3-sccm O_2 flow rate for a CoO ceramic target. Then, ~10-nm thick n-type oxide (IGZO) was deposited by RF magnetron sputtering at 40-W RF power, 40-sccm Ar flow rate, and 0-sccm O_2 flow rate for a IGZO ceramic target. Subsequently, ~30-nm thick p-type oxide (CoO) was deposited at previous referred condition. The wafer was subject to the N_2-annealed at 200 °C for 30 min. Finally, 200-nm thick and 100-um-diameter top Pt electrode was deposited by RF magnetron sputtering using shadow mask. Thus, the p/n/p-type oxide selector has a symmetric

vertical structure between bottom and top Pt electrodes. To investigate the dependency of the CuO/Cu_2O solid electrolytes' resistance on N_2 annealing temperature, ~70-nm thick solid electrolyte films were deposited on 200-nm thick SiO_2 film and then annealed under N_2 ambient at 250, 400, and 500 °C °C for 30 min. Finally, ~ 200-nm thick Pt-electrodes with ~300-μm diameter were deposited and patterned by RF-magnetron-sputtering. The resistance was measured with a four-point probe by using Advanced Instrument Technology CMT-SR5000 and electrical properties were measured by using Agilent 4155C semiconductor parameter analyzers. The material properties of the CuO/Cu_2O solid electrolytes were observed by XRD (ATX-G) and TEM (JEM-2100F). The dependency of *I-V curves* on temperature was measured by using an Agilent B2902A semiconductor parameter analyzer. The AC write/erase endurance cycles were measured by using a B1500A semiconductor parameter analyzer.

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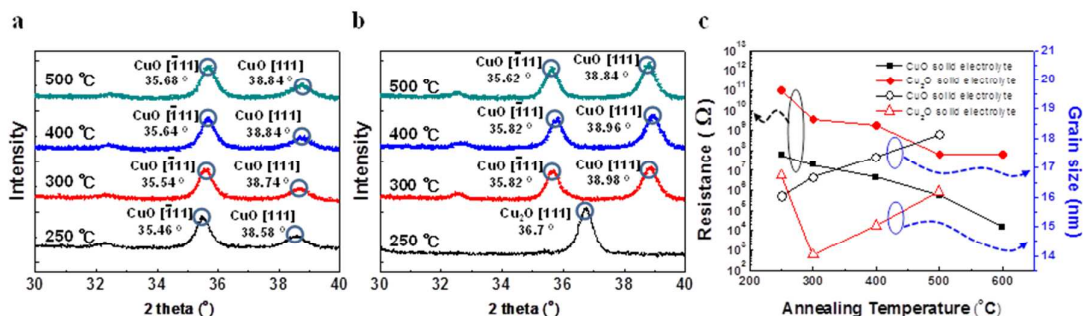57   S. Maikap, R. Panja and D. Jana, Nanoscale research letters, 2014, **9**, 1.

Fig. 1. Dependency of crystalline and electrical characteristics on N_2 post-annealing temperature. (a) XRD data for the CuO solid electrolyte, (b) XRD data for the Cu_2O solid electrolyte, and (c) resistance and average poly-grain size for the CuO and Cu_2O solid electrolytes.
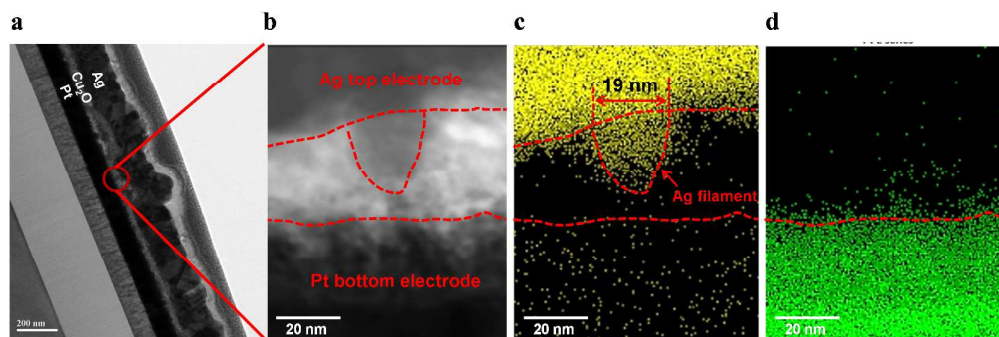

Fig. 2. Morphology of Ag-ion filaments in the Cu_2O solid electrolyte in a line-type CBRAM cell with top Ag electrode and bottom Pt electrode at the set state. (a) cross-sectional TEM image at low magnification, (b) cross-sectional TEM image at high magnification, (c) Ag ion map, and (d) Pt ion map.
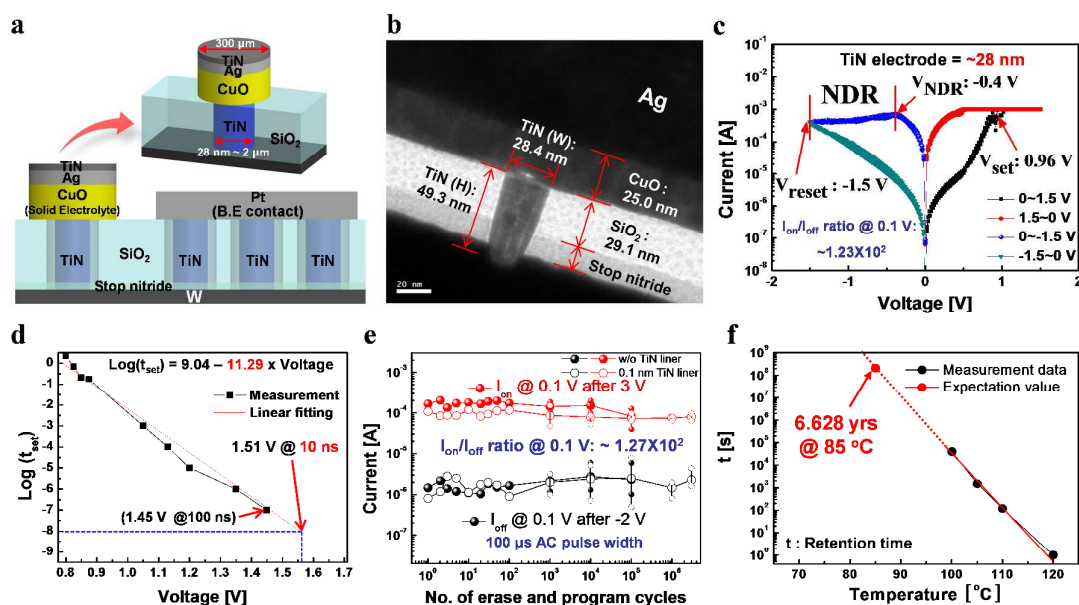
Fig. 3. Non-volatile memory cell performance for the nanoscale (~28 nm) CuO solid-electrolyte based CBRAM memory cells. (a) schematic device structure , (b) x-TEM image, (c) bi-stable dc *I-V* curve, (d) dependency of programming speed on set voltage, (e) AC write(set)/erase(reset) endurance cycles with 100-us pulse width, and (f) dc retention time at 85 ^{o}C.
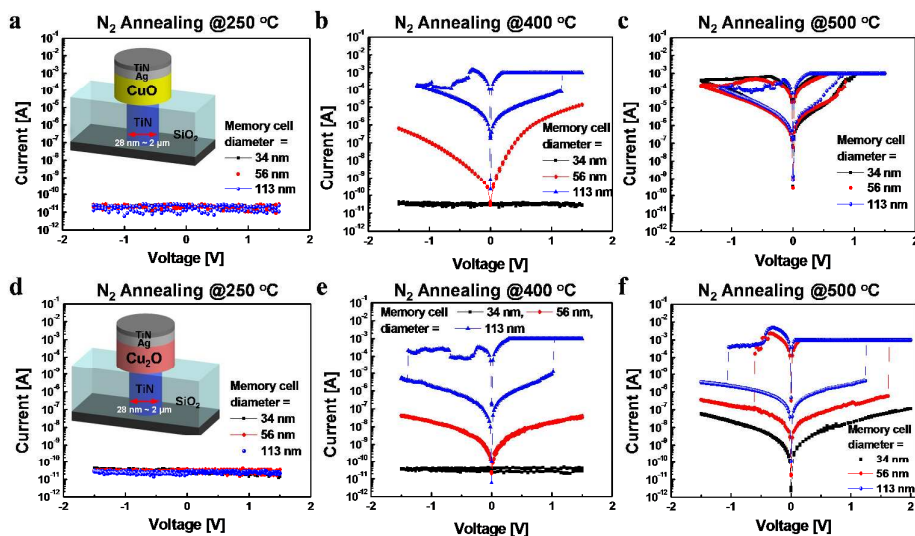
Fig. 4. Dependency of *I-V* curves on nanoscale memory cell size and N_2 post-annealing temperature for the CuO and Cu_2O solid-electrolyte-based CBRAM cells. (a) N_2 post-annealing temperature at 250 ^oC, (b) 400 ^oC, and (c) 500 ^oC for the CuO solid-electrolyte. (d) N_2 post-annealing temperature at 250 ^oC, (b) 400 ^oC, and (c) 500 ^oC for the Cu_2O solid-electrolyte.
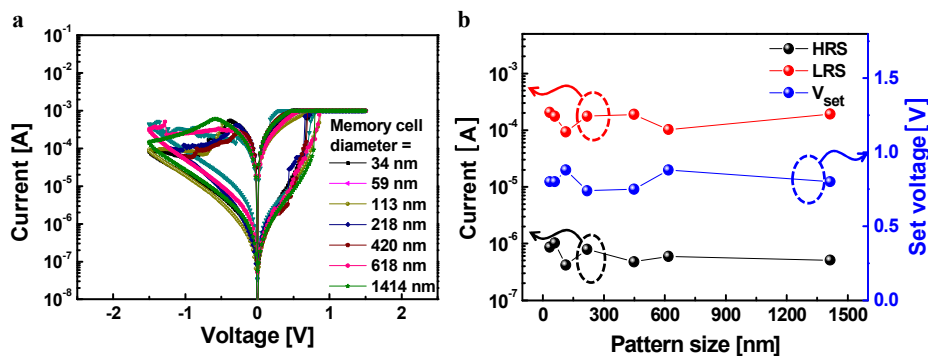

Fig. 5. Dependency of non-volatile memory characteristics on nanoscale memory cell size for the CuO solid-electrolyte-based CBRAM cells. (a) dc *I-V* curves and (b) I_{HRS}, I_{LRS}, and V_{set}.
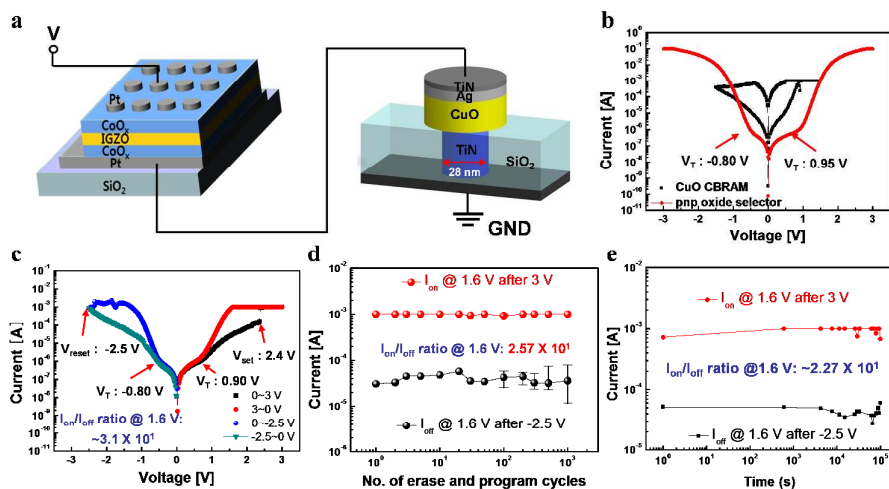
Fig. 6. 1S1R's non-volatile memory characteristics: (a) Schematic drawing of 1S1R, (b) dc *I-V* curves for the p/n/p-type oxide (CoO/IGZO/CoO) selector (1S) and the CuO solid-electrolyte-based CBRAM cell (1R), (c) dc *I-V* curves for 1S1R structure, (d) dc write(set)/erase(reset) endurance cycles with 100-ms pulse width, and (e) dc retention time at RT.
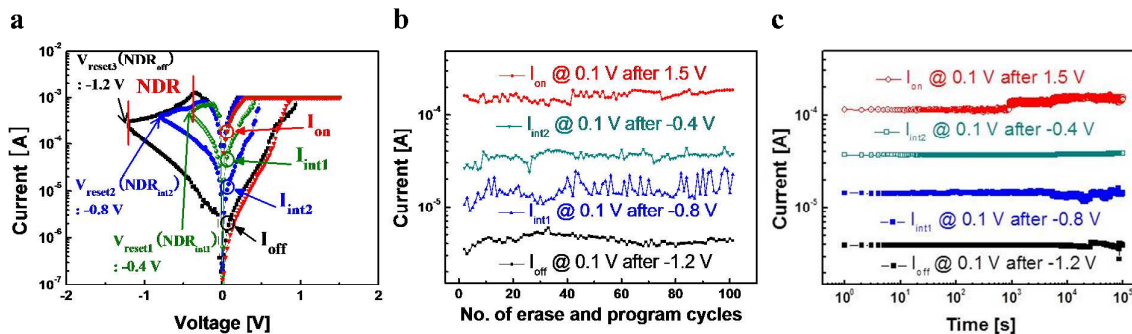

Fig. 7. Multi-level (four-level) cell operation for nanoscale (~28 nm) CuO solid-electrolyte. (a) dc *I-V* curve, (b) AC write(set)/erase(reset) endurance cycles, and (c) dc retention time at RT.
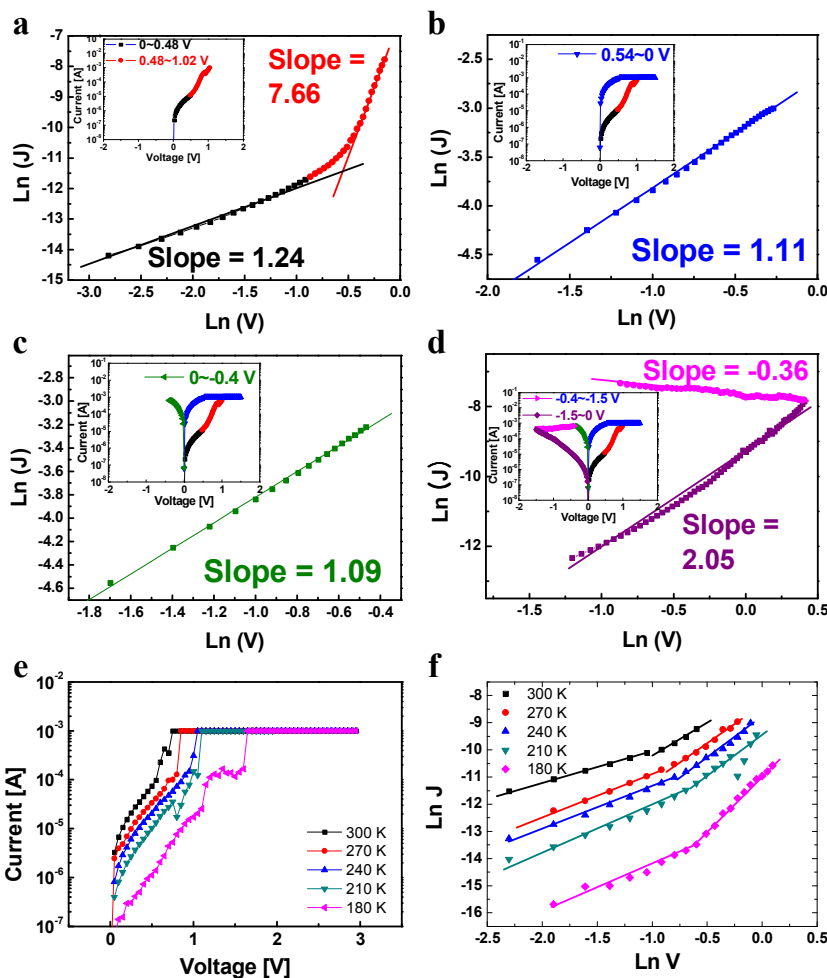

Fig. 8. Current conduction mechanisms for the CuO solid-electrolyte-based CBRAM cell. (a) HRS between 0 and 0.48 V and 0.48 and V_{set} (~0.9 V) (b) LRS between V_{set} (~0.9 V) and 0 V, (c) LRS between 0 and ~-0.4 V, (d) reset process between ~-0.4 V and V_{reset} (~-1.5 V) and HRS between V_{reset} (~-1.5 V) and 0 V, (e) temperature *I-V* measurement from 300 to 180 K. (e) dc *I-V* curves depending on temperature, and (f) *Ln (J)* vs. *Ln(V)* curves fitted by ionic conduction.