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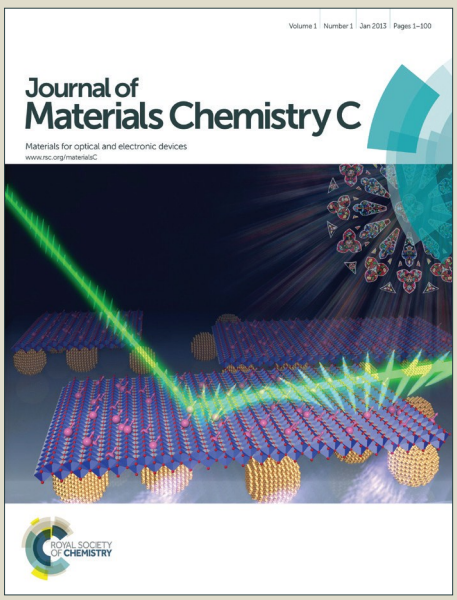

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Solution-processed p-type copper oxide thin-film transistors fabricated by using one-step vacuum annealing technique

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ABSTRACT

Copper oxide (Cu_xO) thin films were fabricated on SiO_2/Si substrates by using solution process. The coated Cu_xO gel films were treated using vacuum annealing method at various temperatures (400-700 ^oC). The X-ray diffraction results indicated that the vacuum annealing technique was effective to transform CuO into Cu_2O. The atomic force microscopy images showed that the mean grain size and the surface roughness of the resulting films increased with increasing annealing temperature. To verify the possibility of the Cu_xO thin films as channel layers, the bottom gate structured thin film transistors (TFTs) were integrated. The electrical properties of the as-fabricated Cu_xO TFTs were improved with increasing processing temperature from 400 to 600 ^oC. The 600 ^oC-annealed Cu_xO TFT exhibited the best electrical performances, including a low threshold voltage of -3.2 V, a large filed-effect mobility of 0.29 $cm^2 V^{-1} s^{-1}$, a small subthreshold swing of 0.8 V/dec, and an on/off current ratio of 1.6×10^4, respectively. However, with increasing annealing temperature further, the electrical properties of the Cu_xO TFT were degraded dramatically. These results suggest that solution-processed Cu_xO TFTs achieved from one-step vacuum annealing technique could potentially be used for high-performance p-type electronic devices, which represents a great step towards the further development of low-cost and all-oxide CMOS electronics.

1. Introduction

Compared with the conventional amorphous silicon (a-Si)-based thin film transistors (TFTs), oxide-based TFTs have received much attention because of their superior electrical properties and high optical transparencies in the visible range.[1] Until now, few studies have been carried out for the fabrication of p-type oxide TFTs compared to the n-type oxide TFTs because of the lack of p-type oxide semiconductors and the difficultly in high-quality thin film growth.[2,3]

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This undoubtedly limited the application of oxide-based TFTs and prevented the implementation of the complementary logic-based transparent electronics.[4,5]

To address these issues, since 2008, several works based on p-type oxide TFTs have been reported, including NiO,[6] Cu_2O,[7] CuO,[8] and SnO.[9] However, the fabricated p-type oxide TFTs generally exhibited inferior electrical performances compared with those n-type oxide TFTs.[10-12] This is mainly attributed to the strongly localized valence band edge of oxides, which is due to the large electro-negativity of oxygen in the valance band (VB) region. For this reason, the hole effective mass becomes very large and the filed-effect mobility is low compared to the n-type oxide semiconductors.[4,12] Among various p-type candidates, Cu_2O is one of the most promising p-type oxide semiconductors, which has been successfully considered as the low-cost and non-toxicity material for solar cell and rectifier diode applications. Meanwhile, Cu_2O is a direct-gap p-type oxide semiconductor with a bandgap of 2.0-2.6 eV, exhibiting a high hole mobility exceeding 100 $cm^2V^{-1}s^{-1}$.[13] The hole transport properties in Cu_2O are attributed to the energetically favorable electron accepting defects (copper vacancies, V_{Cu}) and the dominant Cu 3*d* character near the valence band maximum (VBM).[3,4,14] The latter leads to a more dispersive VB compared to other oxide semiconductors, particularly electron-transporting ones which strongly feature the localizing O 2*p* character near their VBM.[5,14] Therefore, Cu_2O could lead to a small hole effective mass and hence improve hole transporting properties.[5]

In the previous works, the fabrication of Cu_2O TFTs are mainly based on complex vacuum-based deposition techniques such as radio-frequency (rf) sputtering and pulsed laser deposition (PLD).[3,12,15] Although the vacuum-based deposition methods have their own advantages, the high fabrication cost and large-area device uniformity undoubtedly restrict their applications.[16] In contrast, solution-based fabrication techniques possess advantages over vacuum-based ones, including printability, large-area fabrication possibility, and low-cost characteristics.[17] To this end, solution-based techniques could potentially offer a genuine alternative processing method for the manufacturing of large-area microelectronics based on oxide semiconductors.[11,18] Recently, Kim *et al*. succefully achieved solution-processed p-channel Cu_2O TFTs for the first time.[19] In that work, a pre-annealing process in nitrogen atmosphere was carried out to obtain the metallic Cu film. Subsequently, a post-annealing process was developed in various oxygen partial pressures to prepare Cu_xO thin films. However, the two-step annealing process and the poor electrical properties (e.g. on-off current ratio~10^2) undoubtedly increases the complexity and limits the application in

high-performance electronics. In contrast, one-step vacuum annealing process has been demonstrated to be an effective and straight method for reducing CuO to Cu_2O by Sohn *et al.*[20,21] The effect of vacuum annealing is to increase the concentration of oxygen vacancies and to remove the chemisorbed oxygen.[22] During the phase transition from CuO to Cu_2O, the free energy change of the transformation moves the boundry and the out-diffusion of oxygen occurs along the moving phase boundary.[23,24]

It is known that the carrier concentration and transport properties of metal-oxide thin films, derived from molecular precursor solutions, are strongly dependent on the preparation conditions, including annealing conditions and the precursor solution concentration.[10,16,25] However, the annealing effects on the electrical properties of the solution-processed p-type oxide TFTs have never been explored before. In this report, the p-type Cu_xO thin films were synthesized by using a solution process and the vacuum annealing process was employed to prepare Cu_xO thin films at various temperatures. The effect of vacuum annealing temperature on the structural and electrical properties of the Cu_xO thin films and the TFT devices were investigated systematically.

2. Experiment section

2.1 Synthesis of oxide precursor solution

Copper acetate monohydrate [$Cu(COOCH_3)_2 \cdot H_2O$, 99%, Aldrich] was used as the metal cation precursor. A 0.1 M precursor solution was prepared by dissolving $Cu(COOCH_3)_2 \cdot H_2O$ in *N*, *N*-dimethylformamide (C_3H_7NO, 99%, Aldrich) under ambient condition. The 0.2 M ethanolamine (C_2H_7NO, 98%, Aldrich) was then added to the solution as a stabilizer. The mixed solution was stirred continuously and kept at 60 ^oC for 1 h to enhance hydrolysis.

2.2 Fabrication of Cu_xO TFTs

The heavily-doped n-type Si (resistivity ~ 0.001 Ω·cm) with a 150-nm thermally grown SiO_2 was used as the substrate and the dielectric layer. The substrates were cleaned with acetone, ethanol, and deionized water in ultrasonic washer for 10 min and dried by nitrogen gun subsequently. Finally, the substrates were exposed under oxygen plasma to enhance the hydrophilicity.

The Cu_xO precursor solution was filtered through a 0.22 μm polytetrafluoroethylene (PTFE) syringe filter and then spun on the hydrophilic Si substrates at 5000 rpm for 30 s. After spin coating, the thin films were dried at 200 ^oC on a hot plate to remove the solvent. Subsequently, the vacuum annealing process was performed under a base pressure of 2×10^{-6}

Torr at various temperatures (from 400 to 700 ^{o}C) for 2 h. Finally, the Ni source and drain electrodes were deposited on Cu_xO channel layer by thermal evaporation with a shadow mask. The devices have a channel width (W) of 1000 μm and a channel length (L) of 250 μm, respectively. The thicknesses of the Cu_xO thin films annealed at 400, 500, 600, and 700 ^{o}C are 22.6, 19.4, 17.5, and 13.8 nm, respectively.

2.3 Characterization

The surface morphologies of the Cu_xO thin films were measured by an atomic force microscope (AFM, SPA-400, Seiko). The crystal structures of the thin films were investigated by using an X-ray diffractmeter (XRD, X'Pert-PRO MPD and MRD, PANalytical, Holland) with a Cu Kα1 radiation. The electrical measurements of the TFTs were carried out by using a semiconductor parameter analyzer (Keithley 2634B) in a dark box. The thicknesses of the Cu_xO thin films were measured by ellipsometry (ESS01, Sofn Instrument).

3. Results and discussion

Figure 1 shows the XRD patterns of Cu_xO thin films annealed at various temperatures (from 400 to 700 ^{o}C) in vacuum atmosphere. It is revealed that the thin film annealed at 400 ^{o}C showed a CuO (022) orientation. With increasing the annealing temperature from 400 to 500 ^{o}C, the CuO (022) orientation decreased, while the Cu_2O (200) peak appeared. When the annealing temperature was increased to 600 ^{o}C, the peak of CuO (022) disappeared and the thin film contained Cu_2O phase only. For the thin film annealed at 700 ^{o}C, only Cu_2O (111) peak could be observed in the XRD patterns. This indicates that the vacuum annealing process can effectively reduce CuO to Cu_2O when the annealing temperature was higher than 500 ^{o}C. The mechanism of vacuum annealing process can be interpreted in terms of the oxygen desorption into vacuum.[24] The phase change from CuO to Cu_2O is caused by the phase boundary migration between the oxides induced by oxygen out-diffusion in the reaction of $4CuO \rightarrow 2Cu_2O+O_2$ along the moving phase boundary.[23] To better understand the mechanism, a simplified cross-sectional views of device with as-deposited and the vacuum annealed channel layer are illustrated in Fig. 2. In addition, the increased intensity of Cu_2O (111) peak at high annealing temperature indicates the crystallinity enhancedment of the Cu_2O thin film. The high annealing temperature supplies high kinetic energy and increases the surface mobility of deposited particles.[26] The development of the Cu_2O (111) phase is consistent with the preferred extension of the plane with the lowest surface energy for cubic-structured Cu_2O.

It is noted that the peak of Cu phase was not observed in this work, which indicated that thermal reduction of Cu^{1+} to Cu^0 was not happened during vacuum annealing process.

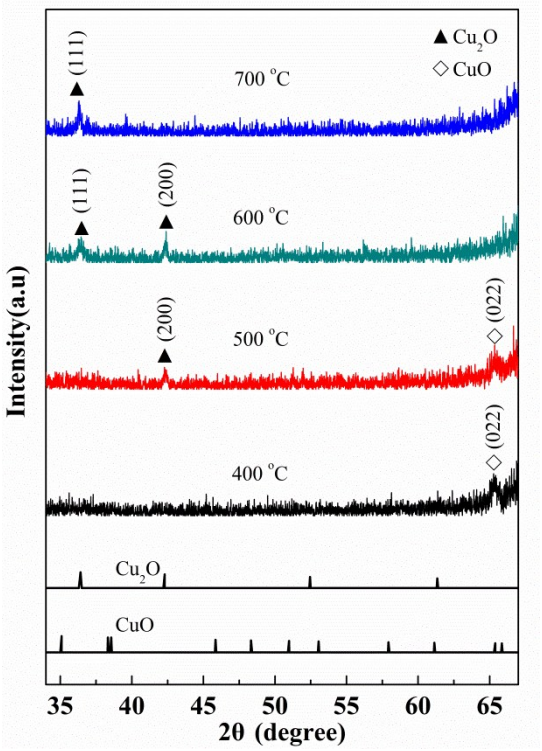

Fig. 1 XRD patterns of the vacuum-annealed Cu_xO thin films at various temperatures.

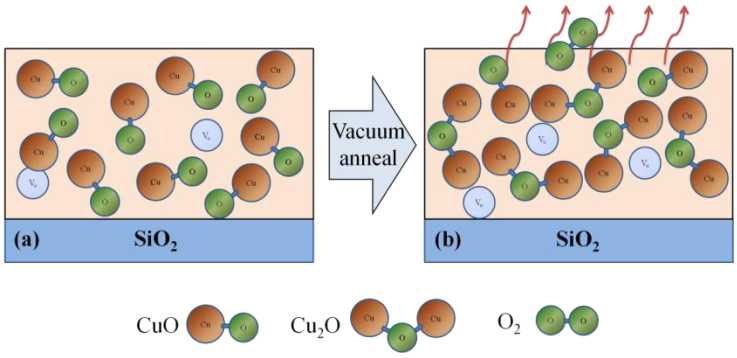

Fig. 2 Schematic cross-section view of the TFT with channel layer of (a) as-deposited and (b) vacuum-annealed Cu_xO thin films.

The surface morphologies of the Cu_xO thin films annealed at various temperatures are shown in Fig. 3(a)-(d). The scanning area was 1 μm×1 μm. The surface roughness and the average grain size of the thin films are summarized in Fig. 3(e). It is found that the root mean square (RMS) roughness and grain size of the Cu_xO thin films increase with increasing the annealing temperature. The average grain sizes of the Cu_xO thin films annealed at 400, 500, 600 and 700 ^oC are 45.82, 49.63, 62.68 and 93.48 nm, respectively. The increment of the grain size is mainly attributed to the increase of the surface energy at high temperature, which

is consistent with the previous reports.[20] The RMS values of the corresponding thin films were 4.72, 4.91, 6.23 and 6.47 nm, respectively. It is known that the electrical properties of the oxide TFTs are strongly dependent on the surface morphology and the crystalline structure of the channel layers.[19] The grain boundaries act as trapping sites for the free carrier in each grain, creating depletion layers near the grain boundaries, and effectively reduce the carrier concentration in polycrystalline thin films.[27] With increasing annealing temperature from 400 to 600 ^{o}C, the gradually increased grain size would lead to fewer grain boundary in polycrystalline Cu_xO thin films.[21] Although the largest grain size of 93.48 nm was obtained in 700 ^{o}C-annealed thin film, the serious agglomeration will undoubtedly degrade the carrier transport in Cu_xO thin film.[2,28]

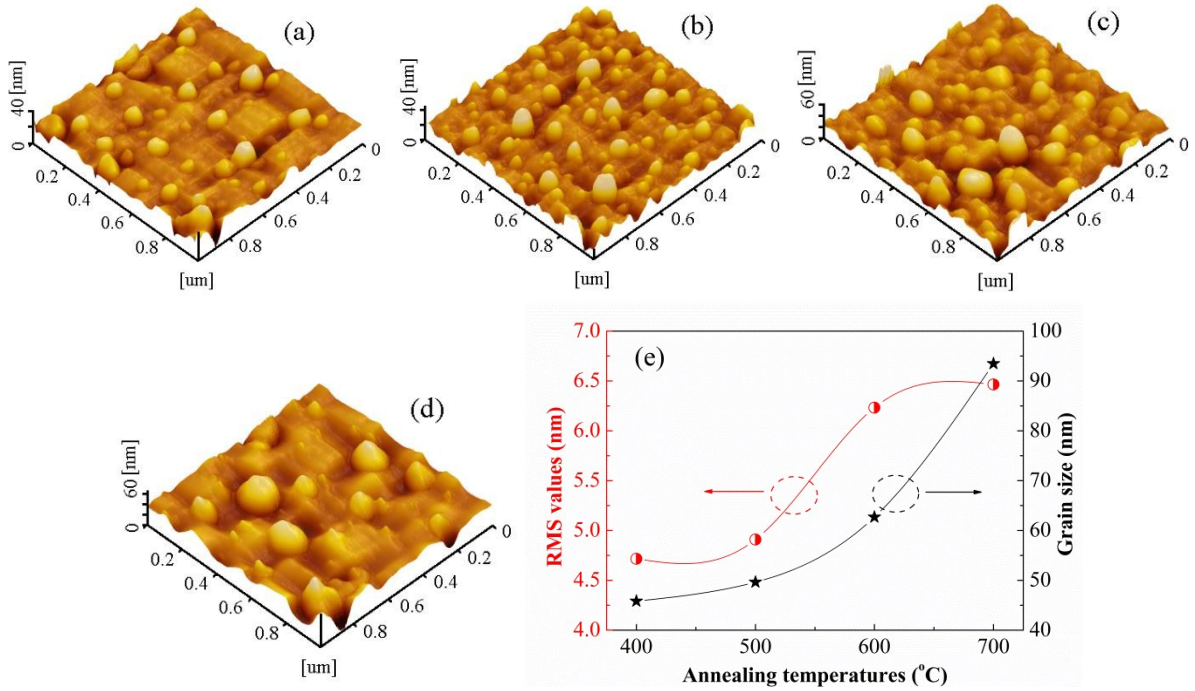

Fig. 3 AFM images of the Cu_xO thin films annealed at (a) 400 ^{o}C, (b) 500 ^{o}C, (c) 600 ^{o}C, and (d) 700 ^{o}C. (e) RMS values and grain sizes of Cu_xO thin films annealed at diffrernt temperatures

To verify the possible application of the Cu_xO thin films as the channel layers, bottom-gated TFTs based on conventional SiO_2 dielectric were fabricated and examined. The schematic diagram of the Cu_xO TFTs is shown in Fig. 4(a). For convenience, the TFTs with Cu_xO channel layers annealed at 400 ^{o}C, 500 ^{o}C, 600 ^{o}C and 700 ^{o}C, hereafter, will be abbreviated as Cu_xO-400, Cu_xO-500, Cu_xO-600 and Cu_xO-700, respectively. The typical transfer characteristics of the Cu_xO TFTs are shown in Fig. 4(b). The key electrical

parameters of the Cu_xO TFTs were calculated and summarized in Table 1. The filed-effect mobility (μ_{FE}) was estimated from the following equation,[2,12]

$$I_{DS} = \left(\frac{1}{2} \frac{W}{L} C_i \mu_{FE} \right) \left(V_{GS} - V_{TH} \right)^2 \qquad (1)$$

where W is the channel width; L is the channel length; and C_i is the areal capacitance of the gate insulator. The threshold voltage (V_{TH}) were determined from linear fits to the dependence of the square root of the I_{DS} on V_{GS}. The μ_{FE} are calculated to be 0.05, 0.26, 0.29 and 0.8×10^{-2} $cm^2\ V^{-1}\ s^{-1}$, repectively, for the Cu_xO TFTs annealed at 400-700 ^oC. The μ_{FE} was increased from 400 ^oC to 600 ^oC owing to the increase of the homogeneity and the decrease of the scattering centers, which is consistent with the AFM images (Fig. 3).[19] The dramatically degrated μ_{FE} of the Cu_xO-700 TFT is mainly related to the island growth becomes dominant. The discontinuity of the surface morphology resulted in a large interface roughness and a high degree of voids in the thin film, orignating from the growth of Cu_2O crystallites.[9] In addition, with increasing annealing temperature from 400 to 600 ^oC, larger on/off current ratio (I_{on}/I_{off}) was achieved; whereas positively shifted V_{TH} was observed. This result is consistent with the grain-boundary charge-trapping model, which accounts for the modulation of the polycrystalline semiconductor films' conductivity.[27] The subthreshold swing (*SS*) values, which is defined as the V_{DS} required to increase the I_{DS} by one decade, were calculated to be 5.1, 2.6, 0.8 and 16.8 V/dec in the Cu_xO-400, Cu_xO-500, Cu_xO-600 and Cu_xO-700 TFTs, respectively. Typically, the *SS* value is determined by the trap density (D_{it}) between the smiconductor and the gate dielectric. From *SS* we can infer the D_{it} by using the following equation,[11]

$$D_{it} = \left[\frac{SS \log(e)}{kT/q} - 1 \right] \frac{C_i}{q} \qquad (2)$$

where k, T, and q are Boltzmann's constant, absolute temperature, and charge quantity, respectively. The D_{it} values were calculated to be 7.5×10^{12}, 3.9×10^{12}, 1.1×10^{12}, and 2.48×10^{13} cm^{-2} for the Cu_xO TFTs annealed at 400, 500, 600, and 700 ^oC, respectively. It can be seen that the Cu_xO-600 have the smallest D_{it} value, which is much smaller than the previous report ($D_{it} = 5.6\times10^{13}$).[14] The improved interface in this work is mainly because that annealing of the Cu_xO films in vacuum could further promote crystal growth.[20] In addition to the optimization of *SS* value, a small D_{it} value can improve the hole mobility and the I_{on}/I_{off} of the TFTs simultanously.[14]

By combining the Cu_xO TFT performance, it is concluded that the annealing temperature of 600 °C is the optimum condition for fabricating Cu_xO channel layer, which exhibits the best electrical parameters. The corresponding output curves of the as-fabricated Cu_xO-600 TFT are shown in the Fig. 4(c). The gate voltage (V_{GS}) varied from 0 to -30 V in a step of -7.5 V. I_{DS} monotonously increases under negatively-biased gate voltage for the TFT, indicating that the Cu_2O TFT exhibits the p-channel behavior operating in an enhancement mode. Despite the relatively high processing temperature, however, the results demonstrate the possibility of fabricating low-cost solution-processed Cu_xO TFTs using simple, one-step vaccum annealing technique. Further processing of material chemistry developments and optimization are most certainly required to decrease the processing temperature and will be the subject of future studies.

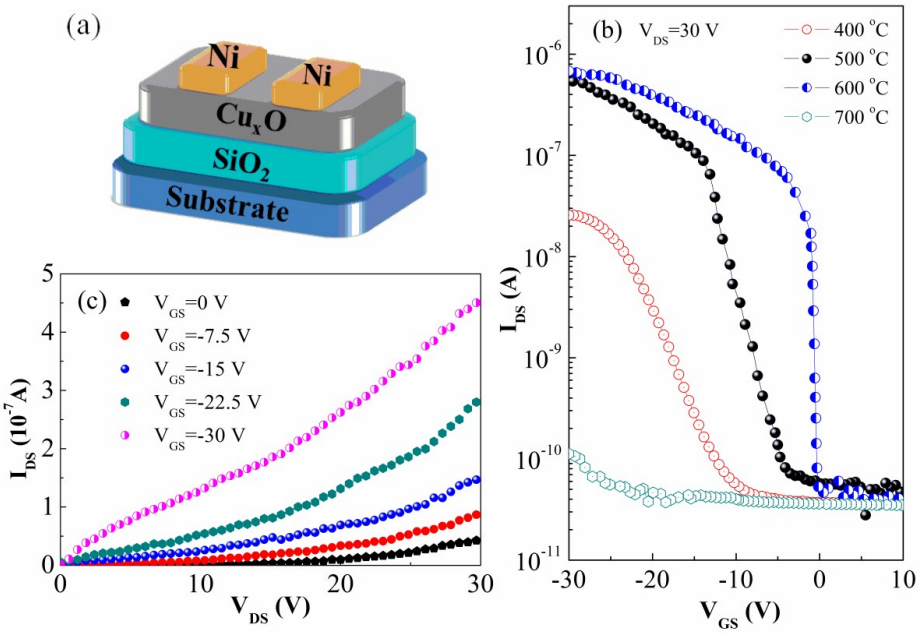

Fig. 4 (a) Schematic diagram of the Cu_xO TFTs. (b) Transfer characteristics of the TFTs with the Cu_xO thin films fabricated at various annealing temperatures in vacuum. (c) Output curve of the TFT with the Cu_xO thin film annealed at 600 °C.

Table 1 Electrical parameters of the solution-processed Cu_xO TFTs fabricated at various temperatures using vacuum annealing process

Temperature (°C)	V_{TH} (V)	I_{on}/I_{off}	μ_{FE} ($cm^2 V^{-1} s^{-1}$)	SS (V/dec)	D_{it} (10^{12} cm^{-1})
400	-15.5±2.0	10^2~10^3	0.05±0.01	5.1±1.5	7.5±2.2
500	-9.4±0.9	~10^4	0.26±0.03	2.6±1.1	3.9±1.5
600	-3.2±0.4	~10^4	0.29±0.04	0.8±0.2	1.1±0.3
700	-25.1±3.5	~4	~10^{-2}	16.8±4.5	24.8±4.5

4. Conclusion

In summary, solution-processed Cu_xO thin films were fabricated by using one-step vacuum annealing process for the first time. With the increase of the annealing temperature, the copper oxide is reduced from CuO to Cu_2O. Meanwhile, the grain size and the RMS value increase with increasing the annealing temperature. To verify the possible applications of the Cu_xO thin films as channel layers, their applications in TFT devices were demonstrated. The results show that the TFT performance was strongly dependent on the crystallinity and the surface morphology of Cu_xO channel layer. The 600 ^oC-annealed Cu_xO TFT exhibits the best electrical performance, including a high μ_{FE} of 0.29 $cm^2V^{-1}s^{-1}$, a small *SS* value of 0.8 V/dec, and a large I_{on}/I_{off} of 1.6×10^4. Our experimental results indicate that the vacuum annealing process is effective in improving the electrical properties of the solution-processed p-type Cu_xO TFTs.

Acknowledgements

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High-performance p-type Cu_xO TFTs were fabricated by solution process and annealed at various temperatures in vacuum.