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# Engineering gate dielectric surface properties for enhanced polymer field-effect transistor performance<sup>+</sup> device performance and stability due to their hydrophilicity and incompatibility with organic semiconductor materials.<sup>8,9</sup> Accordingly, a great many different self-assembled monolayers (SAMs) have been utilized to modify SiO<sub>2</sub> surface to render it hydrophobic and with organic semiconductors, 10-15 leading improvements in OFET performance. Several methodologies such as Langmuir-Blodgett (L-B),<sup>15</sup> vapor deposition,<sup>16</sup> solution immersion <sup>17</sup> and spin-coating techniques,<sup>14</sup> etc. have been utilized to form SAMs on SiO<sub>2</sub> surface. In general, L-B and spin-coating techniques afford relatively ordered SAMs on SiO2 surface, 14,15 but the processes need to be delicately controlled, and are thus not easily scalable to large-area processing. Vapor deposition, while providing high-quality SAMs, is also not practical as it involves deposition in vacuum oven at elevated temperatures (100~200 °C) for a substantially long period of time.<sup>16</sup> The most convenient method for SAM formation on SiO<sub>2</sub> surface is silvlation via solution treatment in which the SiO<sub>2</sub> substrate is immersed in a dilute solution of a silylating agent for a period of time in ambient conditions, followed by solvent rinsing and air drying.<sup>3</sup> This method provides a robust silane SAM as the latter is chemically bonded to the SiO<sub>2</sub> surface through silylation of the hydroxyl groups.<sup>5</sup> However, this procedure may have the drawback of producing SAMs with incomplete surface coverage of gate dielectric,14 giving rise to higher leakage current. Incomplete SAM surface coverage also leads to rougher dielectric surface morphology which adversely affects dielectric/semiconductor interfacial properties.

In this paper, we report our studies on silane modification of SiO<sub>2</sub> gate dielectric via solution treatment, employing four silylating agents of functionally varied structures, methyltrichlorosilane (MTS), phenyltrichlorosilane (PTS), octyltrichlorosilane (OTS-8), and octadecyltrichlorosilane (OTS-18). We will show the effects of silane SAM fabrication conditions on its quality, particularly its surface coverage and defects, on OFET performance using two known polymer semiconductors, diketopyrrolopyrrole-dithienylthieno[3,2b]thiophene (DPP-DTT) (I) and regioregular poly(3-hexythiophene)

# Introduction

In recent years, organic field-effect transistors (OFETs) have generated considerable interest as a low-cost transistor technology for large-area electronic applications.<sup>1-3</sup> Unlike traditional silicon devices, OFETs utilize a small molecule or polymer material as channel semiconductor, offering functionally capable performance when the channel semiconductor achieves high crystalline orders for charge transport efficacy. One of the important factors which affect the crystallinity of channel semiconductor is gate dielectric. Through surface chemistry, the gate dielectric interacts with the overlaying semiconductor and exerts a definitive influence on the molecular ordering of semiconductor, thus its charge transport properties.<sup>4,5</sup> Other critical factors are the dielectric strength and surface morphology of gate dielectric which affects its charge blocking ability as well as the dielectric/semiconductor interfacial properties. The latter in turn has significant impacts on the charge transport in the semiconductor channel.

So far many organic and inorganic insulating materials, including silicon dioxide (SiO<sub>2</sub>), metal oxides, polymers and their composites, have been studied as gate dielectrics in OFETs. Among them, SiO<sub>2</sub> on heavily-doped, conductive silicon wafer has been the most popular and widely investigated for OFETs. This is because SiO<sub>2</sub> surface is very flat and offers excellent reproducibility in device fabrication and performance. Moreover, it possesses a high density of surface hydroxyl groups, permitting great flexibility in tuning its surface properties via chemical reaction for OFET performance.5-7 The surface hydroxyl groups, if left untreated, would adversely affect

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compatible

Modification of silicon dioxide (SiO<sub>2</sub>) gate dielectric with silane self-assembled monolayers (SAMs) via silylation was conducted to study its impacts on polymer field-effect transistor (FET) performance. SAMs formed from silylating agents with long alkyl chains such as octadecyl gave high field-effect mobility but lower on/off ratio because of lower SAM coverage of the gate dielectric surface. In contrast, SAMs from silvlating agents with phenyl or medium alkyl chains (octyl) provided high on/off ratio from high SAM surface coverage but lower mobility due to their inefficiency in promoting molecular ordering of the channel semiconductor. By treating the SiO<sub>2</sub> dielectric surface with two silylating agents, one with an octadecyl chain and one with a octyl or phenyl chain, in proper sequence, a high-performance "hybrid" dual-silane SAM could be created, enabling attainment of both high mobility and on/off ratio, together with other desirable FET properties.

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(regio-P3HT) (II), as channel semiconductors in a bottom-gate, topcontact OFET configuration (Figure 1). Our studies demonstrate that both the silylating agents and the manner with which they are deposited on SiO<sub>2</sub> surface are critical to the quality of the resulting silane SAMs. By treating the SiO<sub>2</sub> surface with two silylating agents, one with a long alkyl chain (OTS-18), and one with a medium alkyl chain (OTS-8) or phenyl group (PTS) in proper sequence, we can capitalize on the efficacy of long alkyl chain silane-SAM in enhancing semiconductor ordering and the high surface coverage of medium alkyl or phenyl silane-SAM in blocking charge leakage to create a dual-silane "hybrid" SAM which provides the best of both worlds. In line with these considerations, our studies have demonstrated a simple, highly efficient, and readily reproducible silane modification process for SiO<sub>2</sub> dielectric, enabling fabrication of high-performance OFETs with high mobility, low leakage current, and high current modulation.

### Results and discussion

The formation of silane-SAMs via silvlation of hydroxyl functions of SiO<sub>2</sub> surface with silvlating agents is graphically presented in Figure 2. The water contact angles of untreated SiO<sub>2</sub> and silvlation treated SiO<sub>2</sub> surface with different silane SAMs are summarized in Table 1. The untreated SiO<sub>2</sub> surface displayed a water contact angle of 25°, showing a very hydrophilic surface with high surface energy due to the abundance of surface hydroxyl groups (Fig. 2a). When the SiO<sub>2</sub> surface was treated with a silvlating agent, the water contact angle increased significantly, demonstrating transformation of a hydrophilic, high-surface energy. This was attributable to the formation of a chemically bonded hydrophobic silane-SAM on the SiO<sub>2</sub> surface through silvlation of its surface hydroxyl functions.



Fig. 1 Schematic representation of experimental OFET device configuration and chemical structures of polymer semiconductors and silylating agents.



Fig. 2 Schematic representation of modification of  $SiO_2$  surface with various silylating agents forming silane self-assembled monolayer through silylation of surface hydroxyl functions.

Specifically, the measured contact-angles were 140°, 73°, 99° and 104° respectively for MTS, PTS, OTS-8 and OTS-18 modifications (Table 1). These contact angles are quite close to those measured for the modifications via similar or other processes,<sup>5,18,19</sup> Other than the extremely high contact angle of MTS modification, these results showing that the hydrophobicity of SiO<sub>2</sub> surface increased with the carbon atoms or alkyl chain length of the silylating agent. The water contact angle of MTS modification has been reported to vary widely, from below 90° to over 150°, depending very much on treatment process, reaction time and temperature, etc. <sup>20</sup> It is highly likely that the high water contact angles after MTS treatment arise from the very high surface coverage due to formation of multi-layer polymethylsiloxane network on the substrate.<sup>20,21</sup>

Interestingly, when the SiO<sub>2</sub> surface was treated with two different silylating agents in sequence, the contact angle of the resulting SiO<sub>2</sub> surface was quite different, depending on which silvlating agent was employed first. Specifically, treatment with a silylating agent carrying a phenyl, small (methyl) or medium alkyl (octyl) chain first, followed by a silylating agent carrying a long alkyl (octadecyl) chain produced a contact angle that was essentially similar to one treated with a silylating agent with respectively a phenyl, a small or medium alkyl silvlating agent only. For example, treatment with OTS-8 first, followed by OTS-18 (herein referred to as "OTS-8/OTS-18") afforded a contact angle of 99° (Fig. 2d), which was the same as the OTS-8only treatment (Fig. 2b). In another word, when the surface was first treated with a silylating agent carrying a small or medium alkyl group, subsequent silvlation reaction appeared to be ineffective in impacting the resulting surface properties. On the other hand, the reverse modification, i.e. treatment with OTS-18 first, followed by OTS-8 (herein referred to as "OTS-18/OST-8"), yielded a larger contact angle (106°; Fig. 2e) than that of OTS-8-only (99°) or OTS-18only (104°) treatment (Fig. 2c). These results suggest the following: (i) treatment by a silylating agent with a small to medium alkyl chain or substituent such as methyl, phenyl, or octyl group led to complete or near-complete silvlation of surface hydroxyl groups, leaving little room for further silylation; (ii) treatment by a silylating agent carrying a long alkyl chain (e.g., OTS-18) left some unreacted hydroxyl groups or surface "voids" due to steric interference of long alkyl chain with the silylation reaction, thus rendering subsequent silylation with a sterically less-demanding silylating agent such as PTS

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Table 1 Water contact angles of untreated/silane-SAM modified  $SiO_2$  surface and electrical properties of DPP-DTT-based OFETs on untreated and silane-SAM-modified  $SiO_2$  gate dielectrics.

Silylating agents	Contact angle (°)	Average FET mobility	On/off notio	Off-current	S.S.
		$(cm^2/V \cdot s)$	On/on rano	(nA)	(V/decade)
Untreated	25 ± 2	0.11	$3.8 \times 10^{2}$	86	8.3
MTS	$140 \pm 2$	0.29	$1.6 \times 10^{5}$	0.5	2.6
PTS	$73 \pm 1$	0.23	$2.3 \times 10^{5}$	0.3	2.4
OTS-8	$99\pm2$	0.73	$6.1 \times 10^{5}$	0.2	2.2
OTS-18	$104 \pm 2$	1.86	$1.6 \times 10^{4}$	18	3.0
MTS/OTS-18	$140 \pm 1$	0.21	$7.4 \times 10^4$	1.2	3.3
OTS-18/MTS	$118\pm2$	0.34	$0.8 \times 10^{4}$	110	5.7
PTS/OTS-18	$74 \pm 2$	0.24	$1.4 \times 10^{5}$	0.9	2.3
OTS-18/PTS	$105 \pm 2$	1.97	1.3×10 <sup>6</sup>	0.4	2.2
OTS-8/OTS-18	$99\pm2$	0.69	$6.7 \times 10^{5}$	0.3	2.1
OTS-18/OTS-8	106 ± 1	2.04	1.5×10 <sup>6</sup>	0.3	2.1

or OTS-8 feasible; and (iii) silylation with a long alkyl silylating agent such as OTS-18 first, followed with a silylating agent with a medium alkyl chain or substituent, such as OTS-8 or PTS, was most efficient for surface modification of  $SiO_2/Si$  dielectric for OFET application.

When a polymer semiconductor was solution-deposited on the silane-modified SiO<sub>2</sub> surface, the surface roughness of the resulting semiconductor film varied with the silylating agent and modification conditions. This was obviously related to the morphology of silane-SAM on the  $SiO_2$  surface due to the extent of silane surface coverage and ensuing SAM surface defects. To gain a better understanding, the morphology of the DPP-DTT (I) semiconductor films on different silane-modified SiO<sub>2</sub> dielectrics was analyzed by atomic force microscopy (AFM). Figure 3 shows the AFM height images of the DPP-DTT (I) thin films on OTS-8, OTS-18 and dual-silane modified SiO<sub>2</sub> substrates. All showed small semiconductor grain size with different surface roughness. The root-mean-square (RMS) roughness values for the semiconductor films on OTS-8- and OTS-18-treated SiO<sub>2</sub> substrates were 1.0 nm (Fig. 3a) and 1.5 nm (Fig. 3b), respectively. The very smooth semiconductor film on the OTS-8 treated substrate correlated well with the high surface coverage of OTS-8 modification and its resulting smooth surface morphology. The much rougher semiconductor film on OTS-18 SAM was attributed to the rougher OTS-18 SAM surface resulted from some surface "voids" due to incomplete silvlation. On the other hand, the semiconductor film on the SiO<sub>2</sub> surface with OTS-8/OTS-18 dualsilane treatment had a surface roughness of 0.9 nm (Fig. 3c), which was practically similar to that of the OTS-8-only modification. This was because OTS-8, when treated first, provided near-complete surface coverage, leaving no room for subsequent OTS-18 silylation.

(a) OTS-8	(b) OTS-18	(c) OTS-8/OTS-18	(d) OTS-18/OTS-8	
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<u>1 ш</u>	n <u>1</u>	іт <u>1</u> µ	.m	12.5 em
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RMS=1.0 nm	EMS=1.5 nm	RMS=0.9 nm	<sub>ङ्ख</sub> . RMS=1.1 nm	

Fig. 3 AFM images showing surface roughness of polymer semiconductor (I) films on silane-modified  ${\rm SiO}_2$  substrates.

This explanation was corroborated by the finding that both OTS-8 and OTS-8/OTS-18 SiO<sub>2</sub> surface modifications gave the same contact angle of 99°. In sharp contrast to the rougher polymer film on the SiO<sub>2</sub> surface of OTS-18-modification (RMS = 1.5 nm), the polymer film on OTS-18/OTS-8 dual silane-treated SiO<sub>2</sub> substrate displayed very smooth surface (RMS = 1.1 nm; Fig. 3d). The improvement in surface roughness in this case was the result of further silylation by OTS-8 on the OTS-18 partially covered SiO<sub>2</sub> surface.

The effects of silane-modified SiO<sub>2</sub> gate dielectrics on OFET performance were investigated firstly using DPP-DTT (I) as channel semiconductor in a bottom-gate, top-contact device configuration under ambient conditions. No precautionary measures were taken to exclude atmospheric oxygen, moisture and ambient light during device fabrication and evaluation. Figure 4 and Table 1 show the transfer characteristics and extracted field-effect properties of OFET devices with untreated and silane-modified SiO<sub>2</sub> gate dielectrics. The control device on untreated SiO<sub>2</sub> gate dielectric (Fig. 4a) exhibited average field-effect mobility of only 0.11 cm<sup>2</sup>/V·s and on/off ratio of  $3.8 \times 10^2$ . With silane-modified SiO<sub>2</sub> gate dielectrics (Figs. 4b-g), significant improvements in mobility, on-off ratio and other FET properties of devices were observed (see Table 1). Specifically, the mobility enhancement follows the order: OTS-18 > OTS-8 > PTS ~ MTS, while the on/off ratio, the order: OTS-8 > PTS ~ MTS > OTS-18.

The fact that OTS-18 modification provided highest mobility (1.86 cm<sup>2</sup>/V·s) was related to the efficiency of long octadecyl chain in promoting the molecular ordering of the overlaid channel semiconductor carrying long alkyl side-chains. On the other hand, OTS-8 modification gave lower mobility (0.73 cm<sup>2</sup>/V·s), suggesting that octyl chain was less efficient in facilitating (I) achieve higher crystallinity. The much lower mobility of MTS- and PTS-modified devices was attributable to the general inefficiency of methyl and phenyl group in promoting the molecular ordering of organic polymer semiconductors. Direct evidence for supporting higher crystalline orders of DPP-DTT polymer semiconductor on OTS-18teated substrate was obtained from the wide-angle, out-of-plane XRD data. Fig. 5 shows the XRD diffraction patterns of DPP-DTT film (~40 nm) on various SiO<sub>2</sub> substrates. It is found that the DPP-DTT thin film on untreated SiO<sub>2</sub> yielded a weak diffraction peak (100) at  $2\theta$ =4.45. In contrast, the semiconductor on the silane SAM treated



Fig. 4 FET performance of OFETs with DPP-DTT (I) as channel semiconductor fabricated on untreated and silane-modified SiO<sub>2</sub> substrates. (a) to (e): transfer characteristics of untreated, OTS-8, OTS-18 and dual-silane-modified gate dielectrics, showing performance improvements with silane modifications; inserts are extracted mobility ( $\mu$ ), on/off ratio; off-current (I<sub>off</sub>), and subthreshold swing (S.S.); (f): transfer characteristics of OFETs with MTS and its OTS-18 dual-silane-modified gate dielectrics; (g): transfer characteristics of OFETs with PTS and its OTS-18 dual-silane-modified gate dielectrics.

SiO<sub>2</sub> substrates yielded much stronger diffraction peak but without changing the peaking position. In particular, the DPP-DTT film on SiO<sub>2</sub> with OTS-18 SAM treatment displayed the strongest (100) diffraction and a discernable (200) diffraction at 20=8.89, confirming the efficacy of long alkyl chain such as OTS-18 in efficiently promoting molecular ordering of DPP-DTT polymer semiconductor. These results are also in line with previous observations that short and medium alkyl chains formed "liquid-like" SAMs while long alkyl chains yielded "more crystalline" SAMs.<sup>22,23</sup>



Fig. 5 Out-of-plane XRD patterns of DPP-DTT thin films (~40 nm) on untreated and silane-treated SiO<sub>2</sub> substrates.

Aside from exerting decisive influence over channel semiconductor ordering, the nature of silane-SAM also had notable impacts on semiconductor/dielectric interfacial properties and dielectric structural integrity. Thus, we observed that while OTS-18 modification provided high field-effect mobility, the on/off ratio of the device was comparatively low (1.6×10<sup>4</sup>). The latter was about one order of magnitude lower than those of OTS-8- or PTS-modified devices. This was obviously attributable to higher off-current (18 nA) of the OTS-18 device because of incomplete surface SAM coverage. This incomplete surface SAM coverage was corroborated by the fact that further silvlation after OTS-18 modification was possible, and yielded OFET devices with much lower off-current. The OTS-18modified devices also displayed larger subthreshold swing (S.S. ~3.0 V/decade; Fig. 4c), revealing significant charge trapping at the semiconductor/dielectric interface likely due to interfacial defects from rougher dielectric surface morphology. In contrast, the OTS-8 (Fig. 4b) and PTS (Fig. 4g) devices had very low off-current (0.2 - 0.3)nA), high on/off ratio (>1×10<sup>5</sup>) and smaller S.S. (2.2 – 2.4) by virtue of full or near complete surface SAM coverage of SiO<sub>2</sub> gate dielectrics (see Table 1).

The above results showed that OTS-8 or PTS dielectric modification was very effective in achieving low off-current, thus high on/off ratio, while OTS-18 modification was particularly efficient in promoting semiconductor ordering leading to high mobility. It thus appeared that one can capitalize on the performance strengths of these silylating agents to create a "hybrid" SAM composition, enabling simultaneous achievement of both high mobility and high on/off ratio, together with other desirable FET properties. This

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hybrid modification approach, comprising of first treatment with OTS-18, followed with OTS-8 or PTS, would yield a structurally robust and smoother composite SAM. The latter would be predominantly rich in OTS-18 with the otherwise remaining surface voids filled up with OTS-8 or PTS, thus enabling essentially complete surface SAM coverage (Fig. 2e). The richness of OTS-18 in the hybrid SAM would enhance device mobility while the high surface SAM coverage with the accompanying smoother surface morphology, would strengthen device's charge blocking capability as well as remove charge trapping sites in the semiconductor/dielectric interface. Characterization of OFET devices with hybrid SAMs of this nature yielded field-effect mobility of 1.97–2.04 cm<sup>2</sup>/V·s and on/off ratio of >10<sup>6</sup> with very low off-current of 0.3-0.4 nA and smaller S.S. of 2.1-2.2 V/decade. This was a strong affirmation on the efficacy of OTS-18/OTS-8 or OTS-18/PTS hybrid SAM in promoting semiconductor ordering on the one hand, and in enhancing the resistance to charge leakage as well as lowering interfacial charge trapping density on the other hand.

It should be emphasized that the ability of dual-silane hybrid SAM in enhancing OFET performance hinges critically on the sequence of two silylation reactions. Thus, we observed that the reverse modification, i.e., OTS-8/OTS-18 (Fig. 4d) or PTS/OTS-18 (Fig. 4g) hybrid SAM, showed no meaningful improvements in OFET performance over those of respectively OTS-8 SAM (Fig. 4b) or PTS SAM (Fig. 4g). This is in agreement with the fact that OTS-8/OTS-18 or PTS/OTS-18 SAM was compositionally quite similar to that of OTS-8-only or PTS-only SAM since the first treatment with OTS-8 or PTS had silylated virtually all the surface hydroxyl groups, leaving no room for further silylation.

The performance improvements of OFETs through utilization of a mixture of OTS-8 and OTS-18 in a single-step silylation of SiO<sub>2</sub> gate dielectric were also investigated. Table S1 summarizes the variations of OFET properties with respect to the OTS-18: OTS-8 mole contents in the silvlating mixture. Some improvements in field-effect mobility and on/off ratio, while not as impressive as the two-step hybrid procedure, could still be achieved by engaging a high ratio of OTS-18 to OTS-8 in silvlation. The optimal ratios appeared to be around 0.8: 0.2 of OTS-18: OTS-8 where reasonably high mobility of 1.8 cm<sup>2</sup>/V·s and on/off ratio of  ${\sim}10^5$  were attained. Nevertheless, this surface modification approach for OFET performance improvement still paled in comparison to the two-step hybrid approach where much higher mobility and on/off ratio could be readily achieved. This is because in the single-step modification, two silylating agents compete with each other for the surface hydroxyl groups; their respective rates of slilyation are difficult to control as these are dependent on their reactivity as well as their relative ratio in the reaction mixture.

To demonstrate the general applicability of the hybrid SAM approach for OFET applications, we also utilized a widely studied, commercially available polymer semiconductor, *regio*-P3HT, as the channel semiconductor. The transfer characteristics and the corresponding FET properties of the devices fabricated and measured in ambient conditions are respectively provided in Figure 6 and Table S2. On untreated SiO<sub>2</sub> gate dielectric, the devices showed very low mobility of only 10<sup>-4</sup> cm<sup>2</sup>/V·s and on/off ratio of 10. With PTS, OTS-8 and OTS-18 silane modifications, the performance improved in the same manner as for the DPP-DTT devices. The best performance improvements were again observed with the hybrid



Fig. 6 Transfer characteristics of OFET devices with regio-P3HT channel semiconductor on untreated and various silane-modified  $SiO_2$  gate dielectrics.

dual-silane modifications. Both the OTS-18/OTS-8 and OTS-18/PTS hybrid SAMs delivered much higher mobility ( $^{10^{-2}}$  cm<sup>2</sup>/V·s), higher on/off ratio ( $^{10^{3}}$ ), and lower off-current (2-3 nA).

## Conclusion

Our studies show that the surface chemistry and morphology of gate dielectric exert great influence on OFET performance, and proper surface modification is central to achieving high performance characteristics in OFETs. Thus, while OTS-18 modification of SiO<sub>2</sub> gate dielectric affords high field-effect mobility, the on/off ratio is comparatively low. On the other hand, OTS-8 or PTS modification leads to higher on/off ratio, but lower field-effect mobility. By combining these two silane modifications of SiO<sub>2</sub> gate dielectric in proper sequence to create a hybrid silane SAM, one can capitalize on the performance strengths of two silylating agents in achieving both high mobility and high on/off ratio in OFETs, together with other desirable OFET performance characteristics. Thus, the present dual-silane SAM modification process, i.e., OTS-18/OTS-8 or OTS-18/PTS represents an efficient surface modification of SiO<sub>2</sub> gate dielectric for OFET performance.

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A high-performance "hybrid" dual-silane SAM enables attainment of both high mobility and on/off ratio, together with other desirable FET properties.

