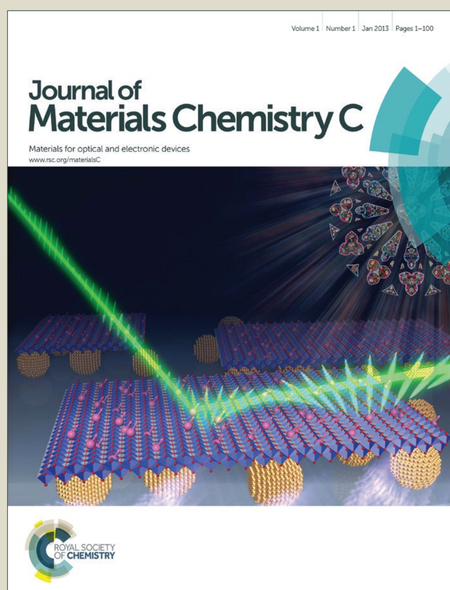
Journal of Materials Chemistry C

Accepted Manuscript



This is an *Accepted Manuscript*, which has been through the Royal Society of Chemistry peer review process and has been accepted for publication.

Accepted Manuscripts are published online shortly after acceptance, before technical editing, formatting and proof reading. Using this free service, authors can make their results available to the community, in citable form, before we publish the edited article. We will replace this *Accepted Manuscript* with the edited and formatted *Advance Article* as soon as it is available.

You can find more information about *Accepted Manuscripts* in the Information for Authors.

Please note that technical editing may introduce minor changes to the text and/or graphics, which may alter content. The journal's standard Terms & Conditions and the Ethical guidelines still apply. In no event shall the Royal Society of Chemistry be held responsible for any errors or omissions in this *Accepted Manuscript* or any consequences arising from the use of any information it contains.

ROYAL SOCIETY OF CHEMISTRY

www.rsc.org/materialsC

Journal Name

ARTICLE

Ultrahigh performance negative thermalresistance switching based on individual ZnO:K,Cl micro/nanowires for multibit nonvolatile resistance random access memory dual-written/erased repeatedly by temperature or bias

Received 00th January 20xx,
Accepted 00th January 20xx

DOI: 10.1039/x0xx00000x

www.rsc.org/

Jie Zhao,[a] Baochang Cheng,*[ab] Yanhe Xiao,[a] Rui Guo[a] and Shuijin Lei[a]

Currently, nanostructure-based random access memories (RAMs) mainly focus on the writing of data information by electricity. Here, nonvolatile multibit thermalresistive RAMs (TRAMs), which are dual-written/erased by different temperatures or drain-source biases, are realized successfully in two-terminal devices based on individual ZnO:K,Cl micro/nanowires. The mechanism of emptying and filling of trap states is proposed for the explanation of temperature and bias controlled multibit information writing and erasing. The incorporation of KCl in ZnO lattice creates abundant defects, which can serve as trap centers and store charges. At relatively high temperature, the trapped charges can escape under a low operation voltage, resulting in a downshift of ZnO Fermi level, and moreover the depth of emptied trap is dependent of loaded temperature. Therefore, a tunable high resistance state can be obtained. At relatively high bias, subsequently, electrons can inject into trap states under a low operation temperature, and moreover the depth of filled trap depends on applied voltage. Therefore, a tunable low resistance state can be acquired due to an upshift of ZnO Fermi level. It is due to the thermal excitation and electric field injection induced emptying and filling of trap states that multibit information can effectively be dual-written/erased by different temperatures or biases. The results indicate that the modulation of trap states by impurity introduction in nanostructures gives a direction to the development of novel nanodevices in rewritable nonvolatile temperature and bias information sensor and memory.

1. Introduction

Candidates for modern nonvolatile random access memories (RAMs), including ferroelectric random access memory (FeRAM),[1] in which the polarization of a ferroelectric material is reversed, magneto-resistive RAM (MRAM),[2] in which a magnetic field is involved in the resistive switching (RS), resistive RAM (RRAM),[3] in which the two very distinct resistance levels are switched by submitted to a voltage pulse, and phase-change RAM (PRAM),[4] in which thermal processes control a phase transition in the switching material from the amorphous state to the crystalline state, have attracted a great deal of attention. Compared with the capacitance-based RAMs, the resistance-change-based RAMs, especially for one-dimensional (1D) RRAMs, are believed to be much free from the inherent scaling problem. The RS characteristics of semiconductor micro/nanowires, such as NiO,[5,6] ZnO,[7] Zn_2SnO_4,[8] and $GeSe_2$,[9] have been extensively studied in resistance-change-based RAM due to its superior performance in simple fabrication process, lower power consumption, long retention time, high operation speed, high endurance write cycles, non-destructive readout, favorable scalability, and CMOS process compatibility.[10-13]

In the RRAM technology, the "0" and "1" logical states correspond to the RS back and forth between low resistance state (LRS) and high resistance state (HRS) by submitted to voltage pulses, and depending on the set and reset processes, the RS characteristics can be classified into bipolar and unipolar switching types.[14,15] The switching mechanism can be attributed to conducting filament,[16,17] charge-trap model alteration of Schottky barrier,[18,19] space-charge-limited current,[20] and Mott transition.[21,22] Recently, back-to-back bipolar RSs were observed in the ohmic and Schottkey contact two-terminal devices.[8,23] In 1D micro/nanostructure based systems, the injection of electrons into/from surface and interface states created by doping can modulate their barrier height, and therefore their conduction states can be well controlled. ZnO micro/nanowire, owing to a wide direct bandgap, a large exciton binding energy, and abundant trap states, becomes the ideal candidate for back-to-back Schottky-like diode, and properly doped ZnO micro/nanowire can

[a] School of Materials Science and Engineering, Nanchang University, Jiangxi 330031, P. R. China. E-mail: bcheng@vip.sina.com
[b] Nanoscale Science and Technology Laboratory, Institute for Advanced Study, Nanchang University, Jiangxi 330031, P. R. China

†Electronic Supplementary Information (ESI) available. See DOI:10.1039/x0xx00000x

This journal is © The Royal Society of Chemistry 20xx

Journal of Materials Chemistry C Accepted Manuscript

Please do not adjust margins

introduce impurity levels and various defect traps, which combine with surface/interface states and intrinsic trap states to form miscellaneous depth trap levels.[24-26]

In order to meet the demands for increased data storage capacity, multibit memory devices have been explored to replace single bit memory devices. For traditional NAND flash memories, it is difficult to realize the scale-down of multibit storage to the size of a single memory cell due to the geometric configuration, which may face some challenge, such as retention, leaky, or endurance reliability issues when device shrinking, and several works have been proposed to solve the problem.[27] For RS memory devices in previous work, the effective mulitbit effect almost based on setting gates or fabricating special configurations.[28-30,31] In addition, comparing to widely exploration for electrical information program, the RRAM, used for thermal data writing, has no relative reports, although the temperature detectors and sensors are rapidly developed today.

In this work, novel programmable thermalresistive RAMs (TRAMs), based on two-terminal devices of individual ZnO:K,Cl superstructure micro/nanowires, were fabricated for the first time, which made the temperature and drain-source bias information acquisition and memory realized easily. The mechanism dominantly originates from the abundant bulk trap states donated by the incorporation of K and Cl impurities. The switching between HRS and LRS corresponds to emptied and filled trap states, respectively, which are regulated by thermal excitation and electric injection, respectively. More interestingly, the depth of emptied and filled trap state can controllably be adjusted by the imposed temperature and bias, which makes the memory a further application in nonvolatile temperature/bias 'dual-writing/erasing' multibit TRAM without the assistance of gate voltages.

2. Experimental

2.1 ZnO:K,Cl Micro/nanowires Synthesis

ZnO micro/nanowires were synthesized on an Al_2O_3 ceramic substrate in a three-zone furnace by a carbonthermal reduction method. Pure zinc oxide powders were mixed with graphite in a mass ratio of 2:1, and potassium chloride was added with a Molar ratio of 5 %. The mixed powders were collected in a ceramic boat and placed the upstream of gas flow. Then the Al_2O_3 ceramic substrate was placed downstream. Argon was used as carrier gases with a flow velocity of 100 sccm. Micro/nanowires were grown within a temperature window of 900-980 °C with an elevated rate of 10 °C per min and holding for 120 min. After the growth process, the furnace was cooled down to room temperature (RT).

2.2 Two-Terminal Devices Fabrication

A thin insulating alumina ceramic substrate was washed with ethanol and deionized water under sonication. Under an optical microscope, an ultra-long ZnO:K,Cl micro/nanowire was transferred on the substrate and the two ends of the micro/nanowire were fixed by silver paste. It should be noted that all of the manufactures and measurements were taken in air, and the output values of devices were hardly to show equal as the differences were inevitable between each single micro/nanowire.

2.3 Characterization and Performance Measurement

The morphology and crystal structure of as-produced micro/nanowires were characterized by X-ray diffraction (XRD, RIGAKU D/max-3b), field-emission scanning electron microscopy (FE-SEM, FEI Quanta 200F), X-ray photoelectron spectroscopy (XPS, ESCALAB 250) and high-resolution transmission electron microscopy (HRTEM, JEOL JEM-2100), respectively. For the performance measurements of multibit nonvolatile TRAMs, the RT was confirmed to be 283 K. Heat source utilized a hot-plate with a highest temperature of 673 K. If the device was not in contact with the heat source, it was placed on a large metal plate to keep at RT. The output signals of TRAMs were carried out by a synthesized function generator (Stanford Research System Model DS345) and a low-noise current preamplifier (Stanford Research System Model SR570). In addition, all the measurements were characterized in dark to avoid the disturbance of light illumination.

3. Results and discussion

3.1 Morphology and Structure Characterization of As-Synthesized ZnO:K,Cl

Typical XRD pattern for as-synthesized product is shown in Fig. 1a. All the diffraction peaks can be indexed to ZnO with a hexagonal structure (JCPDS No. 36-1451). Representative FESEM observation of as-prepared sample is shown in Fig. 1b. As can be seen, the product presents ultralong wire-like morphology with a length in the range from several micrometers to hundreds of micrometers with a diameter of hundreds of nanometers. In order to obtain more detailed information about the microstructure of the micro/nanowires, HRTEM measurement was performed. Fig. 1c shows the HRTEM image of the micro/nanowire, taken along the [100] zone axis. The corresponding fast Fourier transform (FFT) pattern is shown in Fig. 1d. The image of the rectangle region bracketed in Fig. 1c is analyzed by the back and forth FFT using only the (002) diffraction spots as shown in Fig. 1e, indicating the presence of dislocations denoted by "T" and lattice distortion. XPS was used to characterize the chemical composition of as-synthesized micro/nanowires. It can be seen from the core-level photoelectron peaks in Fig. 1f-i that as-prepared micro/nanowires are mainly composed of Zn, O, K, and Cl atoms. Furthermore, comparing with nominally undoped ZnO nanowire, ZnO:K,Cl micro/nanowire presents many dislocations randomly, as shown in Fig. 1j and k, indicating that K and Cl dopants can introduce abundant defects.

3.2 Temperature Response and Memory Effect

To investigate the temperature dependence of conduction performance, the output current of the device was consecutively measured by direct annealing from RT to 400 ^{o}C at a fixed bias voltage of 0.5 V, as illustrated in Fig. 2a. It can be seen obviously that the output current of device decreases first and

Journal of Materials Chemistry C Accepted Manuscript

This journal is © The Royal Society of Chemistry 20xx

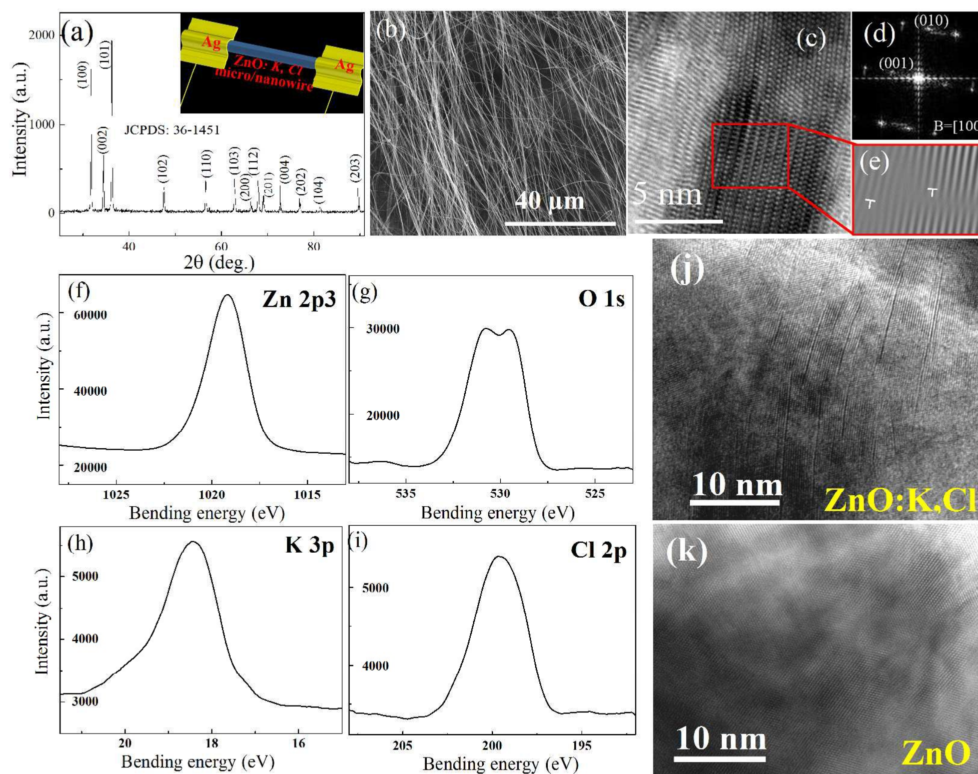


Fig. 1. Structural characterization and composition analysis of as-synthesized micro/nanowires. (a) XRD pattern. The inset in Fig.1a is a device schematic. (b) FESEM image, showing wire-like morphology. (c) HRTEM image and (d) corresponding FFT pattern, which can be indexed to hexagonal ZnO with [100] zone axis. (e) Back and forth FFT pattern from (002) diffraction spots of the rectangle region bracketed in (c) and dislocations are marked by 'T'. The high resolution XPS spectra of Zn 2p3 (f), O 1s (g), K 3p (h) and Cl 2p (i). HRTEM images of ZnO:K,Cl micro/nanowire (j) and undoped ZnO micro/nanowire (k).

reaches a minimum at about 200 °C, and subsequently increases with further increasing temperature. Additionally, the output currents were also measured by annealing from RT to 75, 200, 250, 260, 270, 300, and 375 °C, respectively, and then recooled to RT, as shown in Fig. 2b and c. It is clear that the single ZnO:K,Cl nanowire-based device is highly sensitive to externally imposed temperature. The device shows a negative giant thermalresistance switching performance at the measurement temperature lower than about 270 °C. On the contrary, it shows a positive thermalresistance switching effect at the measurement temperature higher than about 270 °C. After it is completely cooled to RT, more interestingly, the device can still remain a HRS at the annealing temperature lower than 270 °C, namely the presence of an outstanding resistance difference before and after annealing. Moreover, the HRS can remain for a long time, indicating a nonvolatile memory effect. In addition, the maximum variation in resistance can be obtained before and after annealing at about 200 °C. The results indicate that ZnO:K,Cl has a huge potential for temperature sensor applications, especially for nonvolatile temperature-writing memory applications at an operating temperature lower than 270 °C.

I-V characteristics of TRAM cell were further measured at a low bias voltage of 0.5 V before, under and after annealing at 200 and 375 °C, respectively, as shown in Fig. 3. It can be observed that the changing trend of resistances is consistent with that in Fig. 2. Compared with the conductivity of device before annealing, it not only shows a significant reduction under annealing at 200 °C, but remains a distinguishable decrease after annealing at 200 °C. Contrarily, its conductivity exhibits a huge increase under annealing at 375 °C, and unfortunately it shows hardly a variation after annealing at 375 °C, indicating a poor memory effect. Interestingly, each resistance state echoes a certain temperature, which may enable a memory capacity for writing temperature information bit-by-bit into the two-terminal TRAM cell. Therefore, the temperature-related data storage capability can be achieved at annealing temperature lower than 270 °C. The resistance state which responds to the temperature above 270 °C, may not be an appropriate choice for memory due to little resistance variation.

After annealing at the temperature lower than 270 °C, the device shows a HRS. More interestingly, the device can return to its initial LRS after applying a relatively high bias voltage at RT, indicating that the stored temperature information can be erased effectively by a relatively high drain-source bias. Fig. 4 shows the detailed cyclic I-V characteristics in LRS, HRS, and the course of erasing information. It can be seen that all the I-V characteristics show nonlinear behavior before and after

Journal of Materials Chemistry C Accepted Manuscript

This journal is © The Royal Society of Chemistry 20xx

Please do not adjust margins

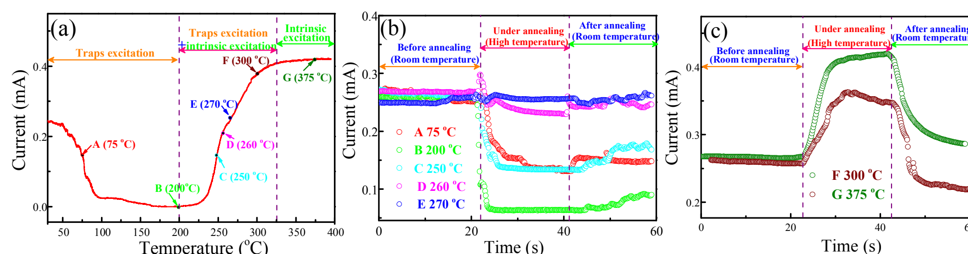


Fig. 2. Resistance variation of TRAM cell before, under and after annealing at different temperatures. (a) The current response to temperature varied consecutively from RT to 400 ^{o}C at a fixed bias voltage of 0.5 V, revealing that the dominant conduction mechanism changes from a trap excitation into an intrinsic bandgap excitation with increasing temperature. (b) The device is heated from RT to 75, 200, 250, 260, and 270 ^{o}C, respectively, and then re-cooled to RT, revealing that there is an obvious increase in resistance after annealing, namely a memory behavior. (c) The device is heated from RT to 300, and 375 ^{o}C, respectively, and then re-cooled to RT, revealing that the resistance decrease during annealing and moreover it merely shows a little variation after annealing.

annealing at 200 ^{o}C, as show in Fig. 4a. To more deeply take insight into the conduction mechanism of TRAM devices, the I-V curves were fit by Poole–Frenkel (PF) emission law.[32,33]

$$J = BVexp\left(\frac{-q\left(\phi_t - \sqrt{qV/\pi\,\varepsilon_0\varepsilon_r d}\right)}{kT}\right) \quad (1)$$

Where B is constant, q is unit charge, ϕ_t is barrier energy height for electron emission, ε_r is relative permittivity of the RS medium, d is thickness between the two electrodes, k is Boltzmann constant, and T is temperature. In Fig. 4b, the inset shows the test fittings for the plotting lnI/V versus $V^{1/2}$. The linear plots suggest that PF emission (bulk limited) is the most predominant conduction mechanism in the applied voltage range of 0–0.5 V, demonstrating that the electrical transport is dominated by the bulk traps rather than the surface state related Schottky barrier at micro/nanowire and electrode interface. Moreover, in order to investigate the relationship between effective trap depth of PF emission and temperature, the applied voltage was constant of 0.5 V, and the relation between ϕ_t and T can be simplified as follow:

$$-Tln(I) \propto \phi_t \quad (2)$$

The temperature dependence of PF emission potential height, from room temperature to 400 °C, was analyzed in Fig. 4c. The trap potential ($-q\phi_t$) is the energies required to transfer electrons from the trap level to the conduction band and the value can be calculated. According to Reference,[33-35] the value of $-q\phi_t$, as obtained are about 287.75 and 761.05 meV for RT and 200 ^{o}C, respectively. The fitting results indicate that the PF trap levels is strongly dependent of temperature, which is consistent with the experiment result as illustrated in Fig. 2a, confirming the lower the current level by temperature effect, the larger the trap level for electron barrier.

As seen from Fig. 4d, the annealed device shows a nonvolatile HRS at read-out voltage lower than 0.5 V. With increasing bias voltage, subsequently, the current jumps abruptly at the voltage of about 4.2 V, switching from HRS to LRS in accompany with a large hysteresis loop, as show in Fig. 4e. Thus, a reset process occurs at about 4.2 V. The corresponding I-V curve was fitted by Fowler–Nordheim (FN) tunnelling,[33,36-40]

$$J = \frac{q^2E^2}{16\pi^2 h\phi_{ox}}exp\left(\frac{-4\sqrt{2m^*}(q\phi_{ox})^{\frac{3}{2}}}{3hqE}\right) = C_1E^2exp\left(\frac{-C_2(q\phi_{ox})^{\frac{3}{2}}}{E}\right) \quad (3)$$

Where E is electric field, q is unit charge, ϕ_{ox} is energy barrier that must be overcome by electron, m^* is electron mass in as-prepared micro/nanowires, h is reduced planck constant, and C_2=6.82×10^3(eV$^{-3/2}$Vμm^{-1}).[37,38] The slope of data fitting under high voltage in Figure 4f led to an extracted electron barrier height ($q\phi_{ox}$) of about 58.87 meV at RT. The FN tunnelling fitting results indicate that the extracted electron barrier strongly depend on the applied bias voltage. Moreover, the depth of filled traps increases with increasing bias voltage, which is well consistent with the experiment results as illustrated in Fig. 11 (b). The A linear decrease relation of ln(|I/V^2|) versus |1/V| can be obtained when the applied bias exceeds the mutation voltage of about 4.2 V, as shown in Fig. 4f. Afterward, when the bias voltage is swept to a negative value, the device current remains LRS, and moreover it is still in LRS under the subsequent cyclic sweeping, demonstrating that the device has become LRS after it is first subjected to a voltage higher than 4.2 V. A nonvolatile ON state is achieved. Therefore, the temperature induced nonvolatile HRS can be erased effectively by applying a relatively high bias voltage. Although the current behaviour under negative voltage sweeping is fairly similar to that under positive voltage sweeping, the hysteresis loop shrinks fast as sweeping progresses going on. For this, several cycles of erasing process

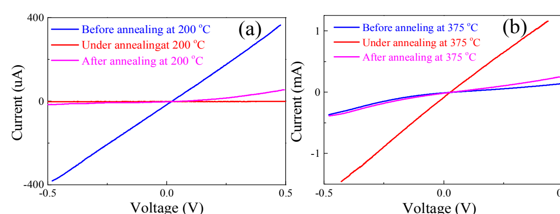


Fig. 3. I–V characteristics of ZnO:K,Cl micro/nanowire-based device before, under, and after annealing at different temperatures. (a) Before, under and after annealing at 200 ^{o}C, revealing the presence of a significant resistance difference before and after annealing. (b) Before, under and after annealing at 375 ^{o}C, revealing the presence of negligible resistance difference before and after annealing.

This journal is © The Royal Society of Chemistry 20xx

Journal of Materials Chemistry C Accepted Manuscript

Please do not adjust margins

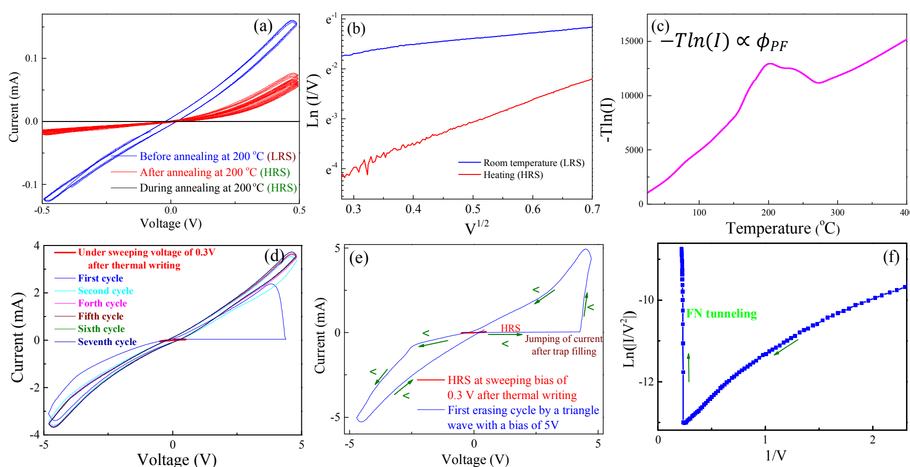


Fig. 4. Cyclic I-V characteristics. (a) At 0.5 V bias voltage, consecutively cyclic I-V characteristics before (blue curves) and under (red curves) annealing at 200 °C, showing a stable device performance at low operating bias. (b) Fitted curves for the positive bias part before and after annealing in (a) by PF emission mechanism. (c) Fitted curve of –Tln(I) vs T, showing the variation of ϕ_{PF} emission height with temperature. (d) After 3 consecutive I-V cycles at 0.3 V bias under HRS, 7 consecutive erasing I-V cycles are swept at a relatively high bias of 5 V, revealing that the device changes into LRS after first applying a high bias. (e) I-V characteristic of the first erasing cycle by using a triangle wave voltage with amplitude of 5 V, revealing the transition from HRS to LRS at about 4.2 V, namely reset/erase process induced by trap filling. (f) Fitted curve for part 1 and 2 in (e) by FN tunnelling mechanism.

under ±5 V were taken, as shown in Fig. 4d. It shows that a relatively large hysteresis loop at first, and then gradually decelerate to zero with periodic cycles.

Owing to the presence of remarkable resistance variation before and after annealing at 200 °C, the temperature was chosen for the memory measurement of TRAM cell. Moreover, the HRS of the device, annealed at about 200 °C, can return to its initial LRS after applying a relatively high bias voltage higher than 4.2 V between two-terminal electrodes, indicating that the stored temperature information can be effectively erased by applying a high drain-source bias voltage. This indicates that suitable temperature and drain-source bias can serve as “gating” on tuning the charge carrier transport in ZnO device. Fig. 5 shows the thermalresistance memory performance for the two-terminal device operated at a fixed bias voltage and triangle wave voltage, respectively. The data can be effectively set/written by annealing at 200 °C under a low operation bias voltage of 0.5 V, and reset/erased by applying a relatively high bias voltage of 5 V in the condition of RT. In the course of readout, moreover, a similarly low bias voltage of 0.5 V is applied. Here, we define the resolution as

$$R = \frac{I_{on} - I_{off}}{I_{off}} \qquad (4)$$

Where I_{on} is LRS current before annealing and I_{off} is HRS current after annealing. As seen from the enlargement of a single write-read-erase-read cycle process, as shown in Fig. 5b and d, the resolution can reach two orders of magnitude. The response time of temperature and electricity sensing are 5 s and 0.4 s, respectively, as shown in Fig. 5e and f. The consecutive write-read-erase-read processes reveal a reversible and repeatable memory property. In addition, temperature-related information can be stored for a long time, and moreover they can be reset by a relatively high bias voltage, as shown in Fig. 6, confirming that the nonvolatile nature of the device is stable and durable.

3.3 Temperature and voltage dependence of memory mechanism

Fig. 7 shows the schematic diagrams of energy band structure and trapped electron distribution for illustrating the multibit TRAM effect in the two-terminal device. Since the work function of Ag (Φ_{Ag}=4.26 eV) is lower than the electron affinity of ZnO (χ_{ZnO}=4.35 eV), it is expected that the ohmic behaviour would be formed when ZnO is in direct contact with Ag electrodes. In RT, however, the I-V curves show nonlinear characteristics rather than typical liner ohmic contact characteristics, as shown in Fig. 3 and 6. It has been accepted that oxygen molecules can capture free electrons from the surfaces of n-type ZnO, which creates a surface space-charge layer from the surface to the interior.[41,42] For one-dimensional ZnO micro/nanowires, abundant trap states, such as surface/interface states, intrinsic trap states, and impurities introduced by doping, exist inside them. The I-V curves, before and after annealing, can be fitted well by PF emission mechanism, as seen Fig. 6a. Therefore, the bulk defects related traps are dominant conduction mechanism rather than surface traps related Schottky barrier. In nanostructure ZnO, the introduction of K and Cl dopants can form defects such as dislocation and lattice distortion, clearly confirmed by HRTEM observation. Therefore, the defects can serve as trap centers and capture electrons. Moreover, the stored electrons can be excited from one trapped state by a random thermal fluctuation, and then hop into another trapped state. When the trap states are emptied, the population of electrons excited by thermal fluctuation decrease, and correspondingly the Fermi level of ZnO will downshift, resulting in a decrease of conductivity. As

Journal of Materials Chemistry C Accepted Manuscript

Please do not adjust margins

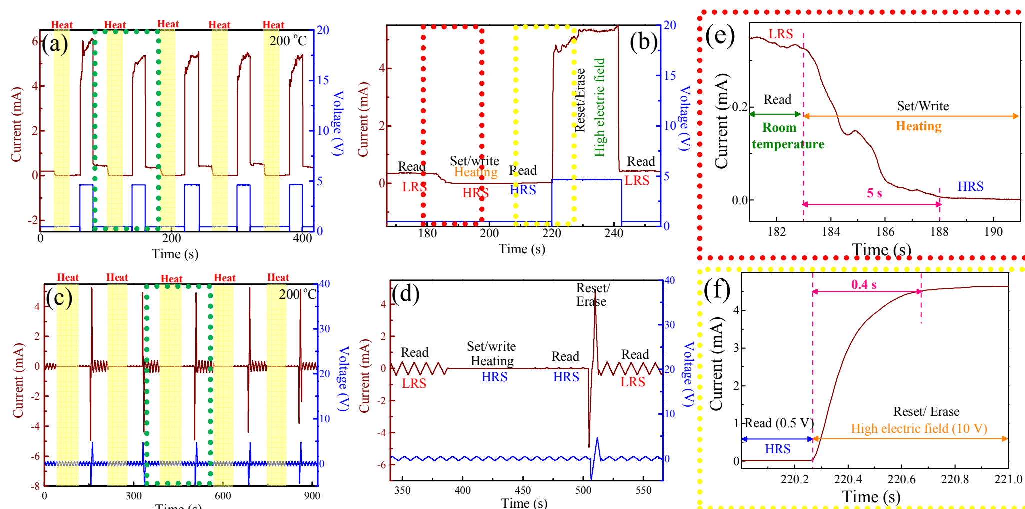


Fig. 5. Write/read access of TRAM cell. Set/write by annealing at 200 °C, reset/erase by applying a high bias of 5 V at RT, and the write and readout bias is under a relatively low bias of 0.5 V. The red curves represent the current response, and the blue curves correspond to the applied voltage. (a) 5 consecutive read-write-read-erase cycles operated under a fixed bias voltage. (b) An enlargement of green dotted frame in (a), showing a detailed read-write-read-erase process. (c) 5 consecutive read-write-read-erase cycles operated under a triangular wave voltage. (d) An enlargement of green dotted frame in (c), showing a detailed read-write-read-erase process. (e) An enlargement of red dotted frame in (b), showing the respond time of about 5 s of temperature sensing. (f) An enlargement of yellow dotted frame in (b), showing the respond time of about 0.4 s of electricity sensing.

seen from Fig. 2a, with increasing temperature, the conduction of RRAM will go through three stages: trap excitation, trap excitation-intrinsic bandgap excitation, and intrinsic bandgap excitation. With the increase of temperature from RT to 200 °C, electrons trapped by deeper level will be excited. Under annealing at 200 °C, the resistance of devices reaches a maximum, indicating the trapped electrons escape completely, and then decreases with further increasing temperature. When the annealing temperature continues to rise, subsequently, its resistance decreases gradually. Under annealing at 270 °C, its resistance can recover to the initial value at RT. After the device is annealed at the temperature higher than 270 °C, moreover, it only takes place a slight variation in resistance, indicating that the conduction will mainly dominated by intrinsic bandgap excitation. In addition, as seen from the cyclic I-V characteristic measured at 200 °C, as shown in Fig. 8, the traps can be filled at the voltage higher than about 4.2 V, whereas it is immediately emptied with decreasing bias voltage, which more firmly demonstrates the origination of temperature and bias dependence of memory effect from trap states.

Upon applying an external electrical field between drain and source electrodes, the energy band will tilt. When the applied bias voltage reaches 4.2 V, the tilt height of energy band (qV) will exceed the height of trap barrier ($\Delta\phi$), resulting in a filling of trap. It is easier for electrons to freely move inside ZnO lattice, and hence the Fermi level of ZnO will upshift and its conductivity increases significantly. As a consequence, the device transforms from HRS to LRS, namely reset process. It is due to the thermal excitation and electric field injection of electrons that result in a memory effect.

In thermal trap excitation stage, the depth of excited trap states increases with increasing temperature and shows a maximum at 200 °C. At the temperature lower than 200 °C, therefore, the trapped electrons can be thermally excited from traps to the conduction band (CB) and then the emptied traps are left in ZnO, resulting in a HRS.

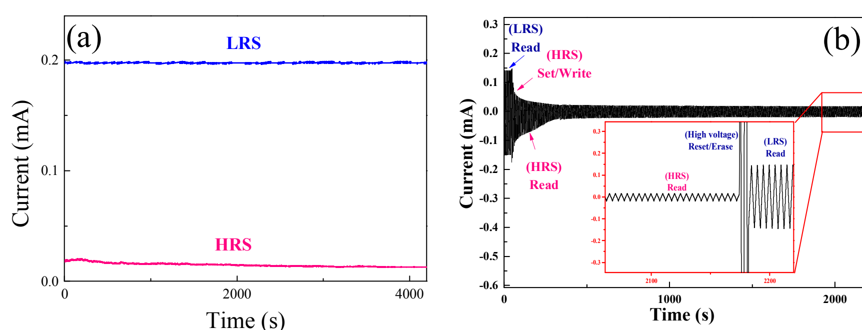


Fig. 6. Stability and retention measurement of TRAM cell in both LRS and HRS at RT. (a) Readout by a fixed low bias voltage of 0.5 V. (b) Readout by a consecutive triangle wave voltage with low amplitude of 0.5 V and frequency of 0.1 Hz.

 This journal is © The Royal Society of Chemistry 20xx

Journal of Materials Chemistry C Accepted Manuscript

Please do not adjust margins

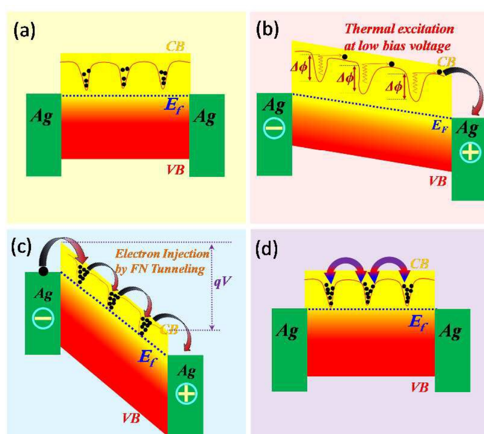


Fig. 7. Schematic energy band structure and trapped electron distribution diagrams for illustrating memory effect in the two-terminal TRAM cell, where E_f, Δϕ, and qV are Fermi level, trap height, and electric field induced tilt height of energy band, respectively. (a) Before annealing, the trap states are partially filled by electrons. (b) After annealing, the trap states are completely emptied due to thermal excitation, and the Fermi level downshifts. The device shows a HRS. (c) At high external bias voltage, the emptied trap states are filled up by electrons from the negative electrode and the Fermi level downshifts. The device transforms from HRS into LRS. (d) After applying a relatively high bias, trap states are filled, which is advantageous for electrons to hop between different traps.

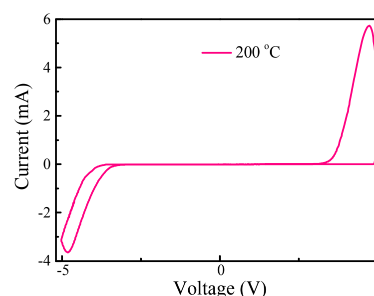


Fig. 8. I-V characteristic measured at 200 °C under a relatively high bias voltage of 5 V, revealing that the traps can be filled at the voltage higher than about 4.2 V, whereas they are immediately emptied with decreasing bias voltage.

In thermal trap excitation-intrinsic bandgap excitation stage, the bandgap excitation is relatively weak, and few electrons can be excited directly from valence band (VB) to CB. The electrons excited from VB can fill into traps and subsequently localized in traps, resulting in a decrease of resistance. The mechanism of memory is similar to that of thermal trap excitation stage. In thermal trap excitation stage and thermal trap excitation-intrinsic bandgap excitation stage, the resistance states can be designed by different temperatures, means that multibit programmable thermal RRAM and temperature recognition can be realized below 270 °C.

In intrinsic excitation stage, the bandgap excitation dominates the conductivity, and therefore the current increase. Since HRS cannot be formed at the temperature higher than 270 °C, as shown the 300 and 375 °C testing results in Fig. 2c, the too high temperature is not suitable for information writing.[43]

3.4 Temperature-induced multilevel effect

As seen from Fig. 2a, the conductivity decreases with increasing temperature from RT to 200 °C, indicating that electrons located in deeper traps can be excited at a higher temperature. As seen from Fig. 2a and 10, in addition, the conductivity of device is different after annealing at different temperatures, and furthermore it is strongly dependent of annealing temperature. After applying a relatively high bias voltage, therefore, the HRS of device can be set by annealing at different temperatures. With the increase of annealing

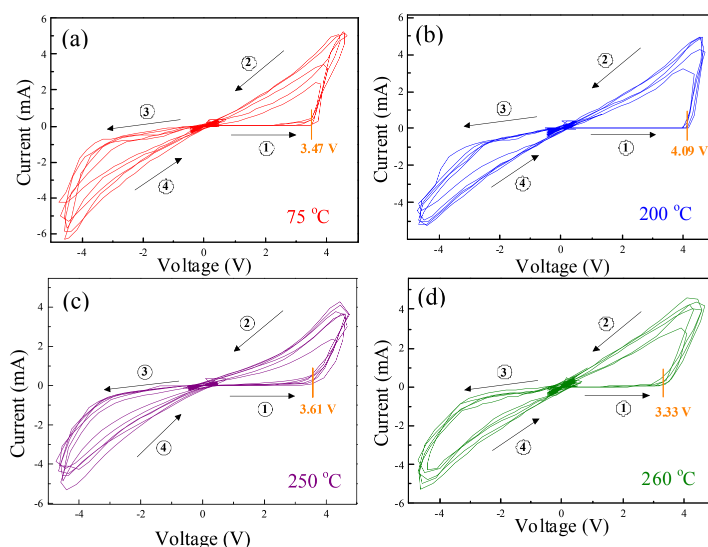


Fig. 9. Cyclic I-V characteristics of read-write-read-erase process, where the write/set temperature are 75 °C (a), 200 °C (b), 250 °C (c) and 260 °C (d), respectively, and the induced HRS is erased by a high voltage with amplitude of 5 V, revealing the temperature dependence of erase switching. The numbers and arrows show the order of voltage sweeping.

Journal of Materials Chemistry C Accepted Manuscript

Please do not adjust margins

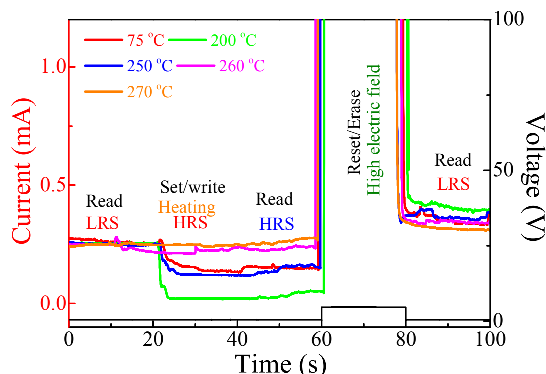


Fig. 10. Temperature dependence of multibit HRS memory effect. The read and set/write operation is carried out at a low bias voltage of 0.5 V, and the reset/erase voltage is 5 V. The color curves correspond to the current response.

temperature, moreover, its conductivity shows a more obvious decrease, indicating the population of trapped electrons decreases dramatically with increasing temperature. After annealing, additionally, the current jumping occurs at different bias voltages, further demonstrating that the annealing temperature determines the concentration of trapped electrons, namely annealing temperature dependence of conduction states. After annealing at different temperatures, therefore, the LRS device can change into different HRS at low operating bias voltage. As seen from Fig. 9, the current of device, annealed at different temperatures, can jump at different voltages, and furthermore they are strongly dependent of the annealed temperatures, revealing the emptied traps are determined by the annealing temperature. Moreover, the voltage of current jumping firstly increase and then decrease with the increase of annealing temperature, which results from the transform of thermal trap excitation-intrinsic bandgap excitation stage. The similar behaviors of RRAM systems can be observed in the work of others.[44,45] Therefore, for the LRS devices applied a relatively high bias voltage, their multibit memory effects can be realized by annealing at different temperatures. The memory properties, operated under different temperatures, have been carried out, as shown in Fig. 10. Owing to the emptied traps are strongly dependent of annealing temperature, the currents of devices are different after erasing by the same high electric field. The trap states of devices are different before heating at high temperature and after applying high electric field, and therefore the LRS before heating is different from that after being subjected to heat treatment and high voltage. It can be seen that the different HRS of the device, subjected to high bias voltage, can be set by annealing at different temperatures, and moreover the change in resistance reaches a maximum after annealing at 200 °C, confirming a nonvolatile multibit temperature memory effect.

3.5 Bias-induced multilevel effect

After annealing at 200 °C, traps can be emptied completely, and correspondingly the device changes into HRS under low operating bias. As seen from Fig. 11, the HRS device, annealed at 200 °C, can change into LRS after applying different bias voltages. Moreover its resistance is strongly dependent of the applied bias voltages, indicating the depth of filled traps increases with increase in bias voltage. For the HRS device annealed at about 200 °C, therefore, its LRS can be set by applying different bias voltages. Higher bias will lead to the filling of deeper traps. Because the definition of 0 and 1 may exchange mutually, the multibit memory performance can be

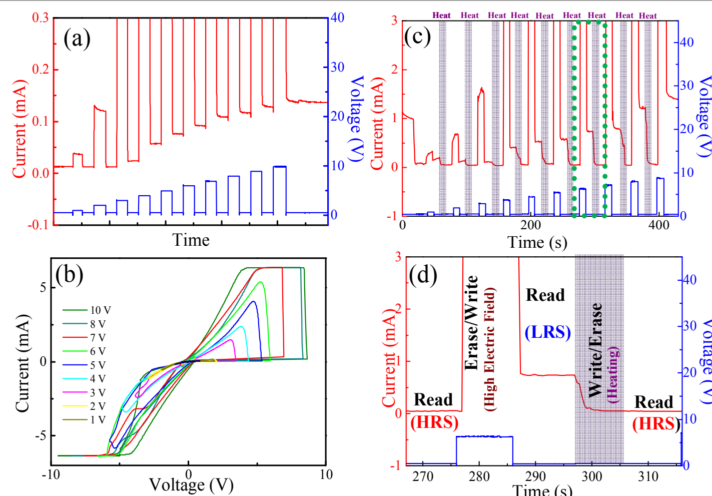


Fig. 11. Voltage dependence of multibit LRS memory effect for the HRS device annealed at 200 °C. (a) After annealing at 200 °C, the recovery of resistance by applying different fixed bias voltages from 1 to 10 V with an interval of 1 V, revealing the bias voltage dependence of the resistance recovery, namely a multibit voltage writing or erasing effect. (b) After annealing at 200 °C, the recovery of resistance by applying a triangle wave voltage with different amplitudes from 1 to 10 V with an interval of 1 V, revealing that the depth of filled traps is dependent of the applied bias voltage. (c) After annealing at 200 °C, the TRAM cell with HRS is subjected to various fixed bias voltages from 1 to 10 V with an interval of 1 V, revealing that the resistance of LRS is strongly dependent of the applied bias voltage. The red curve represents current response and the blue curve corresponds to the applied voltage. (d) The enlarged view of the green dotted frame in (c) shows a detailed read-erase/write-read-write/erase cycle.

This journal is © The Royal Society of Chemistry 20xx

Journal of Materials Chemistry C Accepted Manuscript

Please do not adjust margins

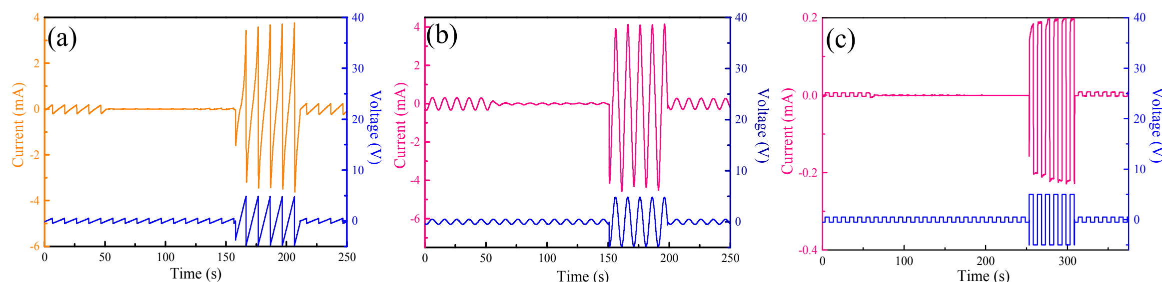


Fig. 12. Memory properties operated under the bias with different wave forms. (a) Saw-tooth wave; (b) sine wave; (c) pulse wave.

written or erased by temperature or bias voltage, respectively. Based on the mechanism of trap modulation, the depth of emptied traps is determined by annealing temperature and the depth of filled traps is determined by applying bias voltage. The two-terminal devices in our research can be used as programmable multibit TRAMs dual-written/erased by temperature or bias voltage, which might be useful in the next generation of functional thermal-electronic circuits. There remain, however, several performance issues that must be resolved if we are to progress with thermal/voltage 'dual-use' memories and, thereby, position them in a distinctive role for multi-functional memories.

Besides for a fixed bias voltage, the memory can similarly be realized under the operation voltage with different wave forms. Fig. 4 and Fig. 12 show the results measured under different wave forms with the same amplitude such as triangle wave, sine wave, saw-tooth wave, and pulse wave. Here, we have attempted to set up new opportunities for RAMs to establish a link between temperature and electricity. Accordingly, this preliminary report of the memory device-featuring multibit data storage capacity, thermal/electronic 'dual-use', and free from the form of working voltage-demonstrates, at the laboratory level, functions of multibit programmable thermal/voltage 'dual-use' memories.

4. Conclusions

In summary, K and Cl-codoped ZnO micro/nanowires were synthesized using a simple carbon thermal reduction. The incorporation of K and Cl leads to the presence of abundant defect traps in ZnO lattice. The individual ZnO:K,Cl micro/nanowire-based device not only shows a negative giant thermalresistance switching effect at the temperature lower than 270 ^{o}C, but shows a novel temperature dependence of trap emptying behavior in the condition of a low operation bias after applying a relatively high bias voltage. Moreover, it shows a bias dependence of trap filling behavior as well in the condition of low operation temperature after annealing at about 200 ^{o}C. Therefore, the micro/nanowire-based two-terminal device can be used as programmable multibit TRAMs dual-written/erased by temperature or drain-source bias. The introduction and modulation of trap states in ZnO nanostructures give a direction to the development of novel nanodevices in repeatable writing/erasing temperature and bias sensors and multibit memories.

Acknowledgements

This work was financially supported by the National Natural Science Foundation of China (51162023, 51462023, 51571107), the Project for Young Scientist Training of Jiangxi Province (20133BCB23002), the Major Program of Natural Science Foundation of Jiangxi Province (20152ACB20010), the Foundation of Jiangxi Educational Commission (GJJ13058), and the Innovation Fund Designated for Graduate Students of Jiangxi Province (YC2015-B002).

References

1 S. Das and J. Appenzeller, *Nano Lett.*, 2011, **11**, 4003.
2 Z. Wang, Y. Zhang, Y. Wang, Y. Li, H. Luo, J. Li and D. Viehland, *ACS Nano*, 2014, **8**, 7793.
3 C. L. Tsai, F. Xiong, E. Pop and M. Shim, *ACS Nano*, 2013, **7**, 5360.
4 B. J. Choi, D. S. Jeong, S. K. Kim, C. Rohde, S. Choi, J. H. Oh, H. J. Kim, C. S. Hwang, K. Szot, R. Waser, B. Reichenberg and S. Tiedke, *J. Appl. Phys.*, 2005, **98**, 033715.
5 L. He, Z. M. Liao, H. C. Wu, X. X. Tian, D. S. Xu, G. L. Cross, G. S. Duesberg, I. V. Shvets and D. P. Yu, *Nano Lett.*, 2011, **11**, 4601.
6 K. Oka, T. Yanagida, K. Nagashima, H. Tanaka and T. Kawai, *J. Am. Chem. Soc.*, 2009, **131**, 3434.
7 W. Wu and Z. L. Wang, *Nano Lett.*, 2011, **11**, 2779.
8 B. Cheng, Z. Ouyang, C. Chen, Y. Xiao and S. Lei, *Sci. Rep.*, 2013, **3**, 3249.
9 M. Cao, B. Cheng, L. Xiao, J. Zhao, X. Su, Y. Xiao and S. Lei, *J. Mater. Chem. C*, 2015, **3**, 5207.
10 K. Oka, T. Yanagida, K. Nagashima, T. Kawai, J. S. Kim and B. H. Park, *J. Am. Chem. Soc.*, 2010, **132**, 6634.
11 K. Nagashima, T. Yanagida, K. Oka, M. Kanai, A. Klamchuen, J. S. Kim, B. H. Park and T. Kawai, *Nano Lett.*, 2011, **11**, 2114.
12 U. Celano, L. Goux, A. Belmonte, K. Opsomer, A. Franquet, A. Schulze, C. Detavernier, O. Richard, H. Bender, M. Jurczak and W. Vandervorst, *Nano Lett.*, 2014, **14**, 2401.
13 Y. Yang, S. Choi and W. Lu, *Nano lett.*, 2013, **13**, 2908.
14 A. Sawa, *Mater. Today*, 2008, **11**, 28.
15 R. Waser and M. Aono, *Nat. Mater.*, 2007, **6**, 833.
16 D. H. Kwon, K. M. Kim, J. H. Jang, J. M. Jeon, M. H. Lee, G. H. Kim, X. S. Li, G. S. Park, B. Lee, S. Han, M. Kim and C. S. Hwang, *Nat. Nanotechnol.*, 2010, **5**, 148.
17 R. Waser, R. Dittmann, G. Staikov and K. Szot, *Adv. Mater.*, 2009, **21**, 2632.
18 M. J. Rozenberg, I. H. Inoue and M. J. Sánchez, *Phys. Rev. Lett.*, 2004, **92**, 178302.

Journal of Materials Chemistry C Accepted Manuscript

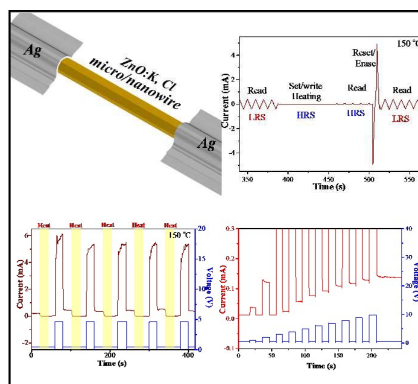
Please do not adjust margins

19 D. C. Kim, S. Seo, S. E. Ahn, D. S. Suh, M. J. Lee, B. H. Park, I. K. Yoo, I. G. Baek, H. J. Kim, E. K. Yim, J. E. Lee, S. O. Park, H. S. Kim, U. I. Chung, J. T. Moon and B. I. Ryu, *Appl. Phys. Lett.*, 2006, **88**, 202102.
20 Y. Gu and L. J. Lauhon, *Appl. Phys. Lett.*, 2006, **89**, 143102.
21 P. Stoliar, L. Cario, E. Janod, B. Corraze, C. Guillot-Deudon, S. Salmon-Bourmand, V. Guiot, J. Tranchant and M. Rozenberg, *Adv. Mater.*, 2013, **25**, 3222.
22 L. Cario, C. Vaju, B. Corraze, V. Guiot and E. Janod, *Adv Mater.*, 2010, **22**, 5193.
23 J. Zheng, B. Cheng, F. Wu, X. Su, Y. Xiao, R. Guo and S. Lei, *ACS Appl. Mater. Inter.*, 2014, **6**, 20812.
24 B. Cheng, G. Wu, Z. Ouyang, X. Su, Y. Xiao and S. Lei, *ACS Appl. Mater. Inter*., 2014, **6**, 4057.
25 B. Cheng, J. Xu, Z. Ouyang, X. Su, Y. Xiao and S. Lei, *J. Mater. Chem. C*, 2014, **2**, 1808.
26 B. Cheng, J. Xu, Z. Ouyang, C. Xie, X. Su, Y. Xiao and S. Lei, *Opt. Express*, 2013, **21**, 29719.
27 L. Ji, Y. F. Chang, B. Fowler, Y. C. Chen, T. M. Tsai, K. C. Chang, M. C. Chen, T. C. Chang, S. M. Sze, E. T. Yu, J. C. Lee, *Nano Lett.*, 2014, **14**, 813.
28 D. Brunel, C. Anghel, D. Y. Kim, S. Tahir, S. Lenfant, A. Filoramo, T. Kontos, D. Vuillaume, V. Jourdain and V. Derycke, *Adv. Funct. Mater.*, 2013, **23**, 5631.
29 S. K. Hwang, I. Bae, S. M. Cho, R. H. Kim, H. J. Jung and C. Park, *Adv. Funct. Mater*., 2013, **23**, 5484.
30 M. P. Lu, M. Y. Lu and L. J. Chen, *Adv. Funct. Mater*., 2014, **24**, 2967.
31 L. W. Feng, C. Y. Chang, T. C. Chang, C. H. Tu, P. S. Wang, Y. F. Chang, M. C. Chen, H. C. Huang, *Appl. Phys. Lett.*, 2009, **95**, 262110.
32 P. Notingher, A. Toureille, J. Santana, L. Martinotto and M. Albertini, *IEEE T. Dielect. El. In.*, 2001, **8**, 972.
33 Y. F. Chang, B. Fowler, Y. C. Chen, Y. T. Chen, Y. Wang, F. Xue, F. Zhou, J. C. Lee, *J. Appl. Phys.*, 2014, **116** (4), 043709.
34 B. R. Huang, C. C. Liao, W. C. Ke, Y. C. Chang, H. P. Huang, N. C. Chen, *J. Appl. Phys.*, 2014, **115**, 113705.
35 R. Maity, S. Kundoo, K. K. Chattopadhyay, *Sol. Energ. Mat. Sol. C.*, 2005, **86**, 217.
36 K. Kim, H. Kang, H. Kim, J. S. Lee, S. Kim, W. Kang, G. T. Kim, *Appl. Phys. A*, 2008, **94**, 253.
37 H. M. Kwon, W. H. Choi, I. S. Han, M. K. Na, S. U. Park, J. D. Bok, C. Y. Kang, B. H. Lee, R. Jammy, H. D. Lee, *Microelectron. Eng*., 2011, **88**, 3399.
38 V. A. Karpyna, A. A. Evtukh, M. O. Semenenko, V. I. Lazorenko, G. V. Lashkarev, V. D. Khranovskyy, R. Yakimova, D. A. Fedorchenko, *Microelectron. J.,* 2009, **40**, 229.
39 R. S. Knox, *J. Am. Chem. Soc.*, 1961, **83**, 3923.
40 J. D. Prades, F. Hernandez-Ramirez, R Jimenez-Diaz, M Manzanares, T. Andreu, A. Cirera, A. Romano-Rodriguez and J. R. Morante, *Nanotechnology*, 2008, **19**, 465501.
41 T. E. Murphy, K. Moazzami and J. D. Phillips, *J. Electron. Mater.*, 2006, **35**, 543.
42 J. D. Prades, F. Hernandez-Ramirez, R. Jimenez-Diaz, M. Manzanares, T. Andreu, A. Cirera, A. Romano-Rodriguez, and J. R. Morante, *Nanotechnology*, 2008, **19**, 465501.
43 E. Liu, B. Zhu, J. Luo, The Physics of Semiconductors, 7th Edition (Publishing House of Electronics Industry), p.227.
44 Y. F. Chang, P. Y. Chen, B. Fowler, Y. T Chen, F. Xue, Y. Wang, F. Zhou, J. C. Lee, *J. Appl. Phys.*, 2012, **11**, 123702.
45 Y. F. Chang, T. C. Chang, C. Y. Chang, *J. Appl. Phys*., 2011, **110**, 053703.

Journal of Materials Chemistry C Accepted Manuscript

 This journal is © The Royal Society of Chemistry 20xx

Nonvolatile multibit sensors and memories, which are written/erased by different temperatures or bias voltages, are realized successfully in two-terminal devices based on individual ZnO:K,Cl micro/nanowires. The modulation of trap states in nanostructures gives a direction to the development of novel nanodevices in rewritable temperature information sensor and memory.



Journal of Materials Chemistry C Accepted Manuscript