



**Carrier confinement effect-driven channel design and achievement of robust electrical/photo stability and high mobility in oxide thin-film transistors**

Journal:	<i>Journal of Materials Chemistry C</i>
Manuscript ID	TC-ART-11-2015-003766
Article Type:	Paper
Date Submitted by the Author:	19-Nov-2015
Complete List of Authors:	Ahn, Cheol Hyoun; Sungkyunkwan University, School of Advanced Materials Science and Engineering Cho, Hyung Koun; Sungkyunkwan University, School of Advanced Materials Science and Engineering Kim, Hyongsu; Sungkyunkwan University, School of Advanced Materials Science and Engineering



## ARTICLE

## Carrier confinement effect-driven channel design and achievement of robust electrical/photo stability and high mobility in oxide thin-film transistors

Received 00th January 20xx,  
Accepted 00th January 20xx

DOI: 10.1039/x0xx00000x

www.rsc.org/

Cheol Hyoun Ahn, Hyung Koun Cho,\* and Hyoungsub Kim

Oxide thin-film transistors (TFTs) with high electrical performance, high electrical/photo stability, and low process temperature capabilities are required to realize next-generation display application. However, commercial available oxide-based TFTs shows a high degree of instability under simultaneous photo-illumination and bias stress conditions, which is related to hole trapping, ambient interactions, and photo-ionization of oxygen vacancy defects. This study the realization of high performance, electrical/photo stable oxide-based TFTs fabricated at low process temperatures (~200 °C) using carrier confinement effect-driven ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice channel structure. ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice structures drive high mobility (>25 cm<sup>2</sup>/Vs) by enhancing electrical conductivity along the planar direction. Also, carrier confinement effect-driven channel structure promoted recombination events between photo-ionized oxygen vacancies and the photo-charged electrons due to effective carrier confinement, resulting in extremely high stability ( $\Delta V_{th} \leq -0.7$  V) under negative gate bias temperature illumination stress conditions, even at low process temperatures. Our channel design is a promising approach for producing highly photo-stable TFTs for the next-generation displays.

### Introduction

Transparent/flexible electronics have received a great deal of interest recently due to their broad range of applications in information displays/storage, physical/chemical/bio-sensors, lighting, photovoltaics, and batteries.<sup>1-5</sup> Traditionally used Si-based devices have reached technical limits for use as an active semiconductor layer in some field, because of their narrow band-gap, rigidity, brittleness, and high processing temperature. Alternatively, organic semiconductors have been suggested as appropriate materials due to their low cost, inherently low temperature, and mechanical flexibility. However, they have some considerable weaknesses with respect to their use in transparent/flexible electronics including low thermal/chemical stability and low mobility.<sup>1,6,7</sup> On the other hand, the oxide-based semiconductors have gained special attention as a promising alternative material to amorphous Si and organic semiconductors because of their high mobility, low production cost, low temperature processing capability, and transparency in the visible region ( $E_g > 3.2$  eV).<sup>1,8,9</sup> In particular, multicomponent oxide semiconductors, such as InZnO,<sup>10</sup> InGaZnO,<sup>1</sup> and ZnSnO,<sup>11</sup> have been studied as a channel layer of thin-film transistors (TFTs) for

next-generation displays. Oxide-based TFTs have been applied as switching/driving devices in active-matrix backplanes for many prototype displays,<sup>12</sup> such as organic light emitting diodes, liquid crystal displays, and e-paper. In addition, Salvatore et al.<sup>13</sup> recently reported the feasibility of extremely flexible and transparent electronics using oxide semiconductors. Nevertheless, the long-term instability of oxide-based TFTs is still one of the most critical issues under various operating conditions such as bias,<sup>14-16</sup> temperature,<sup>17</sup> and illumination stress.<sup>18-20</sup>

The electrical degradation of oxide TFT devices is attributed to the sub-gap density of states in oxide semiconductor layers, which is mainly related to oxygen vacancies with the smallest formation energy.<sup>21,22</sup> Many research groups have suggested various origins for the instability of oxide TFTs under various stress conditions.<sup>20,22,23</sup> Oxygen vacancy ( $V_O$ ) related defects have an energy level near 1 eV above the valence band, and can be activated even under visible light ( $\geq 2$  eV). The photo-ionization process of oxygen vacancies ( $V_O$ ) into  $V_O^+/V_O^{2+}$  by visible light donates one/two free electrons to the channel layer. Thus, large oxide TFT instability has been observed under a negative gate bias illumination temperature stress (NBITS). Moreover, the photo-induced current makes the oxide semiconductors conductive several days after turning off the light. As a result, many studies have been devoted to suppressing oxygen vacancies by the incorporation of metal cations (stabilizer) with a high oxygen-bonding ability in oxide semiconductors, and the optimization of growth conditions and post-annealing methods.<sup>24-28</sup> Although these efforts provide improved stability with reduced  $V_O$ , the resulting TFTs inevitably suffer from reduced field effect mobility ( $\mu_{FE}$ ).

School of Advanced Materials Science and Engineering, Sungkyunkwan University, 2066 Seobu-ro, Jangan-gu, Suwon, Gyeonggi-do, 440-746, Republic of Korea. E-mail: chohk@skku.edu; Tel: +82-31-299-7364

† Footnotes relating to the title and/or authors should appear here.

† Electronic Supplementary Information (ESI) available: [details of any supplementary information available should be included here]. See DOI: 10.1039/x0xx00000x

Currently, the main research on the oxide TFTs is focused on achieving good mobility/stability at lower process temperatures for flexible/transparent applications. The design of artificially controlled channel layers, such as bi-/multi-layers<sup>29-31</sup> and superlattice structures,<sup>32</sup> has provided new potential for simultaneously obtaining high mobility and high stability. Since the trade-off between electrical mobility and photo-stability is unavoidable, several groups have attempted to develop photo-stable channels using a bi-layer structure, including a high conducting layer (In-Zn-O In-Sn-O) and a relatively stable additional layer. Recently, we firstly proposed a ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice channel consisting of a semiconductor and insulator and obtained high mobility.<sup>32</sup> In this structure, the electrons were effectively confined in the potential well of ZnO due to the high conduction band offset ( $\Delta E_C = 1.71 \sim 2.46$ ) between ZnO (the well layer) and Al<sub>2</sub>O<sub>3</sub> (the barrier layer). Thus, the stacked superlattice film is expected to induce charge transport along the in-plane direction due to the quasi-two-dimensional nature of the charges confined in the well layer.

Here, we report a carrier confinement effect driven-channel design by depositing different Al<sub>2</sub>O<sub>3</sub> barrier thicknesses, and we achieve robust electrical and photo stability as well as high mobility in oxide TFTs. In particular, the maximum process temperature used in this experiment is quite low (200 °C), compared to other chemical vapor deposition or sputtering processes requiring high-temperature post-thermal annealing. Superlattice TFTs show a  $\mu_{FE}$  of  $> 25 \text{ cm}^2/\text{Vs}$ , which is the highest value reported for binary ZnO transistors fabricated at  $\leq 200 \text{ }^\circ\text{C}$  to the best of our knowledge. Also, superlattice TFTs with suitable barrier thickness exhibit excellent robust electrical and photo stability under NBITS along with high  $\mu_{FE}$ . In this work, we illustrate the mechanism of high performance in oxide TFTs with a well-designed superlattice channel.

## Experimental

The ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice films were deposited by atomic layer deposition (ALD) at 150 °C. High-purity diethylzinc (DEZn), trimethylaluminium (TMA), and deionized water were used as precursors for zinc, aluminum, and oxygen, respectively. The temperatures of the cooling circulators for DEZn, TMA, and deionized water were 10 °C. These precursors were injected directly into the reaction chamber using nitrogen carrier gas with a flow rate of 100 sccm, which was also used as a purging gas. One cycle for film deposition consisted of exposure to DEZn (or TMA) (0.1 s), a 10 s purge, exposure to H<sub>2</sub>O (0.1 s), and a 10 s purge. The growth rates of the ZnO and Al<sub>2</sub>O<sub>3</sub> layers were  $\sim 1.5 \text{ \AA}/\text{cycle}$  and  $\sim 1.0 \text{ \AA}/\text{cycle}$ , respectively. The ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice channels were composed of Al<sub>2</sub>O<sub>3</sub>/ZnO/Al<sub>2</sub>O<sub>3</sub>/ZnO/Al<sub>2</sub>O<sub>3</sub>/ZnO/Al<sub>2</sub>O<sub>3</sub>, as shown in Fig. 1 (a). In the superlattice structure, the thickness of the ZnO layer was  $\sim 50 \text{ \AA}$ , and the Al<sub>2</sub>O<sub>3</sub> layers had the thickness of  $13 \sim 108 \text{ \AA}$ . The ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice channels deposited on SiO<sub>2</sub>/Si substrate by ALD were defined by conventional lithography and a wet etching process using H<sub>3</sub>PO<sub>4</sub>. Then, the source and drain regions were formed by depositing Ti (30 nm)/Au (70 nm) bi-layer

electrodes with an e-beam evaporator. The width/length of the channel was 500  $\mu\text{m}/50 \mu\text{m}$ . TFT devices were annealed at 200 °C in an O<sub>2</sub> atmosphere for 2 hours. To analyse charge transport along the out-of-plane direction of the superlattice, the ITO/glass and the top-contact metal (Ti/Au) were used as the bottom and the top electrodes, respectively, as shown in Fig. 1(a). The in-plane current flow in the superlattice was characterized on the patterned superlattice films with vertical current blocking layer (Al<sub>2</sub>O<sub>3</sub> = 20 nm). Here, two Ti/Au electrodes were deposited on superlattice with shadow mask by e-beam evaporator.

The electrical properties of the superlattice films and TFT devices were measured using an HP4145B semiconductor parameter analyzer. The field effect mobility ( $\mu_{FE}$ ) in the TFT devices was determined by the maximum transconductance at a drain voltage of 0.1 V. The sub-threshold-swing (SS) was extracted from the equation,  $SS = (dV_g/d\log I_{ds})$ , in the linear region. The threshold voltage ( $V_{th}$ ) was determined as the gate voltage at a drain current of  $L/W \times 10 \text{ nA}$ . For light illumination, a 150 W Xe arc lamp and a monochromator were used. The optical power of the monochromatic light was calibrated using a UV-enhanced Si detector and was controlled to be  $0.1 \text{ mW}/\text{cm}^2$  in the green wavelength (2.25 eV).

## Results and discussion

### Electrical properties of ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice

Figure 1 shows the J-V curves along the in-plane and the out-of-plane directions as a function of Al<sub>2</sub>O<sub>3</sub> thickness in the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattices. These current densities have quite different barrier thickness dependency with respect to the current direction. The planar current density continuously increases with barrier thickness, but the vertical current density exhibits an inverse trend. From a quantum mechanical point of view, the increase in the barrier thickness induces an enhancement in electron carrier confinement inside each narrow band gap well due to the loose overlap between the adjacent electron wave functions in the well and the large barrier height in the conduction band, as shown in the schematic diagram of Fig. 1(b). Also, if the barrier width in the conduction band is sufficiently narrow, electrons under an applied bias can tunnel through an insulating barrier directly despite the high barrier height, indicating field-emission-type current flow. Thus, a slight reduction in the vertical current level is observed up to a barrier thickness of 36  $\text{\AA}$  [Fig. 1(d)]. On the contrary, the planar current density is continuously enhanced with increasing Al<sub>2</sub>O<sub>3</sub> barrier thickness due to the strong carrier confinement of electrons, as shown in Fig. 1(c). If the wave functions of electrons are wider than the barrier width, it might be possible for the electrons to appear in the both sides of the barrier. Otherwise, these electrons are strongly localized in a well region and carrier transport is primarily via two-dimensional (2D)-like lateral components, as indicated by arrows in Fig. 1(b). The current path of an electron along the in-plane direction will be affected by both well and barrier layers due to the overlapping electron wave functions. Thus, the current flow behavior observed in the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice along the planar

direction can be explained by stronger carrier confinement with increasing barrier thickness. On the other hand, the vertical current density along the out-of-plane direction is related to the probability of quantum tunneling, as indicated by arrows in Fig. 1(b).

#### Thin-film transistor using ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice channels

Oxide TFTs were fabricated using these ZnO/Al<sub>2</sub>O<sub>3</sub> superlattices as channel layers, and Figs. 2(a) and (b) are transfer curves and figures-of-merit, respectively, for ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs with varying barrier thickness. The threshold voltage ( $V_{th}$ ) was determined as the gate voltage at a drain current of  $L/W \times 10$  nA. The field effect mobility ( $\mu_{FE}$ ) of the TFT devices was calculated from transfer curve measured at a drain voltage of 0.1 V by the following equation,

$$\mu_{FE} = (L_{ch}/W_{ch}) [1 / ((C_i \cdot V_{DS}) / (dI_{DS}) / (dV_{GS}))] \quad (1)$$

Despite its ultra-thin barrier, the field effect mobility ( $\mu_{FE}$ ) of the superlattice TFT with the smallest barrier thickness of 13 Å is 6.5 cm<sup>2</sup>/Vs, which is higher than that of the single ZnO channel (~ 4 cm<sup>2</sup>/Vs).<sup>32</sup> As shown in Figs. 2(a) and (b), the on-current and mobility of the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs are considerably enhanced by increasing barrier thickness ( $\geq 72$  Å), although the current density out-of-plane in the superlattice structure is reduced. Interestingly, these on-current levels show similar trends with current flow along the in-plane direction in the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattices showing the dominant electron confinement in the well layers. Superlattice TFTs have shown average  $\mu_{FE}$  values of  $28 \pm 3$  cm<sup>2</sup>/Vs for a barrier thickness of 36 Å and  $35 \pm 3$  cm<sup>2</sup>/Vs for a barrier thickness of 72 Å, despite the low process temperature of 200 °C. This indicates that the on-current and  $\mu_{FE}$  in the superlattice TFTs are mostly determined by the electrical conductivity along the 2D-like planar direction in the conducting well layers with a narrow band gap. However, the superlattice TFT with a barrier thickness of 108 Å does not show typical I-V performance due to significantly reduced tunneling transport along the vertical direction, as shown figure 2(a). In addition, the off-current level ( $I_{off}$ ) of the superlattice TFTs rises with the increasing barrier thickness together with a negative shift in the  $V_{th}$ . These results on  $\mu_{FE}$ ,  $V_{th}$ , and  $I_{off}$  are attributed to an increase in mobile carrier density along the in-plane direction of the superlattice channels.

Figures 3(a) and (b) show the out-put curves of the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs as a function of Al<sub>2</sub>O<sub>3</sub> thickness. The superlattice TFTs with relatively thin Al<sub>2</sub>O<sub>3</sub> barrier thickness (13~36 Å) exhibited general transistor characteristics. However, abnormal out-put behavior is observed in superlattice TFTs with barrier thicknesses of 72 and 108 Å. Here, a negative differential resistance (NDR) is detected in the out-put curves under different gate voltages, as shown in Fig. 3(b). Recently, it was reported that GaAs/AlGaAs based field-effect transistors show an N-shaped NDR characteristic by real space transfer behavior, where the electrons have sufficient energy to overcome the band offset in the conduction band by application of a large gate bias parallel the layer interface.<sup>33,34</sup> As a result, some electrons were injected into the adjacent barrier layers with low conductivity, and the contribution of electrical conduction

along the well layers was reduced, inducing an N-shaped NDR in the I-V output characteristics. Thus, the NDR behavior is observed for lower drain voltages with increasing gate bias. However, the drain voltage showing the NDR characteristic in our ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs is independent of gate voltage, and also exhibits interesting multi-NDR properties, as shown in Fig. 3(b). Moreover, the band offset in the ZnO/Al<sub>2</sub>O<sub>3</sub> may not be negligible, and thus a real space transition is unexpected.

Alternatively, another mechanism for NDR phenomena observed at low bias was suggested in high quality, epitaxially grown ZnO/MgZnO heterostructures,<sup>35</sup> and GaAs/AsGaAs<sup>36</sup> or InP/InGaAs<sup>37</sup> superlattice structures, where the NDR occurs due to resonant tunneling process. Also, a-Si:H/a-SiC:H quantum well structures<sup>38</sup> and Si nanocrystals embedded in an amorphous Al<sub>2</sub>O<sub>3</sub> film<sup>39</sup> showed the NDR characteristics by resonant tunneling. When the energy levels between quantized states in the conduction band of the wells match each other, it is expected that the tunneling probability is sharply increased by the resonance of the wave function. Figures 3(c) and (d) shows  $dI_D/dV_D$  versus  $V_D$  data obtained from the out-put curves of the superlattice TFTs with barrier thicknesses of 36 Å and 72 Å, respectively. Two NDR regions are observed at drain voltage of 1~3.4 V and 16.4~24.9 V for a barrier thickness of 72 Å. In addition, the NDR characteristic was strengthened with an increase of gate voltage. In the bottom-gate TFT devices with top-contact, the current path of electrons along the out-of-plane direction was affected by both drain and gate voltages due to the formation of a vertical field. Consequently, the NDR characteristics in ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs are attributed to resonant tunneling. On the contrary, the NDR characteristic is indistinguishable in the output curves of superlattice TFTs with thin barrier thickness, as shown figure 3. The carriers in well layers with a thin Al<sub>2</sub>O<sub>3</sub> barrier layer can easily migrate due to direct tunneling by a strong overlap between the adjacent electron wave functions in the well. Therefore, it could be difficult for superlattice TFTs with thin Al<sub>2</sub>O<sub>3</sub> barrier layer to exhibit the NDR characteristic due to non-resonance tunneling transport.

#### Photo-bias stability of ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs.

To realize the robust channel structure with retaining its high  $\mu_{FE}$ , temperature stress (TS) and NBITS tests for comparative analysis of device stability were conducted for the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs with different barrier thicknesses. First, the instability of the temperature stress on the transfer characteristics of superlattice TFTs was examined. Figure 4 shows the variation of the transfer curves of the superlattice TFTs as a function of measurement temperature. Generally, the  $V_{th}$  of TFT devices was negatively shifted with increasing temperature, which was attributed to the generation of thermally activated free carriers from deep level trap sites.<sup>17,40,41</sup> The ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs similarly show low  $V_{th}$  shift ( $\leq 1.1$  V) in the TS test, despite different barrier thickness, as shown in Fig. 4. This assumed that the total charge trap density of the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs is irrelevant to the barrier thickness.

The NBITS tests were also conducted for comparative instability analysis of the superlattice TFTs with different barrier thicknesses. The stress condition of gate bias was normalized as

$V_{\text{str}}-V_{\text{th}} = -30$  V was applied to TFT devices at 60 °C for 2 hours. A green light (2.25 eV) with a power density of 0.1 mW/cm<sup>2</sup> was simultaneously illuminated in the TFT devices. The variation of  $V_{\text{th}}$  shift for the superlattice TFTs is shown as a function of stress time in Figs. 5(a)-(d). Surprisingly, the  $\Delta V_{\text{th}}$  of the superlattice TFTs under NBITS was considerably reduced with increasing barrier thickness, while the superlattice TFT with a thin barrier (13 Å) show huge  $V_{\text{th}}$  shift. The superlattice TFT with a barrier thickness of 36 Å exhibits highly robust electrical stability, with  $\Delta V_{\text{th}}$  below -0.7 V and no change in the SS values for 2 hours, despite simultaneous temperature, illumination, and bias stress. Generally, ZnO semiconductors are very sensitive to light illumination above 2 eV and produce high photo-current, since the existing defect levels related to oxygen vacancies are located about 1 eV above the valence band.<sup>21</sup> The photosensitivity (P) in our TFT devices is compared by using the following expression,

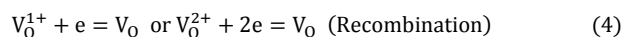
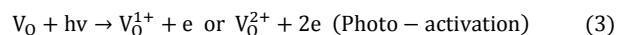
$$P = I_{\text{Ph}}/I_{\text{DS,dark}} = (I_{\text{DS,illumination}} - I_{\text{DS,dark}})/I_{\text{DS,dark}} \quad (2)$$

Where  $I_{\text{DS,illumination}}$  and  $I_{\text{DS,dark}}$  are the drain current under the illumination and the dark, respectively, at a fixed gate bias of 30 V. As shown in Fig. 5(e), the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFT with a barrier thickness of 36 Å demonstrate suitable NBITS stress without significant photosensitivity. This indicates that the formation of photo-generated carriers in the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice can be extremely suppressed with increasing barrier thickness.

Plausible mechanisms proposed for the negative  $V_{\text{th}}$  shift of oxide TFTs under NBITS are to i) charge trapping/injection of holes in the gate-interface or within the dielectric layer,<sup>14,15</sup> ii) photo-desorption of ionized oxygen molecules adsorbed on the surface of back channel,<sup>16</sup> and iii) transition of neutral oxygen [ $V_{\text{O}}$ ] to [ $V_{\text{O}}^{1+}/V_{\text{O}}^{2+}$ ] charged states by photo-illumination.<sup>20</sup> The sub-gap states in the ZnO-based semiconductors originated from oxygen vacancies ( $V_{\text{O}}$ ), according to first principle calculations<sup>21</sup> and various experimental analyses.<sup>42-44</sup> The  $V_{\text{O}}$  in the ZnO layers can be photo-excited into  $V_{\text{O}}^{1+}/V_{\text{O}}^{2+}$  energy levels under a photon energy above ~ 2 eV, and they thereby donate one/two carrier electrons for electrical conduction. These ionized oxygen vacancies can easily migrate to the gate insulator/semi-conductor interface by means of the gate field, and the photo-generated electrons can freely contribute to charge carriers, as shown in Fig. 6(a). Thus, the huge negative  $V_{\text{th}}$  shift of the oxide TFT has been explained based on the energy level transition of neutral oxygen defects. In the previous study,<sup>32</sup> we reported that the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs exhibited higher stability under positive/negative gate bias stress than the single ZnO TFT due to the low defect density in the superlattice channel. Also, entire surface of the channel structure is finished with the Al<sub>2</sub>O<sub>3</sub> layer suppress the backchannel effect. Thus, hole trapping at the gate dielectric interface or photo-desorption of oxygen molecules at the back surface can be dismissed as the origin for  $V_{\text{th}}$  variation induced by NBITS in the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs with different barrier thicknesses.

The TFT with a barrier thickness of 13 Å exhibits at substantial degradation of SS from 0.27 to 3.92 V/dec. during 2 hour NBITS test. The SS is used as a reference value to evaluate device stability, which is related to the total charge trap density in the bulk channel layer or at the interface between the channel and dielectric layers.

Therefore, it is expected that the degraded SS under NBITS is mainly attributed to the defects photo-generated in the ZnO well layers. On the other hand, the photo-ionized oxygen vacancies can be neutralized to  $V_{\text{O}}$  again by a recombination process with the photo-generated electron or intrinsic electrons, as per the following equations:



Thus, in order to achieve improved mobility and photo-stability in the oxide TFT devices, two viewpoints can be considered: i) the suppression of oxygen-related defect density and ii) the fast relaxation of ionized-defect states produced in oxide layers by illumination. Unfortunately, the oxide TFTs incorporating stabilizers such as Hf and Zr were associated with reduced mobility,<sup>25,28</sup> which may be ascribed to the increased carrier scattering by adding impurities and the reduced effective carrier density. If fast recombination of photo-activated charges can occur in the oxide layers, it is expected that the NBITS related photo-stability of oxide-based TFTs can be significantly improved. It is well known that the photo-ionized oxygen vacancies in the oxide layers remained as unoccupied states by virtue of lowering of the Fermi level by an applied negative gate bias. Then, these ionized-oxygen vacancies were rapidly separated from the photo-generated electrons and moved to the gate dielectric/channel interface by a negative gate field. As a result, the accumulation of photo-ionized oxygen vacancies with positive charge near the interface caused downward band bending [Fig. 6(a)], and led to the enormous negative shift in  $V_{\text{th}}$  position, as shown in Figs. 5(a) and (b). Unfortunately, this process suppresses the frequency of recombination events between positive  $V_{\text{O}}^{2+}$  ions and negatively charged electrons due to charge separation by negative gate bias, even after turning off the light, resulting in delayed recovery. Recently, Jeon et. al.<sup>45</sup> reported that the photo-degraded oxide TFTs under NBITS could be promptly recovered by promoting the recombination rate between electron and ionized oxygen vacancies, where a positive gate pulse induced upward band bending. This approach could be applied to optical sensors for contact-free interactive displays or remote control of touch using oxide-based TFT devices. Consequently, this implies that the channel structure, which induces frequent recombination events in the oxide semiconductors, can be considered one of the key concepts to achieve robust photo-stability of oxide TFTs. For the channel design of the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice, the barrier layer with a wide band gap will obstruct the migration of photo-ionized oxygen vacancy defects to the gate dielectric interface, as shown in Figs. 6(b) and (c). Also, the charged electrons in the conduction band experience an identical situation. Thus, the photo-ionized oxygen vacancies will be distributed evenly in all of the well layers even under a negative gate field if the barrier layers are of suitable thickness. As explained, the tunneling of photo-generated charged carriers along the vertical direction in the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice will be suppressed by an increase in barrier thickness due to effective carrier confinement, as shown in Fig. 6(c). As a result, the recombination probability between photo-ionized oxygen vacancies and charged electrons (intrinsic or photo-generated electrons) can

be considerably promoted by increasing barrier thickness, resulting in robust photo-stability under NBITS testing, as shown in Figs. 5(c) and 6. Hence, the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice channel with well-defined interfaces and appropriate thickness can achieve a good  $\mu_{FE}$  value and a great enhancement in photo/electrical stability at the same time.

## Conclusions

In conclusion, we have proposed an oxide channel structure that results in great enhancement of photo/electrical stability as well as a high field effect mobility ( $>25 \text{ cm}^2/\text{Vs}$ ), where the channel layers consisted of a ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice with well-defined interfaces grown by ALD. To survey the confinement effect of the charged carriers in the superlattice with a large band offset, the barrier Al<sub>2</sub>O<sub>3</sub> layers with different thicknesses were deposited with the same ZnO thickness. The field effect mobility and threshold voltage of the superlattice TFTs strongly depended on electrical conductivity along the 2D-like planar direction due to the confinement of carriers along the vertical direction, resulting in a high mobility of  $>25 \text{ cm}^2/\text{Vs}$  in the samples with barrier thicknesses of 36 Å and 72 Å. In addition, the increase in barrier thickness in the superlattice accompanied a great enhancement in electrical/photo stability under NBITS, which was attributed to increased recombination events between photo-ionized oxygen vacancies and charged electrons due to effective carrier confinement.

## Acknowledgements

This work was supported by the Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2013R1A1A2063631) and Basic Research Lab. project of the Korea government (MSIP) (2014R1A4A1008474).

## Notes and references

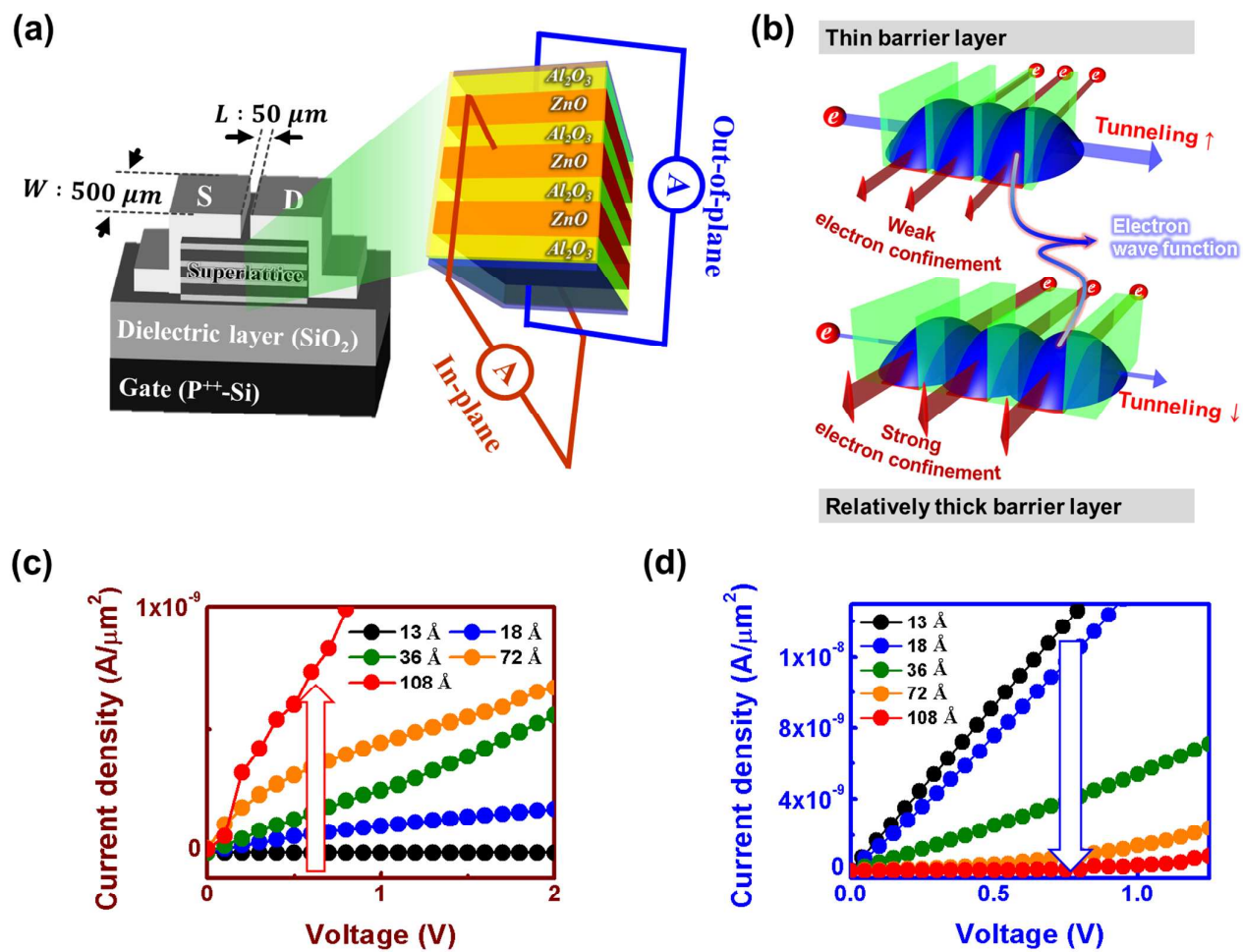
- Y. Sun, J. A. Roger, *Adv. Mater.* 2007, **19**, 1897-1916.
- S. M. Paek, E. J. Yoo, I. Honma, *Nano Lett.* 2009, **9**, 72-75.
- M. Kaltenbrunner, T. Sekitani, J. Reeder, T. Yokata, K. Kuribara, T. Tokuhara, M. Drack, R. Schwodiauer, I. Graz, S. Bauer-Gogonea, S. Bauer, T. Someya, *Nature* 2013, **499**, 458-463.
- J. T. Mabeck, G. G. Malliars, *Anal. Bioanal. Chem.* 2006, **384**, 343-53.
- T. Suga, H. Ohshiro, S. Sugita, K. Oyaizu, H. Nishide, *Adv. Mater.* 2009, **21**, 1627-1630.
- U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, K. Kern, H. Klauk, *Adv. Mater.* 2010, **22**, 982-985.
- K. Kuribara, H. Wang, N. Uchiyama, K. Fukuda, T. Yokota, U. Zschieschang, C. Jaye, D. Fischer, H. Klauk, T. Yamamoto, K. Takimiya, M. Ikeda, H. Kuwabara, T. Sekitani, Y. Loo, T. Someya, *Nature communications* 2012, **3**, 723.
- K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hosono, *Nature* 2004, **432**, 488-482.
- S. K. Park, C. Hwang, M. Ryu, S. Yang, C. Byun, J. Shin, J. Lee, K. Lee, M. S. Oh, S. Im, *Adv. Mater.* 2009, **21**, 678-682.
- E. Fortunato, P. Barquinha, G. Goncalves, L. Pereira, R. Martins, *Solid-State Electron.* 2008, **52**, 443-448.
- H. Q. Chiang, J. F. Wager, R. L. Hoffman, J. Jeong, D. A. Keszler, *Appl. Phys. Lett.* 2005, **86**, 013503.
- T. Kamiya, K. Nomura, H. Hosono, *Sci. Technol. Adv. Mater.* 2010, **11**, 044305.
- G. A. Salvatore, N. Munzenrieder, T. Kinkeldei, L. Petti, C. Zysset, I. Strebel, L. Buthe, G. Troster, *Nat. Commun.* 2014, **5**, 2982.
- J. Lee, I. Cho, J. Lee, H. Kwon, *Appl. Phys. Lett.* 2008, **93**, 093504.
- A. Suresh, J. F. Muth, *Appl. Phys. Lett.* 2008, **92**, 033502.
- J. K. Jeong, H. W. Yang, J. H. Jeong, Y. Mo, H. D. Kim, *Appl. Phys. Lett.* 2008, **93**, 123508.
- M. D. H. Chowdhury, P. Migliorato, J. Jang, *Appl. Phys. Lett.* 2011, **98**, 153511.
- P. Görrn, M. Lehnhardt, T. Riedl, W. Kowalsky, *Appl. Phys. Lett.* 2007, **91**, 193504.
- K. Takechi, M. Nakata, T. Eguchi, H. Yamaguchi, S. Kaneko, *Japan. J. Appl. Phys.* 2009, **48**, 010203.
- J. Kwon, J. S. Jung, K. S. Son, K. Lee, J. S. Park, T. S. Kim, J. Park, R. Choi, J. K. Jeong, B. Koo, S. Y. Lee, *Appl. Phys. Lett.* 2010, **97**, 183503.
- A. Janotti, C. G. Van de Walle, *Prog. Phys.* 2009, **72**, 126501.
- B. Ryu, H. Noh, E. Choi, K. J. Chang, *Appl. Phys. Lett.* 2010, **97**, 022108.
- J. Yao, N. Xu, S. Deng, J. Chen, J. She, H. D. Shieh, P. Liu, Y. Huang, *IEEE Trans. Electron Devices* 2011, **4**, 1121-1126.
- T. Iwasaki, N. Itagaki, T. Den, H. Kumomi, K. Nomura, T. Kamiya, H. Hosono, *Appl. Phys. Lett.* 2007, **90**, 242114.
- C. Kim, S. Kim, J. Lee, J. J. Park, S. Kim, J. Park, E. Lee, Y. Park, J. H. Kim, S. T. Shin, U. Chung, *Appl. Phys. Lett.* 2009, **95**, 252103.
- J. Park, K. Kim, Y. Park, Y. Mo, H. D. Kim, J. K. Jeong, *Adv. Mater.* 2009, **21**, 329-333.
- K. Nomura, T. Kamiya, M. Hirano, H. Hosono, *Appl. Phys. Lett.* 2009, **95**, 013502.
- S. Yang, K. H. Ji, U. K. Kim, C. S. Hwang, S. K. Park, C. Hwang, J. Jang, J. K. Jeong, *Appl. Phys. Lett.* 2011, **99**, 102103.
- J. Kim, J. H. Ji, H. Y. Jung, S. Y. Park, R. Choi, M. Jang, H. Yang, D. Kim, J. Bae, C. D. Kim, J. K. Jeong, *Appl. Phys. Lett.* 2011, **99**, 122102.
- C. H. Ahn, M. F. Yun, S. T. Lee, H. K. Cho, *IEEE Trans. Electron Devices* 2014, **61**, 73-78.
- H. Kim, J. S. Park, H. Jeong, K. Son, T. S. Kim, J. Seon, E. Lee, J. G. Chung, D. H. Kim, N. Ryu, S. Y. Lee, *ACS Appl. Mater. Interfaces* 2012, **4**, 5416-5421.
- C. H. Ahn, K. Senthil, H. K. Cho, S. Y. Lee, *Sci. Rep.* 2013, **3**, 2737.
- Y. Li, S. Wang, X. Xu, W. Liu, Y. Chen, *J. J. Appl. Phys.* 2010, **49**, 104002.
- R. Liu, W. Liu, *Microelectron. Reliab.* 1998, **38**, 367-372.
- S. Krishnamoorthy, A. A. Iliadis, A. Inumpudi, S. Chopun, R. D. Vispute, T. Venkatesan, *Solid-state Electron.* 2002, **46**, 1633-1637.
- R. A. Deutschmann, W. Wegscheider, M. Rother, M. Bichler, G. Abstreiter, *Appl. Phys. Lett.* 2011, **99**, 1564.
- W. Wang, H. Pan, K. Thei, K. Lin, K. Yu, C. Cheng, L. Lai, S. Cheng, W. Liu, *Semicond. Sci. Technol.* 2000, **15**, 935-940.
- Y. Jiang, H. Hwang, *IEEE Trans. Electron Devices* 1989, **36**, 2816.
- Q. Wan, T. H. Wang, M. Zhu, C. L. Lin, *Appl. Phys. Lett.* 2002, **81**, 538.

## ARTICLE

Journal of Materials Chemistry C

- 40 K. H. Ji, J. Kim, Y. Jung, S. Y. Park, Y. Mo, J. H. Jeong, J. Kwon, M. Ryu, S. Y. Lee, R. Choi, J. K. Jeong, *J. Electrochem. Soc.* 2010, **157**, H983-H986
- 41 J. K. Jeong, S. Yang, D. Cho, S. K. Park, C. Hwang, K. I. Cho, *Appl. Phys. Lett.* 2009, **95**, 123505.
- 42 T. Kamiya, K. Nomura, H. Hosono, *Phys. Status Solidi A* 2009, **206**, 860-867
- 43 C. H. Ahn, Y. Y. Kim, D. C. Kim, S. K. Mohanta, H. K. Cho, *J. Appl. Phys.* 2009, **105**, 013502.
- 44 N. Yamaguchi, S. Taniguchi, T. Miyajima, M. Ikeda, *J. Vac. Sci. Technol. B* 2009, **27**, 1746.
- 45 S. Jeon, S. Ahn, I. Song, C. J. Kim, U. Chung, E. Lee, I. Yoo, A. Nathan, S. Lee, J. Robertson, K. Kim, *Nature Mater.* 2012, **11**, 301-305.

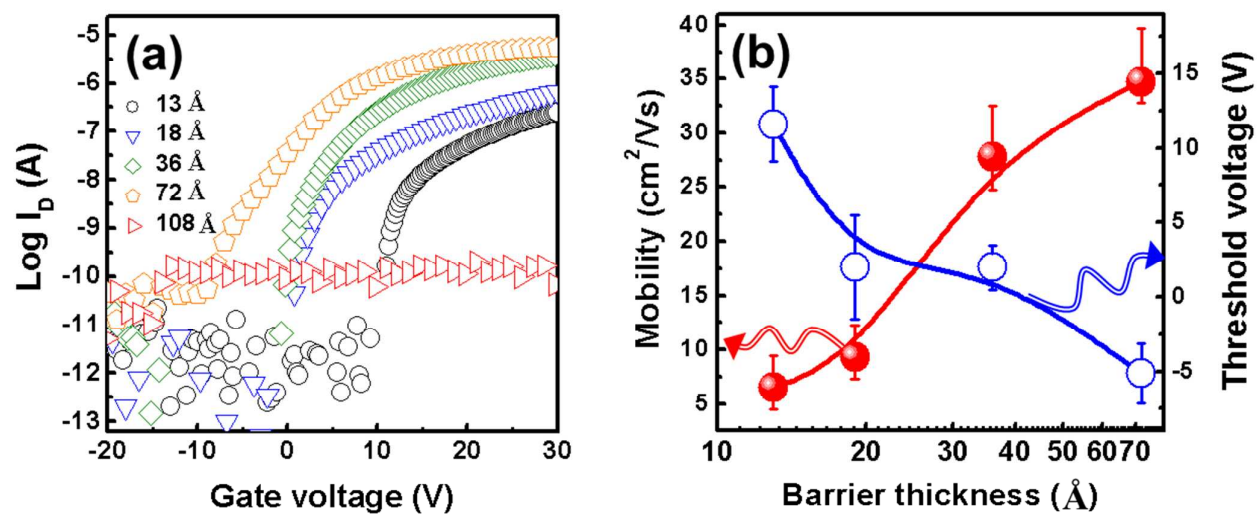
Figure 1



**Figure 1.** (a) Schematic diagram of the TFT structure and ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice structure indicating the measurement directions of J-V curves (in-plane and out-of-plane). (b) Overlap between the adjacent electron wave functions depending on Al<sub>2</sub>O<sub>3</sub> thickness. (c) The in-plane and (d) the out-of-plane J-V curves depending on Al<sub>2</sub>O<sub>3</sub> thickness within the superlattices.

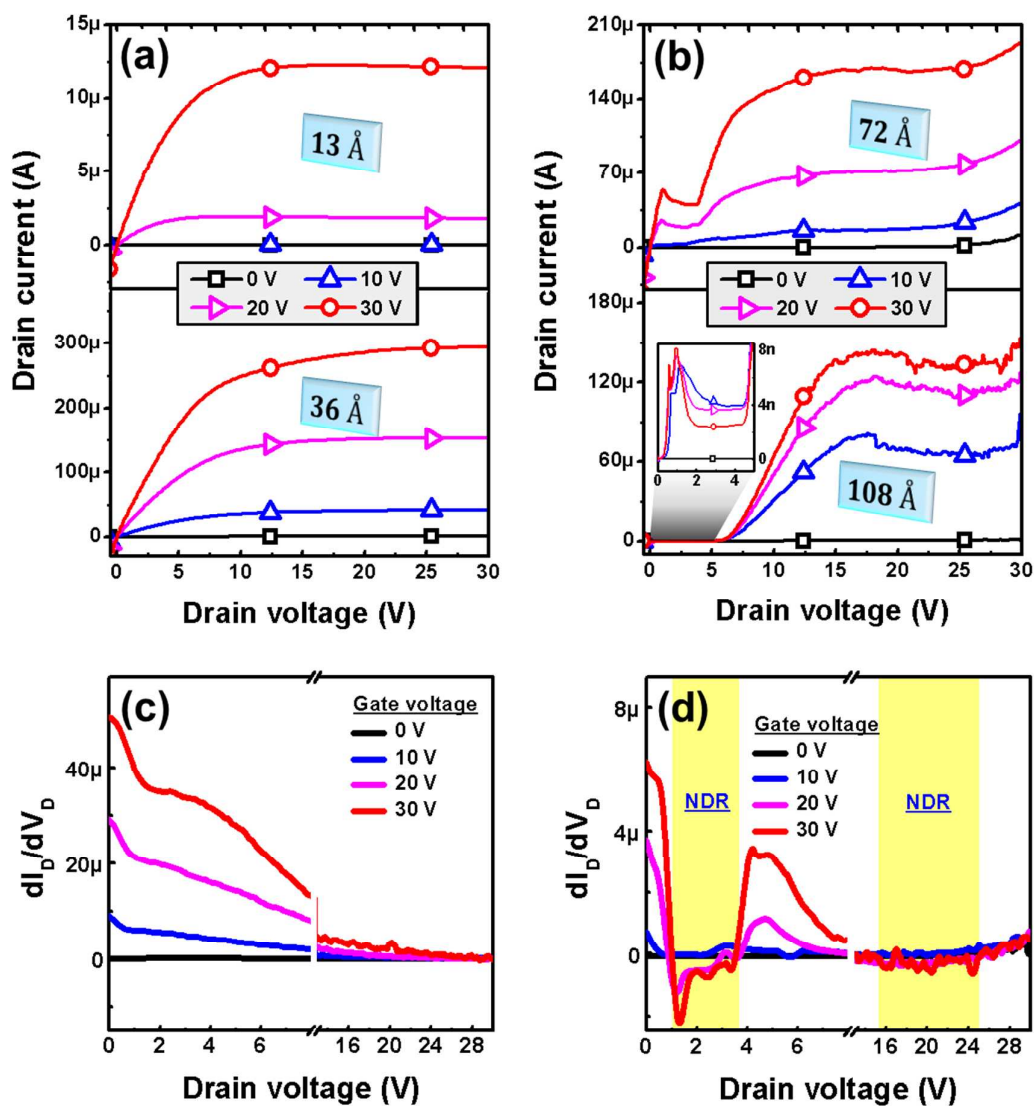


Figure 2



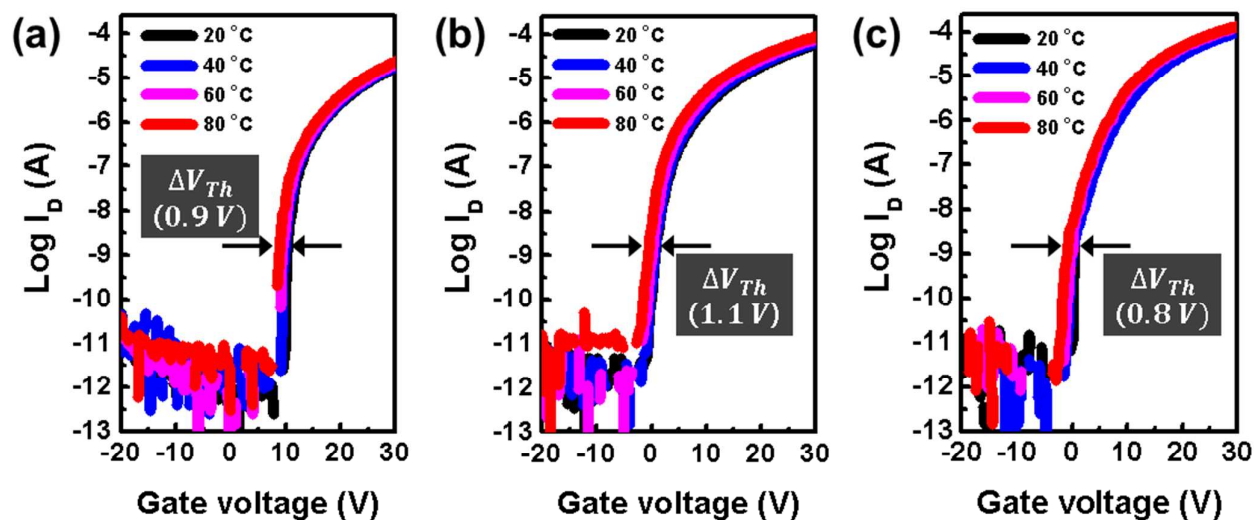
**Figure 2.** (a) Transfer curves and (b) figures of merit for the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs measured at a fixed drain voltage (0.1 V) as a function of barrier thickness.

Figure 3



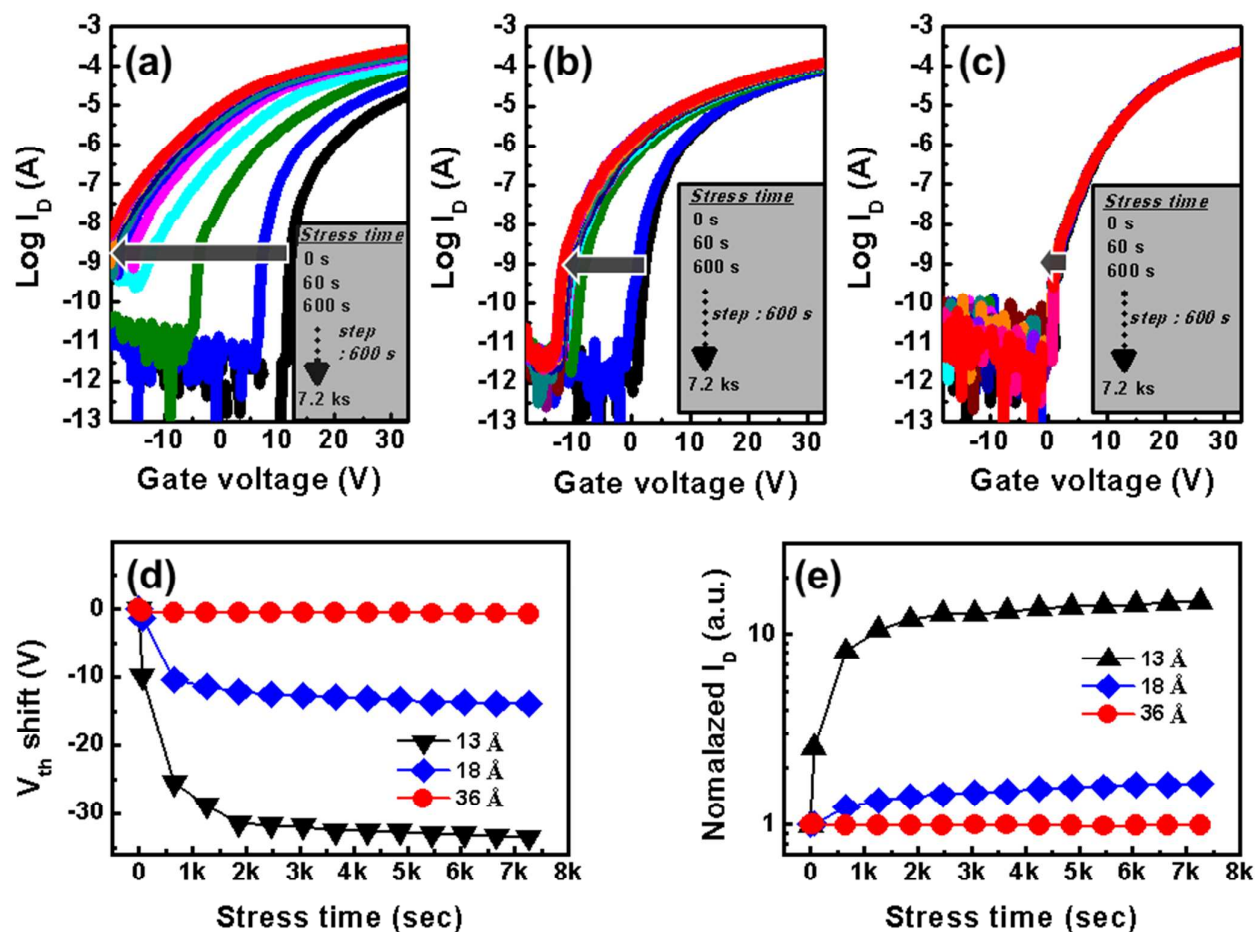
**Figure 3.** Out-put curves for the ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs with various barrier thicknesses: (a) 13 Å, 36 Å, and (b) 72 Å, 108 Å. The  $dI_D/dV_D$  vs.  $V_D$  obtained from out-put curves of the superlattice TFTs with different barrier thicknesses : (c) 36 Å and (d) 72 Å.

Figure 4



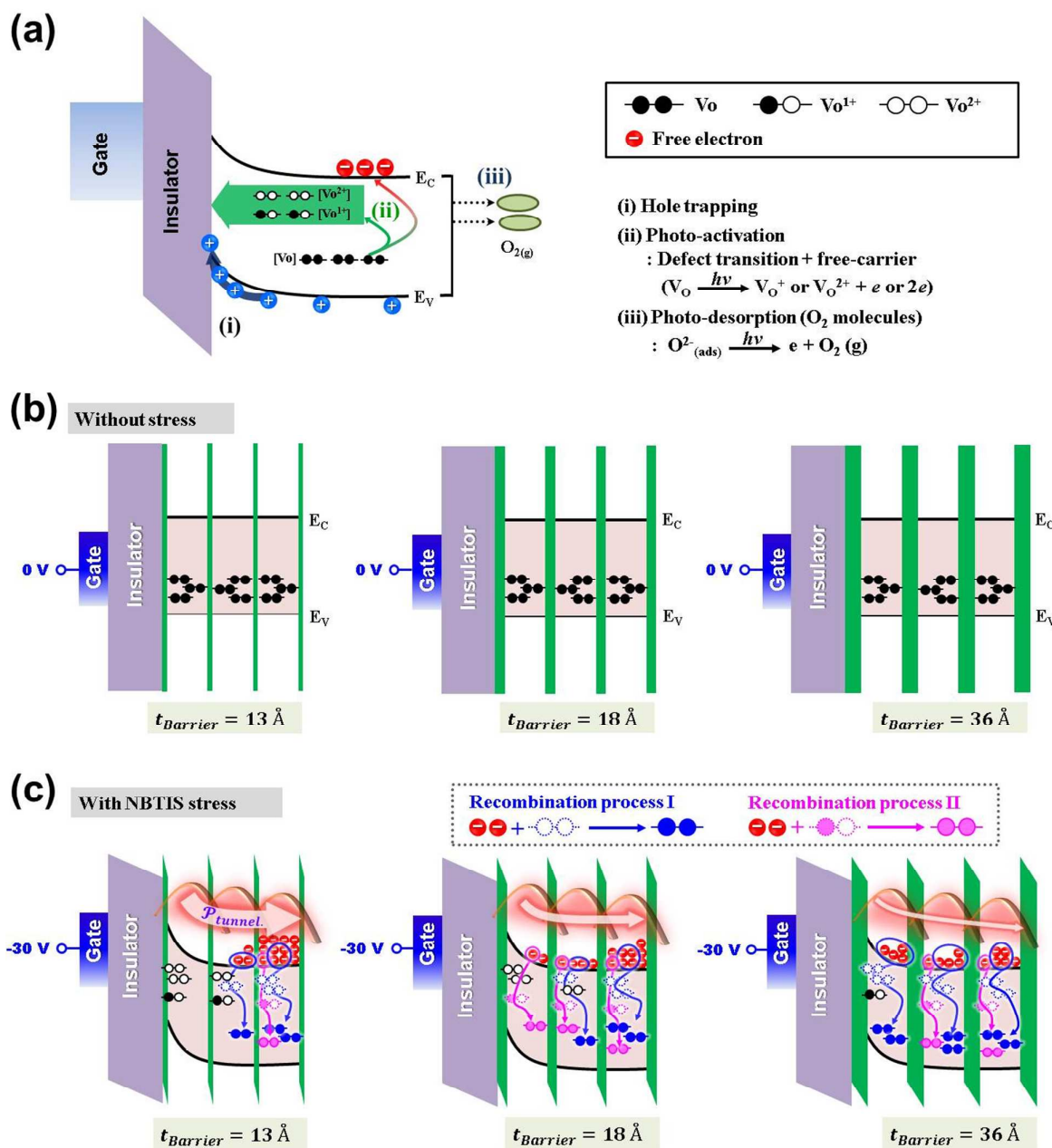
**Figure 4.** I-V curves showing the shift of transfer curve of ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice TFTs measured at a drain voltage of 10 V with various barrier thicknesses as a function of measurement temperature: (a) 13 Å, (b) 18 Å, and (c) 36 Å.

Figure 5



**Figure 5.** Variation of transfer curves for the superlattice TFT devices measured at a drain voltage of 10 V with different barrier thicknesses under NBITS Test at 60 °C: barrier thickness of (a) 13 Å, (b) 18 Å, and (c) 36 Å. (d) Summary of  $V_{th}$  shift of the superlattice TFTs induced by NBITS depending on barrier thickness. (e) Photosensitivity of the superlattice TFTs measured at a fixed gate voltage (+30 V).

Figure 6



**Figure 6.** (a) Schematic diagram showing the suggested origin of instability in oxide-based TFTs under a negative gate illumination stress : (i) trapping of the hole, (ii) transition of a neutral oxygen vacancy ( $V_o$ ) to a charged state ( $V_o^+/V_o^{2+}$ ) with a generated electron by illumination, and (iii) photo-desorption behavior of absorbed oxygen molecules at back channel regions. Schematic band diagrams to explain the different instability results observed in samples with various barrier thicknesses: (b) dark conditions and (c) NBTIS conditions.

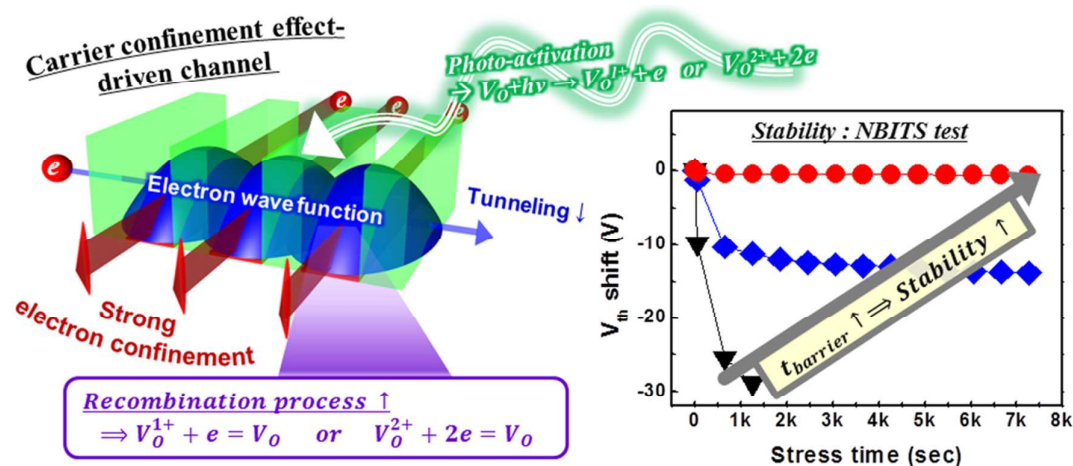
# Graphical abstract

## *Journal of Materials Chemistry A*

Carrier confinement effect driven-channel design and achievement of robust electrical/photo stability and high mobility in the oxide thin-film transistors

Cheol Hyoun Ahn, Hyun Koun Cho\*, and Hyoungsub Kim

School of Advanced Materials Science and Engineering, Sungkyunkwan University, 2066 Seobu-ro, Jangan-gu, Suwon, Gyeonggi-do, 440-746, Republic of Korea, E-mail: [chohk@skku.edu](mailto:chohk@skku.edu)



The performance of the carrier confinement effect-driven ZnO/Al<sub>2</sub>O<sub>3</sub> superlattice thin-film transistor strongly depended on electrical conductivity along the two-dimensional-like planar direction due to the confinement of carriers along the vertical direction. Also, carrier confinement effect-driven channel promoted recombination events between photo-ionized oxygen vacancies and the photo-charge electrons, resulting in extremely high stability under negative gate bias temperature illumination stress conditions.