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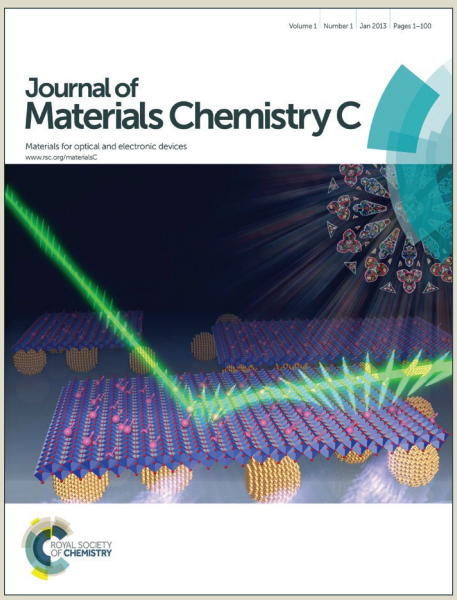





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# Low operating voltage ambipolar graphene oxide-floating-gate memories based on quantum dots

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Solution processed quantum dots (QDs) were employed as semiconductor layer in low operating voltage nonvolatile memory devices where the graphene oxide (GO) embedded as the charge storage element. Ambipolar PbSe QD layer intrinsically has the ability to transport holes and electrons, which provides an opportunity for the GO layer to trap both holes and electrons efficiently, resulting in bidirectional threshold voltage shifts after the program/erase operations applied. The memory exhibited a large memory window ($\Delta V_{on}$ ~ 6 V) and long retention time (>$10^4$ s) under low program/erase operating voltages as -/+ 25 V. The magnitude of $\Delta V_{on}$ is controlled not only by the programming/erasing voltages ($V_{P/E}$) but also by the bias voltage ($V_{DS}$), where $\Delta V_{on}$ shows a quadratic function to $V_{P/E}$ and linearly depends on $V_{DS}$. The QD based GO-floating-gate memories supply a facile route to fabricate flexible devices with low-cost large-scale integration.

## 1. Introduction

Lately, floating-gate based transistor nonvolatile memories have attracted considerable attention due to their dual functionality, i.e. transistor and memory operation, which have the benefits of single transistor, nondestructive read-out, and complementary integrated circuit architectural compatibility.[1-6] The basic mechanism of the floating-gate nonvolatile memories is that charge carriers induced by the external gate voltage can be trapped into or released from floating gate during programming/erasing (P/E) operations, resulting in reversible shifts on threshold voltage ($V_{th}$) to open a memory window in gate voltage.[7] Among the several choices (various metal and semiconductor nanoparticles) for charge storage nodes, graphene oxide (GO) is considered high relevant because it has many charge trapping sites due to oxygen groups such as epoxy and hydroxyl groups and the defective edge structure which bears carboxyl and ketone groups.[8,9] Several research groups have achieved GO-floating-gate memories (GOFGMs) with high performances. Park et al. reported pentacene-based GOFGM exhibiting a large memory window (~24 V for PMMA tunnel layer and ~15 V for PVP tunnel layer) at programming voltage of +80 V.[10] Kim et al. used pentacene as the active layer in a GOFGM, showing a memory window of around 2 V under an applied gate bias from 4 V to −5 V.[8] The GO charge trapping layers have generally been used in unipolar organic channel field-effect transistor (FET) memories, but inorganic bipolar quantum dots (QDs) have not yet been used as channel material.

The semiconductor QD FETs are easy to achieve bipolarity, which is suitable to integrate with complementary circuits.[11-13] The ambipolar QDs as a semiconductor layer can transport holes and electrons, which make it possible for the charge trapping layer to trap both holes and electrons efficiently.[14] So, in the QDs based memory devices, the trapping charges can be switched from one type to another according to the applied programming gate bias, resulting in a bidirectional $V_{th}$ shift and correspondingly a large memory window.[15,16] Importantly, the injected charges can overwrite the opposite trapped charges, which gives a promising way to reduce P/E operation voltages as well as power consumption. Therefore, developing ambipolar QD GOFGMs is significant and necessary. However, QD GOFGMs have never been reported as our knowledge.

In this work, we fabricated PbSe QD GOFGMs by using solution process method. The electrical behavior of the GOFGM can be modulated by either trapping holes or electrons in the GO sheets, which serve as both electron and hole trapping elements.[14] The use of PbSe QDs in GOFGMs successfully lowered programming and erasing voltages of the memory devices. The GOFGMs exhibited good memory characteristics with a large memory window and good retention capability, confirming the reliable nonvolatile memory properties. The semiconductor, tunneling and charge trapping layers of the GOFGMs were all developed using inexpensive and simple solution process at low temperatures.

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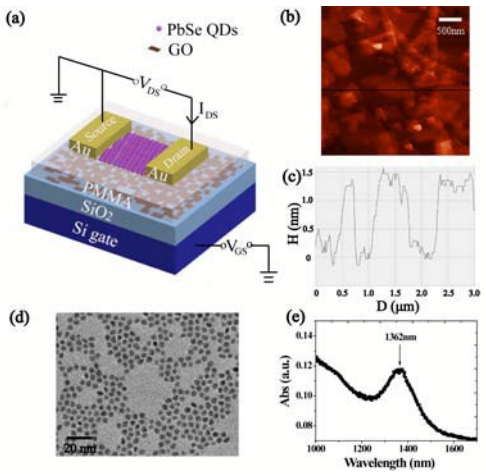


Fig. 1 (a) Schematic diagram of the ambipolar GOFGM; (b) AFM of GO deposited on $n^+$ Si/$SiO_2$ substrate; (c) The height of GO film; (d) TEM of PbSe QDs; (e) Light absorbance of PbSe QDs.

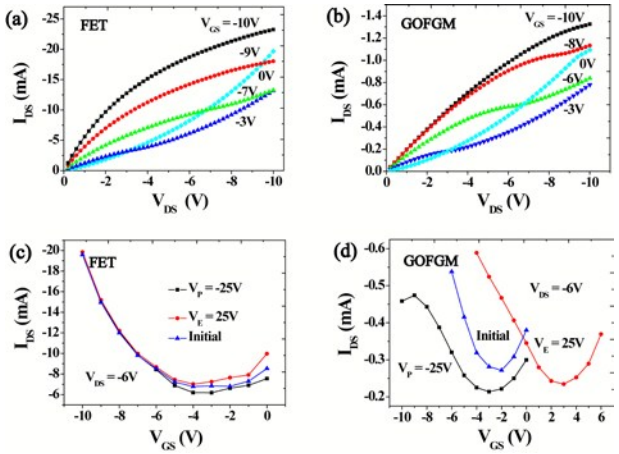


Fig. 2 Output characteristics of the FET (a) and the GOFGM (b) at the initial state. Transfer characteristics of the FET (c) and the GOFGM (d) after $V_{P/E}$ at - / + 25 V at $V_{DS}$ of -6 V.

Due to the advantages of bipolarity, high mobility, large area and low-cost, the QD GOFGMs can be considered to be a promising candidate for inorganic counterparts.

## 2. Experimental details

### 2.1 Device fabrication

The device architecture of the bottom gate top contact transistor-based GOFGMs is shown schematically in Fig. 1(a). The structure of GOFGM is $n^+$ Si/$SiO_2$/GO/polymethyl methacrylate (PMMA)/PbSe QDs/Au source-drain. A heavily doped n-type silicon ($n^+$ Si) with a 300-nm-thick thermally growth $SiO_2$ was used as the substrate after cleaned by ultrasonic treatment in propanol, acetone and deionized water for 10 minutes in sequence. Here, we used $n^+$ Si as gate electrode and $SiO_2$ as the gate insulator. To make a uniform GO charge trapping layer, a well dispersed solution of GO in deionised water (0.4 mg/ml) was spin-coated on $SiO_2$ surface at 6000 rpm for 60 s, followed by annealing at 80 ℃ for 15 minutes in air. A 30-nm-thick PMMA tunneling dielectric layer was formed by spin-coating an ethyl acetate solution (7 mg/ml) at 6000 rpm for 60 s and then annealed at 60 °C for 2 hours. Source and drain electrodes were prepared by thermally evaporated through a sophisticated shadow mask, by which the channel length (*L*) and channel width (*W*) were defined as 0.1 mm and 2.5 mm, respectively. In the final step, three layers of PbSe QDs were deposited on the top by using a layer-by-layer (LBL) approach from toluene solution. The details of the preparation and deposition of the PbSe QD see reference.[17] Before testing, the samples need to dry over 12 hours at vacuum to remove excess water and solvent.

By comparison, FETs with similar structures and processing conditions of GOFGMs were also fabricated, except for absence of the Go charge trapping layer. The structure of FET is $n^+$ Si gate/$SiO_2$/PMMA/PbSe QDs/Au source-drain. An $n^+$ Si with a 300-nm-thick $SiO_2$ was used as the gate electrode covered with the control dielectric. Subsequently, an approximately 30 nm thick PMMA tunneling layer was formed by spin-coating an ethyl acetate solution of PMMA (7 mg/ml) and cured at 60 °C for 2 hours. Source and drain electrodes were fabricated by thermally evaporated through a shadow mask with channel *L* and *W* defined as 0.1 mm and 2.5 mm, respectively. Finally, three layers of PbSe QDs were deposited on the top by spin-coating toluene solution.

### 2.2 Characterization

Fig. 1(b) demonstrates the atomic force micrograph (AFM) of the deposited GO layer between the PMMA tunneling layer and $SiO_2$ dielectric, showing clearly the surface morphology and coverage of the GO sheets. The $SiO_2$ dielectric was well covered by GO nanosheets with a step height of ~1.5 nm as shown in Fig. 1(c). The absorbance of PbSe QDs is displayed in Fig. 1(e), which was analyzed using a Zolix Omni-λ300 spectrometer. The absorption peak was located at 1362 nm, indicating the uniform size distribution of PbSe QDs. Based on the transmission electron microscopy (TEM) image of fig. 1(d), the average size of the PbSe QDs was 4 nm.

### 2.3 Electric measurements

In the electrical measurements, a bias voltage ($V_{DS}$) was applied to the drain and source (i.e., ground connection) electrodes by using a Keithley™ 2400; the channel current ($I_{DS}$) which flowed into the drain was also measured using the Keithley™ 2400. An applied gate voltage ($V_{GS}$) electrically connected the gate electrode and the ground using an HP6030A. The measurement was performed at room temperature in dark.

## 3. Results and discussion

### 3.1 Electrical characteristics

Fig. 2 shows electrical properties of the fabricated FETs and GOFGMs. The FET was used as a reference to analyse the charging effect of the dielectric system.

Fig. 2 presents the output characteristics ($V_{DS}$~$I_{DS}$) of the FET (a) and GOFGM (b), showing a *p*-channel field-effect behavior.

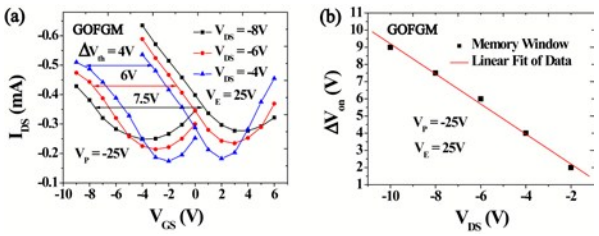


Fig. 3 (a) Memory hysteresis behavior of the GOFGM as a function of the $V_{DS}$ at -4 V, -6 V, -8 V; (b) Memory window of the GOFGM as a function of the $V_{DS}$ bias.

At low $V_{GS}$, FET and GOFGM exhibit typically ambipolar, $I_{DS}$ increasing rapidly with the increase of $V_{DS}$. It indicates both holes and electrons transport in the channel of the FET and GOFGM.[18] In thus voltage range, the increasing of non-saturating $I_{DS}$ was attributed to electron injection from the drain contact. The $I_{DS}$ of GOFGM was much lower than that of FET at the same $V_{GS}$, which can be attributed to the shielding effect of trapped charge carriers in the GO charge trapping layer.

To verify the programmable and erasable property, the initial, programming and erasing transfer curves of the FET and GOFGM were presented by measuring the $I_{DS}$ according to the applied $V_{GS}$ before (initial curve) and after the P/E operations. As shown in Fig. 2(c), there is a ignorable shift of the transfer curves in the FET after applying P/E voltages ($V_{P/E}$) of −/+ 25 V for 5 s at $V_{DS}$ = −6 V, indicating that negligible positive or negative charges are trapped in the gate dielectric layer of the FET.

Unlike the properties of FET, the negative and positive transfer characteristic shifts versus the initial curve were obviously in GOFGM, as shown in Fig. 2(d). The V-shape transfer curve is a typical ambipolar presentation controlled by the polarity of $V_{GS}$. The bidirectional shifts indicate not only holes but also electrons were trapped into the floating gate.[19] For ambipolar GOFGM, we define the turn-on voltage ($V_{on}$) as the $V_{GS}$ at which the $I_{DS}$ changes from hole transport to electron transport.[20] After applying a programmed gate bias ($V_P$) of −25 V to the bottom gate electrode, the transfer curve shifted to the negative direction in comparison with the initial curve, indicating holes charged up the GO. The $V_{on}$ for the GOFGM after P operation was −3 V. Until applying an erasing gate bias ($V_E$) of 25 V, the transfer curve shifted to the positive direction, indicating electrons, instead of holes, stored in the GO. The $V_{on}$ for the GOFGM after E operation was 3 V.

The memory window ($\Delta V_{on}$) is defined as the shift range between the transfer curves through applying the P/E pulses.[21] Fig. 2(d) shows a conspicuous $\Delta V_{on}$ of 6 V with $V_{P/E}$ of −/+ 25 V for 5 s and the $V_{DS}$ kept at −6 V. The broadened $\Delta V_{on}$ of the GOFGM is attributed to the independent trapping of holes and electrons in the GO during the P/E operations. The mobility ($\mu$) of the fabricated devices in the saturation region is estimated from the following equation:[22]

$$I_{DS} = \frac{WC_i}{2L}\mu(V_{GS} - V_{th})^2 \qquad (1)$$

where $C_i$ is the insulator capacitance per unit area and $V_{th}$ is the threshold voltage. The $V_{th}$ of the device is determined by extrapolating the intercept of plot of $(I_{DS})^{1/2}$ versus $V_{GS}$.[23] The hole and electron mobility of the GOFGM are calculated to be 0.41 and 0.27 $cm^2 V^{-1} s^{-1}$, respectively. Those values are higher than that of the organic transistor memories that have been reported elsewhere.[8,10]

### 3.2 Influence of $V_{DS}$ on memory window

To evaluate the effect of bias voltage on memory window, different bias pulses were supplied to drain electrode and then the transfer characteristics were measured. Fig. 3(a) shows three typical hysteresis transfer curves with obviously positive and negative shifts of the $V_{on}$ as $V_{DS}$ increased. When the drain voltage increased from −4 V to −8 V, the memory window increased from 4 V to 7.5 V with a fixed $V_{P/E}$ voltages of −/+ 25 V. It indicates that the $\Delta V_{on}$ of the GOFGM depends strongly on the magnitude of the applied $V_{DS}$ at the fixed P/E conditions.

In order to further examine the influence of $V_{DS}$ to $\Delta V_{th}$, more bias voltages were applied to the drain electrode. Fig. 3(b) shows the $\Delta V_{on}$ raised almost linearly with the increase of the $V_{DS}$. By following the linear fit, equation $\Delta V_{on}$ = 0.45 − 0.875 $V_{DS}$ was obtained. It confirms that memory window of the GOFGM is controlled not only by the P/E voltages but also by the $V_{DS}$ applied on the channel.

### 3.3 Influence of $V_{P/E}$ on memory window

Fig. 4 shows the change trend of the memory window and charge trap density of the GOFGM along with the applied $V_{P/E}$ voltages.

When the $V_{P/E}$ range was increased from −/+ 10 V to −/+ 25 V at $V_{DS}$ = −6 V, the memory window of the GOFGM increased from 0.5 V to 6 V. The larger $V_{P/E}$ pulses led to larger memory windows. The $\Delta V_{th}$ was raised with the increase of the $V_{P/E}$ following the polynomial fit equation $\Delta V_{on}$ = −2.5 + 0.332 $V_{P/E}$ − 0.003 $(V_{P/E})^2$. The number of stored charges can be estimated from the equation:[24]

$$\Delta n = \frac{C_i \cdot \Delta V_{on}}{e} \qquad (2)$$

where $C_i$ is the specific capacitance of the gate dielectric, $e$ is the element charge, and $\Delta V_{on}$ is the memory window. The density of trapped charges in the device for the $V_{P/E}$ range increased from −/+ 10 V to −/+ 25 V is calculated to increase from 0.32 × $10^{12}$ $cm^{-2}$ to 3.8 × $10^{12}$ $cm^{-2}$. These values are

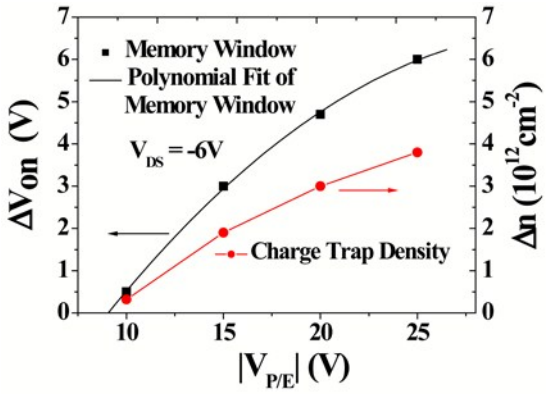


Fig. 4 Memory window (black dots), polynomial fit of memory window (black line) and charge trap density (red dots) versus the $V_{P/E}$ sweep range.

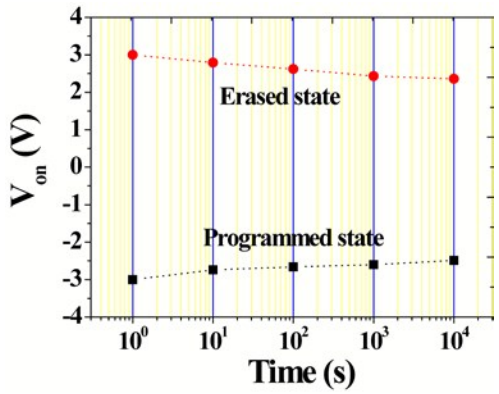


Fig. 5 Programming (black dots)/erasing (red dots) data retention properties as a function of the retention time.

comparable to the other GOFGMs that have been reported elsewhere.[8] The transferred charges are trapped in the GO sheets which can be tuned by changing the number of defects or degree of oxidation.

The memory window is determined by the amount of trapped charges in the GO layer, which is oriented from the applied voltage level of both P/E and $V_{DS}$ voltages.

### 3.4 Retention characteristic of the GOFGM

As an important parameter of the nonvolatile memory devices, the data retention capability is a function of the elapsed time in the P/E states, which can demonstrate the potential lifetime of nonvolatile storage. Fig. 5 shows the GOFGM was programmed/erased by applying $V_{P/E}$ of −/+ 25 V for 5 s at $V_{DS}$ = −6 V and recorded the $V_{on}$ at a certain period of time (time intervals: 1, 10, $10^2$, $10^3$ and $10^4$ s). The initial memory window was approximately 6 V. Both the programmed and erased states degraded with time. The memory window was remained at 80.8% for $10^4$ s, which was comparable to the previously reported low voltage organic memory devices.[25]

Vertical loss of storage is the typical results of charge tunneling from GO layer through the PMMA tunnel layer.[14] Due to the energy barrier between GO and PMMA, the trapped carriers are difficult to escape from the potential well merely by thermal energy at normal temperature.[26] The controlled separation of neighboring GO sheets can also prevent the lateral loss.

### 3.5 Memory mechanism

To analyze the memory behavior, the possible mechanism of GOFGM is shown in Fig. 6 by using the energy-band diagrams corresponding to P/E processes. In the ambipolar GOFGM, the memory properties are achieved by trapping both holes and electrons according to gate voltage.

When applying a negative $V_{GS}$ for programming, the orbital energy level of PbSe QDs bends upwards, as shown in Fig. 6(a).The holes have chances to tunnel though the PMMA layer from the highest occupied molecular orbital (HOMO) of PbSe QDs units to the GO sheets, while the electrons are released from the GO to the lowest unoccupied molecular orbital (LUMO) of PbSe QDs. After neutralizing the residual electrons, the redundant holes generate a built-in electric field, resulting

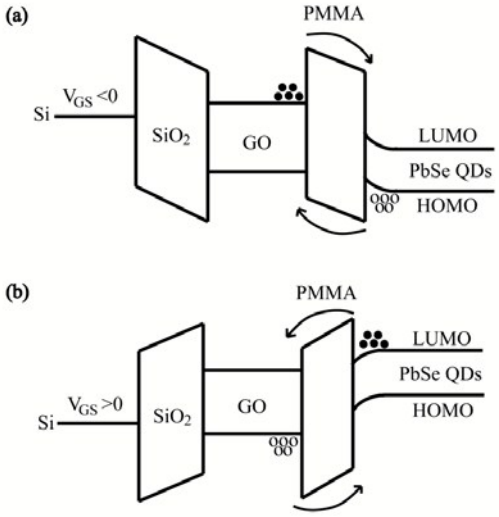


Fig. 6 Energy level diagrams with supplying negative $V_{GS}$ (a) and positive $V_{GS}$ (b).

in obvious negative shift of transfer curve. The holes trapped in the GO layer are confined by the PMMA tunneling layer, even after the $V_{GS}$ is removed, due to the existence of a potential barrier between the GO and the HOMO of PMMA, resulting in nonvolatile memory.[27] Similarly, when a large positive $V_{GS}$ is supplied for erasing, the orbital energy level of PbSe QDs bends downwards, as shown in Fig. 6(b). The trapped holes are ejected from the GO to the PbSe QDs channel and more electrons are injected into the GO. After neutralizing the residual holes, the electrons trapped in the GO generate a built-in electric field , which lead to a positive shift of the transfer curve.[28] The electrons are confined in the GO by the potential barrier between LUMO of the PMMA and the GO layer.

Due to the charge trapping and releasing in the GO, a wide memory window with bidirectional turn-on voltage shift is obtained in the memory device.

## Conclusions

We have developed inorganic PbSe QDs based low voltage GOFGMs by using solution-processed method where GO nano sheets served as charge-trapping layer. Due to the bipolarity of QD active layer, the transfer curves showed negative or positive turn-on voltage shifts according to the applied $V_{P/E}$, indicating ambipolar charges trapping and detrapping in GO nanosheets. Under applying $V_{P/E}$ of − /+ 25 V, the memory device showed large hysteresis with a memory window of around 6 V and with the trapped charge density of $3.8 \times 10^{12}$ $cm^{-2}$ at $V_{DS}$ = −6 V. Furthermore, the GOFGM showed good memory retention characteristics with the memory window maintained at 80.8% for $10^4$ s. As a promising candidate for inorganic FGM, the QD GOFGM showed high performances,

which were fabricated by all simple and low-temperature solution processes. Therefore, those devices exhibit the scale fiercely competitive in flexible memories with low cost, large-integration and high performances.

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