RSC Advances

Expedient floating process for ultra-thin InGaZnO thin-film-transistors and their high bending performance

Journal:	*RSC Advances*
Manuscript ID	RA-ART-03-2016-006372.R1
Article Type:	Paper
Date Submitted by the Author:	11-Jun-2016

Complete List of Authors:	Kang, Won Jun; SungKyunKwan University , School of Advanced Materials Science and Engineering Ahn, Cheol Hyoun; Sungkyunkwan University, Yun, Myeong Gu; SungKyunKwan University , School of Advanced Materials Science and Engineering Cho, Sung Woon; Sungkyunkwan University, School of Advanced Materials Science and Engineering Kim, Ye kyun; SungKyunKwan University Kim, Da Eun; Sungkyunkwan University, Advanced Materials Science and Enginnering Kim, Bora; SungKyunKwan University Cho, Hyung Koun; Sungkyunkwan University, School of Advanced Materials Science and Engineering Kim, Yunseok; Sungkyunkwan University,

Subject area & keyword:	Inorganic materials < Materials

RSC Advances

ARTICLE

Expedient floating process for ultra-thin InGaZnO thin-film-transistors and their high bending performance

Received 00th January 20xx,
Accepted 00th January 20xx

DOI: 10.1039/x0xx00000x

www.rsc.org/

Won Jun Kang, Cheol Hyoun Ahn, Myeong Gu Yun, Sung Woon Cho, Ye Kyun Kim, Da Eun Kim, Bora Kim, Hyung Koun Cho* and Yunseok Kim

Recently, much attention has been focused on the development of the devices with ultra-thin sample thickness for imperceptible and patchable applications, but the use of inorganic active films in flexible electronics exhibited a great obstacle due to brittle mechanical properties during bending, despite better electrical performance and high stability. We report the procedure for fabricating inorganic electronic devices on ultra-thin polymer substrates using a *floating process.* This process uses water soluble polyvinyl alcohol (PVA) as a sacrificial layer and the maximum process temperature is increased until around 200 ^{o}C, which is a valuable condition for high-quality InGaZnO channels and Al_2O_3 gate dielectrics. The 400 nm PVA coating produced with low molecular weight characteristics had relatively smooth surface roughness and the quick floating process. The ultra-thin InGaZnO TFT showed good transfer and reproducible performances under extreme bending conditions due to the use of ultra-thin compliant substrates.

Introduction

Various approaches for the development of electronic skin (e-skin) that mimics human skin have been suggested since 2010.[1] To fabricate e-skin devices, driver circuits for controlling sensors as well as sensor devices such as pressure and temperature response should be directly embedded.[2,3] For the realization of transistor devices on flexible or stretchable substrates, some groups demonstrated a method to attach semiconductor nanowire transistors to sticky substrate in the early stages.[4-7] Many researchers including Bao's team and Someya's team have successfully utilized organic materials as active semiconductors due to the enormous advantage on it flexibility and low process temperature.[8-10] Nevertheless, organic semiconductors have undesirable features including environmental instability and low field effect mobility, which significantly constrain their commercialization despite long term study.[11] On the contrary, the material concerns on inorganic semiconductors have been changed from conventional Si to novel oxides with amorphous phases that exhibit high field effect mobility and high stability as well as moderate temperature processibility compatible with plastic substrates. However, these oxide based transistors also have limitations related to marginal mechanical brittleness in flexible devices. Novel electronic devices such as e-skins require the use of lightweight substrates and transparent films for imperceptible applications.[7] These requirements can be realized by combining ultra-thin substrates and transparent oxide semiconductors.[12,13] In particular, it is well known that significant reduction in sample thickness reinforces the mechanical durability of inorganic amorphous films, resulting in modest bending performance. However, ultra-thin substrates are difficult to handle during device fabrication, thus, transfer processes using polymer stamps and spalling processes to remove the top layer have been suggested, but these are inadequate for large scale wafers.[14]

Recently, some researchers reported a concept for ultra-thin devices using inorganic semiconductors and suggested the use of a soluble sacrificial layer for the detachment of rigid substrates.[12,13,15] Polymers such as Polyethylene naphthalate (PEN), Polyamide, Polyethylene terephthalate (PET), Parylene, etc., are acknowledged as the most suitable substrates due to their thickness controllability, insulating property, compatibility with human skin, durability, processibility, chemical resistance and so on. In particular, imperceptible devices require the use of ultra-thin and transparent polymer substrates. However, polymer substrates deform easily at high temperatures near the glass transition temperature.

School of Advanced Materials Science and Engineering, Sungkyunkwan University, 2066 Seobu-ro, Jangan-gu, Suwon, Gyeonggi-do 16419, Republic of Korea.
Electronic Supplementary Information (ESI) available: [details of any supplementary information available should be included here]. See

In this study, we demonstrated a floating process using water soluble polyvinyl alcohol (PVA) to produce ultra-thin electronic devices with ~10 µm thickness on flexible substrates. The PVA, which has outstanding water-solubility, is used as the sacrificial layer, and the final flexible substrate is Parylene, which has superb properties of high heat resistance, high chemical resistance, and transparency. The Parylene is deposited on the PVA/rigid substrate by chemical vapor deposition (CVD). We optimized the floating process by evaluating the surface roughness, floating time, and residues from PVA with various molecular weights (M_w), and then characterized the electrical and bending performances of the *a*-InGaZnO (*a*-IGZO) thin-film-transistors.

Experimental section

PVA coating

Fig. 1 (a) demonstrated the process flow for the preparation of flexible and ultra-thin polymer substrates with around 10 µm thickness. Here, we utilized the difference in chemical bonding by coating a sacrificial polymer (PVA) soluble in DI water, and consequently, the ultra-thin polymer substrates with low area mass density floated on the surface of the DI water.

The sacrificial PVA layers were prepared by dissolving 12 g of PVA (Sigma Aldrich, 13,000 M_w, 31,000 M_w, 89,000 M_w, and 146,000 M_w) in 100 ml of DI water (70 °C) (aq.). Since the PVA materials consisted of many hydroxyl groups (-OH), they were soluble in water. According to their intrinsic characteristics, higher M_w is expected to induce harder viscosity, and dissolution in the solvent takes a long time.[15] The viscosity of PVA with 146,000 M_w is too strong, and as a result, the surface was not sufficiently flat. The prepared PVA solution was dropped onto the cleaned glass substrates, followed by spin coating at 1,000 ~ 6,000 rotations per minute (RPM). Finally, a baking process was performed at 100 °C for 2 min.

Parylene coating

As the second step, Fig. 1 (b), Parylene films with a thickness of 10 µm were deposited on the PVA using CVD, where the Parylene films were utilized as ultra-thin substrates for the flexible devices. Prior to the deposition, dimmer liquid state of a Parylene precursor was vaporized at 175 °C and was changed into the monomer state by pyrolysis at 680 °C. Rapid cooling to room temperature (RT) of the monomerized Parylene resulted in coagulation by polymerization. In this process, the coating thickness corresponding to 10 µm was determined by the initial amount of Parylene liquid. These Parylene films are often used for the surface protection of metal, plastic, and rubber from harmful environmental conditions, since they show high corrosion resistance and chemical stability to oxidation up to 350 °C.[16,17] Furthermore, the RT coating of the Parylene induces low film stress with the underlying/overlying layers and low pinhole density, which are very attractive chemical and physical properties for ultra-thin electronic devices.

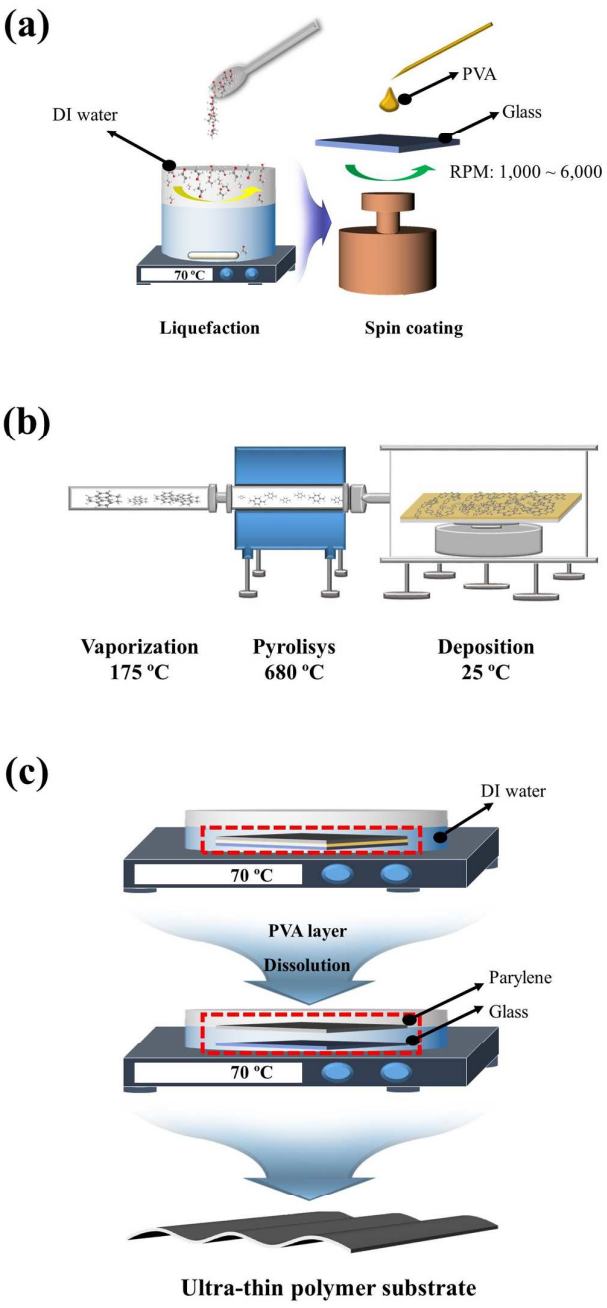


Fig. 1 (a) The first coating film was water soluble PVA (13,000 M_w, 31,000 M_w, and 89,000 M_w) used as a sacrificial layer on the rigid glass. (b) Parylene film with 10 µm thickness was deposited on the PVA by CVD. (c) Floating process of the Parylene/PVA/glass to detach rigid glass and Parylene in the DI water (70 °C), resulting in the formation of an ultra-thin Parylene substrate.

TFT fabrication

"We fabricated *a*-IGZO TFTs on Parylene/PVA/glass substrates. The source/drain (S/D) electrodes were composed of Mo (100 nm) and were deposited via direct-current magnetron sputtering at room-temperature. Patterning of the electrodes was carried out using a lift-off process that employed an AZ5214 photoresist. The active layer of *a*-IGZO (55 nm) was also deposited via radio-frequency sputtering, and the *a*-IGZO channels were patterned using a photolithography process. The Al_2O_3 (80 nm) gate dielectric layers were deposited using tri-methyl-aluminium (TMA) and high-purity H_2O as precursors, via ALD. The maximum process temperature including that used for ALD was relatively low (150 °C). Finally, the gate metal was also composed of Mo (100 nm), and was defined using a lift-off process. The width and length of the channel were 500 µm and 50 µm, respectively.[18] After fabricating *a*-IGZO TFTs, the samples were dipped in water (70 °C) for separation of the glass substrate and the a-IGZO TFT. The electrical performance of these ultra-slim flexible TFTs was measured using an HP4145B semiconductor parameter analyzer."

Floating process

As shown in Fig. 1(c), the soaking of the Parylene/PVA/glass in the DI water led to detachment between the rigid glass and Parylene substrate by dissolving water soluble PVA. The dissolution begins from the edge, and the ultra-thin Parylene substrate eventually peels off the glass surface and floats on the DI wafer due to its light weight. Afterward, we named this method for detachment with glass substrates the *floating process.*

Results and discussion

The thickness of the coated PVA strongly depends on the RPM speed of the spin-coater and the M_w of the solute. Our optimization process for the PVA coating mainly focused on the designed thickness and the uniformity of the film roughness. The coating thickness and the film uniformity are related with the accessibility in the handling of the ultra-thin devices and the interface roughness of multilayer devices, respectively. These properties of the PVA used as a sacrificial layer were determined by the rotation speed of the spin-coater and the solution viscosity. The intrinsic viscosity (η) of the solution increases with increasing M_w according to the equation $[\eta] = KM_w\alpha$, where K and α are constants depending on the type of solute or solvent and depending on the temperature, respectively. Also, it is accepted that the film thickness is inversely proportional to the RPM depending on $h_f \propto (\eta_0/\rho\omega)^{1/2}$, where h_f is the film thickness, ω is the spin speed, η_0 is the initial solution viscosity, and ρ is the initial solution density.[19] With decreasing M_w, a PVA coating with high uniformity and various thicknesses is expected despite low RPM. On average, the PVA coating with 400 nm thickness

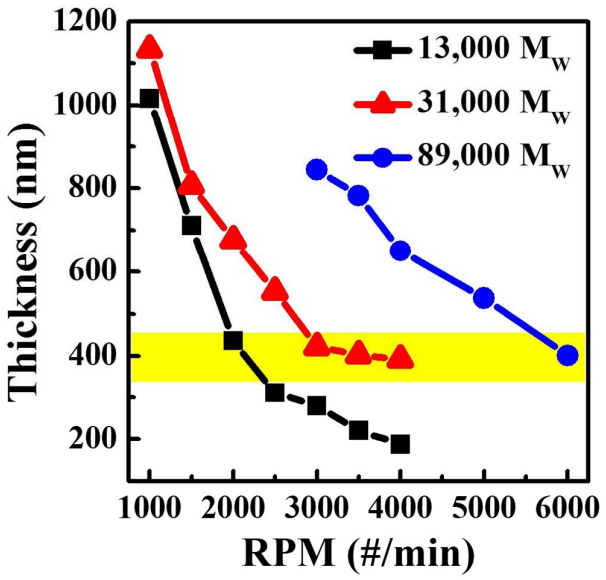


Fig. 2 The thickness of the PVA coated with different M_w as a function of the RPM for spin coating. The yellow region corresponds to the PVA thickness with good uniformity used in this study.

shows relatively good uniformity and sacrificial properties, as indicated by the yellow shading in Fig. 2. Thus, we selected 400 nm as the thickness of the sacrificial PVA, and it was controlled by the M_w and RPM speed at the same time.

Fig. 3 is the AFM results showing the surface morphology of PVA films with the same film thickness prepared under different M_w. For comparison, the morphology of the glass substrate was measured, as shown in Fig. 3(a), and the PVAs with 13,000 M_w, 31,000 M_w, and 89,000 M_w were characterized by atomic Force Microscopy (SPM: NX10, Tip: NCHR). The PVA film prepared with 13,000 M_w showed a slightly higher R_{rms} value (0.58 nm) compared to glass (0.37 nm). However, further increase in the M_w induced an abrupt increase in the R_{rms} values, as shown in Figs. 3(c) and (d). This is attributed to the enhanced condensation of hydrogen bonding from the overlap of polymer chains.[20] Consequently, the best surface morphology was observed in the PVA coating with 13,000 M_w.

To fabricate inorganic devices such as various sensors or oxide thin-film-transistors, temperature elevation is recommended for high performance and stability. This process includes growth temperature and post-thermal treatments, such as thermal annealing of oxide channels and ALD for gate dielectrics. Except for the ultra-violet annealing procedure, most fabrication process involve substrate heating at around 150 °C at least. The popular Polyimide substrates with high glass transition temperatures had low transmittance in the visible range and high-cost, and thus, they are not the best choice for invisible and ultra-thin (imperceptible) electronics.

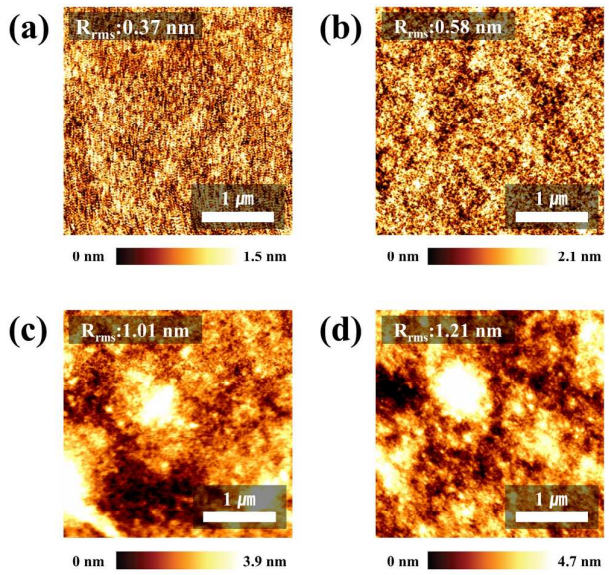


Fig. 3 AFM images showing the surface morphology of the coated PVA: (a) glass, (b) 13,000 M_w, (c) 31,000 M_w, and (d) 89,000 M_w.

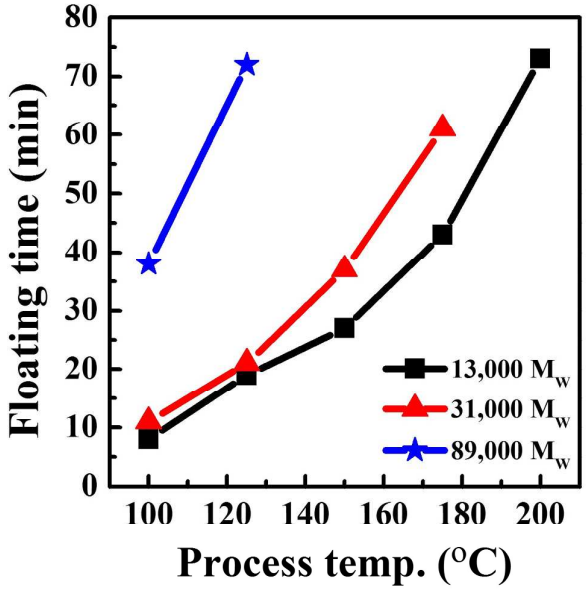


Fig. 4 Variation of floating time for detachment as a function of thermal treatment temperature for 3 hours Evolution of floating process according to soaking time.

On the other hand, the Parylene substrate is optically transparent and electrically insulating, and has relatively high glass transition temperature and superb chemical stability. Nevertheless, the elevation of the process temperature above the transition temperature during device fabrication may induce strong solidification after cooling due to the thermoplastic property. Additionally, the intrinsic water soluble characteristics disappear, resulting in the absence of the function of PVA as a sacrificial layer between glass and Parylene films. Thus, we investigated the tolerance temperature of the PVA depending on the M_w. The water soluble PVA thin films make the glass substrate and the Parylene film detach after device fabrication, and the ultra-thin Parylene film plays a role in ensuring flexible substrates.[12,17] Therefore, the utility of PVA is limited as a dissolved sacrificial-layer without any functions. Thus, we can increase the process temperature above the glass transition temperature (T_g) of PVA.

Fig. 4 shows the average time required for the floating (or detachment) of ultra-thin Parylene as a function of annealing temperature for 3 hours, where the annealing process is related to the thermal treatment during the entire follow-up process. It is generally known that PVA has a T_g of 75 °C and a melting temperature (T_m) of 185 °C.[21] However, in this work, process temperatures between the T_g and T_m of PVA were used, since the optimum process temperature should be determined by considering the application of high process temperature and the floating process dimmer liquid state. It is anticipated that the PVA cannot be soluble in water due to condensation and gelation prepared by excess high process temperatures. In addition, the PVA with higher M_w had a longer dissolution time (Fig. 4). The reduced process temperature and the PVA with lower M_w are expected to result in shorter floating time. For example, with a process temperature of 150 °C applied for 3 hours, the PVAs with 13,000 M_w and 31,000 M_w had floating times of 27 and 37 min, respectively, in water at 70 °C. However, the PVA with 9,000 M_w demonstrated non-detachable performance between the glass and Parylene, despite a long time soaking in water. Consequently, the floating process is a very simple and workwithable approach for producing ultrathin polymer substrates or devices.

Fig. 5 contains the optical microscope images showing PVA related residues on the surface of glass substrates after the floating process. The high temperature process clearly leaves insoluble residues even on the PVA with 13,000 M_w, as expected. As shown in Figs. 5(c) and (d), the residues begin to be observed in the samples processed at 200 °C. Since the T_m of PVA is 185 °C, the 200 °C thermal process induces active rotational motion in each molecular chain.[21,22] The glass substrates with PVA residues were further investigated by FT-IR (VERTEX 70). Figure 5(e) illustrates the FT-IR absorption spectra between 2,500 and 4,000 cm^{-1}. This range includes the peaks assigned for O-H and C-H bonding, where 2,850~3,000 cm^{-1} and 3,400~3,650 cm^{-1} peaks correspond to C-H and O-H bonding, respectively. Compared to the sample without residues, this result indicates a distinct polymer bonding from thermal processing above 200 °C. The cross-linking is made up by the adjacent O-H bonding of PVA.

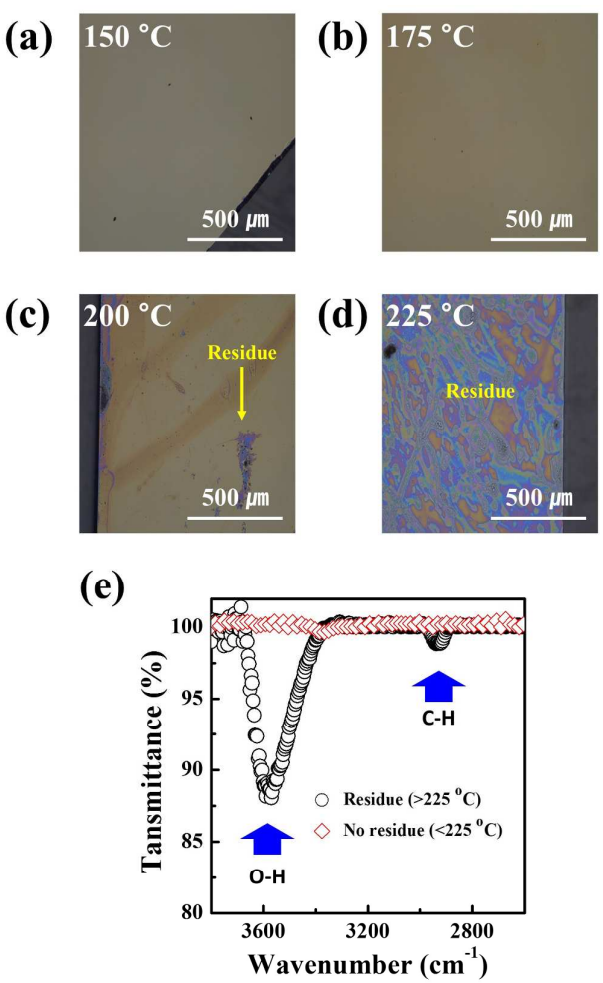


Fig. 5 Optical microscope images showing PVA residues after floating process for the samples with different annealing temperatures. (a) 150 °C, (b) 175 °C, (c) 200 °C, and (d) 225 °C. (e) FT-IR absorption spectrum of 2,500~4,000 cm^{-1} obtained from the samples with and without PVA residues. Here, 2,850~3,000 cm^{-1} and 3,400~3,650 cm^{-1} peaks correspond to O-H and C-H bonding, respectively.

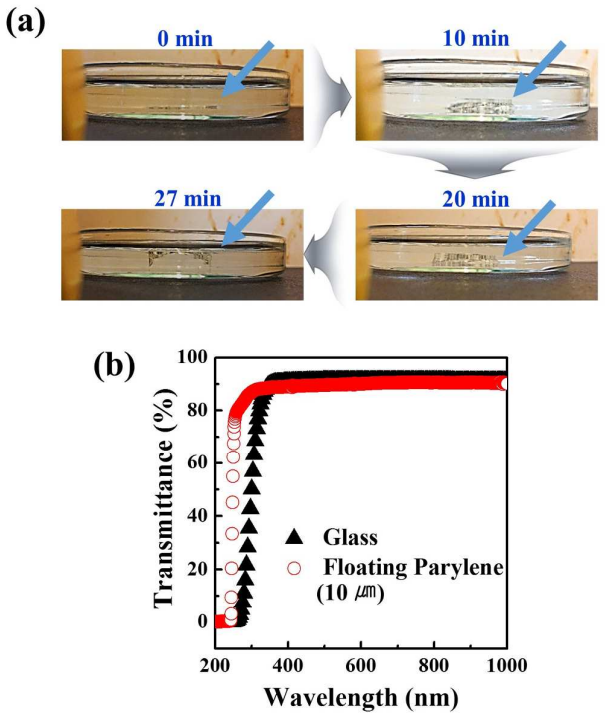


Fig. 6 (a) Evolution of floating process according to soaking time. (b) UV-Vis Transmittance of glass substrate and ultra-thin Parylene substrate

Fig. 6(a) shows the floating evolution depending on the soaking time from the sample prepared with 13,000 M_w. This sample was completely detached after 8 min, and floated on the surface of water. The thickness of the used Parylene is around 10 μm. For imperceptible devices, ultra-thin PVA samples should be transparent and lightweight. Therefore, we measured optical transmittance in the ultra-violet-visible region by UV spectrometer (UV-1800), as shown in Fig. 6(b). The 10 μm thickness Parylene (90.5 %) showed similar transmittance as a glass substrate (91.3 %) due to its high transmittance and ultra-thin thickness. To compare the lightness of this sample, we estimated the area mass ($\rho_{area} = M/S$, where M and S are total mass and area) by measuring mass. The detached Parylene with 10 μm thickness had an area mass of 0.95 g/cm^2, which corresponds to around 1/5 of an A_4 paper (5 g/cm^2).

To illustrate the effectiveness of the fabrication of ultra-thin devices using a simple floating process, we produced an oxide thin-film transistor (TFT) with a top-gate structure, as shown in Fig. 7. The gate and S/D metals were deposited with Mo (100 nm) by a magnetron sputtering system through a shadow mask to define width and length of 500 μm and 50 μm, respectively. The active layer and gate oxide were deposited with IGZO (55 nm) and Al_2O_3 (80 nm) by sputtering and ALD, respectively. After the formation of a traditional TFT on the glass substrate with PVA/Parylene coating, the device was soaked in water for the floating of the TFT device. The maximum process temperature used for the TFT fabrication was 150 °C in the ALD for the Al_2O_3 gate dielectric. The TFTs on Parylene were safely detached from the glass substrate in water.

A typical top-gate *a*-IGZO TFT structure was used for fabrication of the ultra-thin and flexible substrate, as shown in Fig. 7(a). The electrical performance of the ultra-thin *a*-IGZO TFT shows a typical transfer curve [drain current (I_D)-gate voltage (V_G)] under different gain voltages (V_D). The threshold voltage (V_{th}) of the TFT was calculated to be -0.72 V, which was the gate voltage at which a I_D of 1 nA flows. Also, the field-

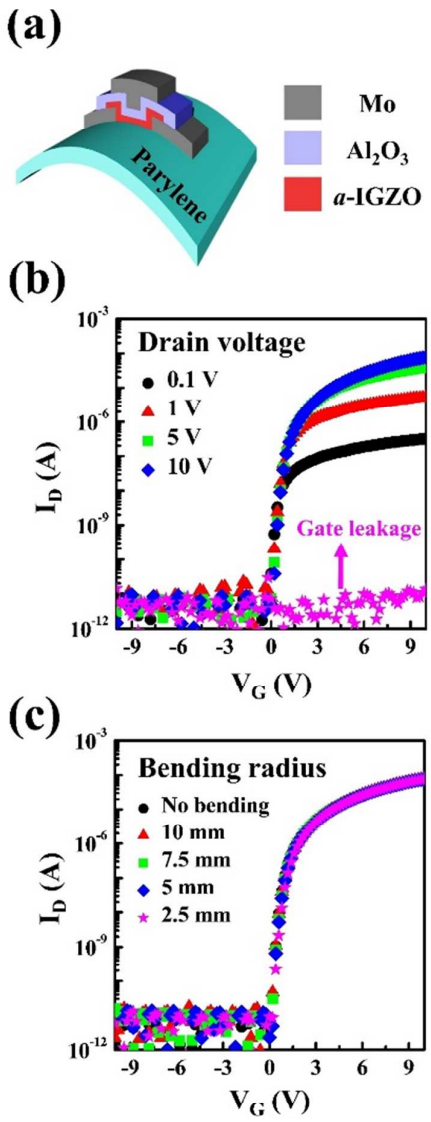


Fig. 7 (a) Schematic of the flexible *a*-IGZO TFT structure. (b) Transfer characteristics of an *a*-IGZO TFT fabricated on an ultra-thin Parylene substrate. (c) Variation in transfer characteristics of the a-IGZO TFTs under extreme bending stress (2.5~10 mm).

effect mobility (μ_{FE}) and the subthreshold swing (SS) values were estimated using the following equations.[5,22,23]

$$\mu_{FE} = \left[\frac{Lg_m}{C_i W V_D}\right]_{max} \qquad SS = \left[\left(\frac{d\log I_D}{dV_G}\right)_{max}\right]^{-1} \qquad (1)$$

where W, L, gm C_i, and V_D are the channel width, channel length, trans-conductance, gate insulator capacitance per unit area, and drain voltage at the linear region, respectively. The μ_{FE} and SS values of the ultra-thin IGZO TFT were determined to be 12.6 $cm^2/V{\cdot}s$ and 0.2 V/dec, respectively, as shown in Fig. 7(b). As shown in the figure, this TFT has good performance. Bending tests of ultra-thin TFTs with thicknesses of 10 µm were carried out using very small radii of 2.5, 5, 7.5, and 10 mm. As shown in Fig. 7(c), the IGZO TFT had nearly identical transfer curves without breaking the gate dielectric.[25] Interestingly, the as-fabricated ultra-thin high-performance devices also showed good reproducibility and mechanical flexibility under the ultimate bend condition due to the use of very thin substrates. When an inorganic film is deposited on a thin and compliant substrate, the stress in the film is significantly reduced and the neutral surface shifts from the middle to the film, resulting in the reduction of the strain on the top surface consisting of inorganic materials.[26] Also, the strain (σ) applied to the sample is estimated using $D/2R$, where D is the total thickness (film and substrate) and R is the bending radius.[10,27] Therefore, the decrease of D value from ultra-thin flexible substrate induces the reduces the strain under the same bending radius.

Conclusions

We have optimized the floating process with water soluble PVA sacrificial layers for ultra-thin devices. The PVA sacrificial layers were produced with various molecular weights and spin coating conditions, and their morphological and detachable characteristics were investigated. The PVA films prepared with 13,000 M_w and 2000 RPM had a smooth surface and quick floating time. PVA residues began to appear after thermal treatment at 200 °C, and it indicated that the oxide TFTs could be safely fabricated below 200 °C on Parylene substrates with 10 µm thickness and area mass of 0.95 g/cm^2. Our flexible oxide TFTs exhibited good field-effect mobility and SS values of 12.6 $cm^2\ V^{-1}\ s^{-1}$ and 0.19 V/dec, respectively, and showed identical transfer characteristics during extreme bending. These results suggest that the floating process is an adequate and convenient method for the fabrication of ultra-thin electronic devices with regard to sample handling, large scale, low cost, electrical performance, etc.

Acknowledgements

This work was supported by National Research Foundation of Korea (NRF) grant funded by Basic Research Lab. project of the Korea government (MSIP) (2014R1A4A1008474), and was also supported by the Human Resources Program in Energy Technology of the Korea Institute of Energy Technology Evaluation and Planning (KETEP) granted financial resource from the Ministry of Trade, Industry & Energy, Republic of Korea (20154030200870).

Notes and references

1 A. N. Sokolv, B. C. Tee, C. J. Bettinger, J. B. Tok and Z. Bao, *ACS Appl. Mater. Inter.,* 2012, **45**, 361–371.
2 G. Schwartz, B. C. Tee, J. Mei, A. L. Appleton, D. H. Kim, W. H. Wang and Z. Bao, *Nat. Commun.*, 2013, **4**, 1859-1867.
3 T. Someya, Y. Kato, T. Sekitani, S. Iba, Y. Noguchi, Y. Murase, H. Kawaguchi and T. Sakurai, *P. Natl. Acad. Sci. USA*, 2005, **102**, 12321–12325.

4 K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, *Nature*, 2004, **432**, 488-492.
5 S. H. Kim, C. H. Ahn, M. G. Yun, S. W. Cho and H. K. Cho, *J. Phys. D: Appl. Phys.,* 2014, **47**, 485101.
6 Z. Bao, *Adv. Mater.*, 2000, **12**, 227-230.
7 D. H. Son and D. H. Kim, *Nat. Nanotechnol.,* 2014, **9**, 397-404.
8 T. Sekitani, U. Zschieschang, H. Klauk and T. Someya, *Nat. Mater.*, 2010, **9**, 1015-1022.
9 T. Sekitani, H. Nakajima, H. Maeda, T. Fukushima, T. Aida, K. Hata and T. Someya, *Nat. Mater.*, 2009, **8**, 494-499.
10 T. Sekitani, Y. Kato, S. Iba, H. Shinaoka and T. Someyaa, *Appl. Phys. Lett.*, 2005, **86**, 073511.
11 U. Zschieschang, F. Ante, T. Yamamoto, K. Takimiya, H. Kuwabara, M. Ikeda, T. Sekitani, T. Someya, K. Kern and H. Klauk, *Adv. Mater.*, 2010, **22**, 982–985.
12 G. A. Salvatore, N. M. nzenrieder, C. Barraud, L. Petti, C. Zysset, L. Buthe, K. Ensslin and G. Troster, *ACS Nano*, 2013, **7**, 8809-8815.
13 G. A. Salvatore, N. Munzenrieder, T. Kinkeldei, L. Petti, C. Zysset, I. Strebel, L. Buthe and G. Troster, *Nat. Commun.*, 2014, **5**, 2982.
14 J. Zaumseil, T. Someya, Z. Bao, Y. L. Loo, R. Cirelli and J. A. Rogers, *Appl. Phys. Lett.*, 2003, **82**, 793-796.
15 E. W. Merrill, E. W. Salzman, P. S. L. Wong, T. P. Ashford, A. H. Brown and W. G. Austen, *J. Appl. Phys.*, 1970, **29**, 723-730.
16 M. A. Spivack*, Rev. Sci. Instrum.*, 1970, **41**, 1614-1617.
17 T. Godaa, T. Konno, M. Takai and K. Ishihara, *Colloids. Surface B.*, 2007, **54**, 67–73.
18 S. Y. Lee, *Trans. Electr. Electron. Mater*., 2015, **16**,139-141.
19 D. B. Hall, P. Underhill and J. M. Torkelson, *Polym. Eng. Sci.*, 1998, **38**, 2039-2045.
20 Q. Huang, I. Yoon, J. Villanueva, K. Kimb and D. J. Sirbuly, *Soft. Matter*, 2014, **10**, 8001–8010.
21 G. V. N. Rathna, J. P. Jog and A. B. Gaikwad, *Polym. J.*, 2011, **43**, 654–661.
22 S. Sugumaran, C. S. Bellan, D. Muthu, S. Raja, D. Bheeman and R. Rajamanif, *RSC Adv*., 2015, **5**, 10599–10610.
23 C. H. Ahn, M. G. Yun, S. Y. Lee and H. K. Cho, *IEEE Electron. Dev.*, 2014, **61**, 73-78.
24 C. H. Ahn, S. H. Kim, M. G. Yun and H. K. Cho, *Appl. Phys. Lett*., 2014, **105**, 223513
25 G. Cantarella, N. Münzenrieder, L. Petti, C. Vogt, L. Buthe, G. A. Salvatore, A. Daus and Gerhard Troster, *IEEE Electr. Device L.,* 2015, **36**, 781-783.
26 S. Wagner, H. Gleskova, I. C. Cheng and J. C. Sturm, in *Flexible Flat Panel Displays*, ed. G. P. Crawford, John Wiley and Sons, Ltd., 2005, **12**, 263-282
27 H. C. Lai, Z. Pei, J. R. Jian and B. J. Tzeng, *Appl. Phys. Lett.*, 2014, **105**, 033510.

SUNG KYUN KWAN UNIVERSITY

School of Advanced Materials Science and Engineering

2066 Seobu-ro, Jangan-gu, Suwon, Gyeonggi-do, 16419, Korea
TEL +82-31-290-7364, FAX +82-31-290-7410
E-mail : chohk@skku.edu

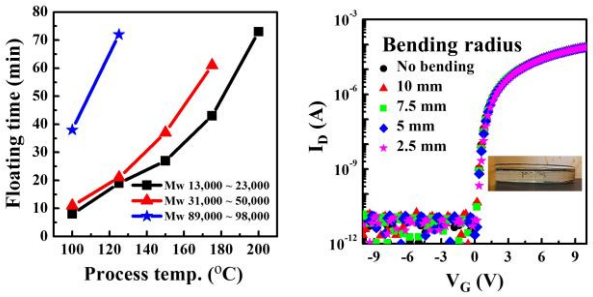
Mar 10, 2016

Editorial Office: ***RSC Advances***

Title: **Expedient floating process for ultra-thin InGaZnO thin-film-transistors and their high bending performance**

Author: **Won Jun Kang,** Cheol Hyoun Ahn, Myeong Gu Yun, Sung Woon Cho, Ye Kyun Kim, Da Eun Kim, Bora Kim, **Hyung Koun Cho*** and Yunseok Kim

Polyvinyl alcohol with low molecular weight exhibited good surface morphology and quick floating time for the fabrication of the top-gate oxide TFTs.



Sincerely yours,

Hyung Koun Cho

Corresponding Author: Hyung Koun Cho

Telephone number: +82-31-290-7364 Fax number: +82-31-290-7410

E-mail : chohk@skku.edu