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Substrate Dependent Resistive Switching in Amorphous-HfOx Memristors: An Experimental and Computational Investigation†

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ABSTRACT While two-terminal HfO_X (x<2) memristor devices have been studied for ion transport and current evolution, there have been limited reports on the effect of the long-range thermal environment on their performance. In this work, amorphous-HfO_X based memristor devices on two different substrates, microscopic glass (~1 mm) and thin SiO_2(280 nm)/Si, with different thermal conductivities in the range from 1.2 to 138 W/m-K were fabricated. Devices on glass substrates exhibit lower reset voltage, wider memory window and, in turn, a higher performance window. In addition, the devices on glass show better endurance than the devices on the SiO_2/Si substrate. These devices also show non-volatile multi-level resistances at relatively low operating voltages which is critical for neuromorphic computing applications. A Multiphysics COMSOL computational model is presented that describes the transport of heat, ions and electrons in these structures. The combined experimental and COMSOL simulation results indicate that the long-range thermal environment can have a significant impact on the operation of HfO_x-based memristors and that substrates with low thermal conductivity can enhance switching performance.

Keywords: Metal Oxide based memristor, Valance change memory, Resistive switching, Digital and analog switching, Oxygen vacancies/ ions migration

INTRODUCTION

Metal Oxide (MO) based resistive random access memory (ReRAM) devices have been drawing a lot of attention recently for their various potential applications, including neuromorphic computing.[1-3] Many researchers have demonstrated that a hybrid system, composed of complementary metal oxide semiconductor (CMOS) neurons and memristor synapses, can support important neuronal functions such as spike timing dependent plasticity (STDP).[4, 5] Wang et *al.* have reported that a diffusive memristor and its dynamics can accomplish a direct emulation of both short- and long-term plasticity of biological synapses, while other researchers have established MO based synapses at the device level.[6, 7]

Among the typical binary transition MOs (e.g. TiO_2, TaO_2, ZrO_2 and HfO_2), HfO_X ($x<2$; sub-stoichiometric) is very popular as a valance change memory (VCM) material due to its promising physical and chemical properties, such as good scalability (< 10 nm), fast switching speed (~ ns), and fair switching endurance (≥ 10^{10} cycles).[2, 8, 9] Oxide-based VCMs are one type of memristive device, where changes in the resistance or conductance can be induced by redox reactions in the oxide within a filament or at the oxide−electrode interfaces under DC bias voltage or a given voltage pulse.[10, 11] HfO_X is both chemically and physically stable and also compatible with CMOS technology.[9] Amorphous (a)-HfO_X offers a few additional advantages, such as high uniformity over large area, low temperature synthesis and controlled electrical properties.[12] To date, both amorphous and poly-crystalline stoichiometric and sub-stoichiometric (oxygen deficient) HfO_X based memristors have been studied experimentally and computationally,[12-18] and more importantly, stand-alone synaptic devices have been demonstrated.[19] While there has been significant prior research related to digital switching in filamentary adaptive HfO_2, there has been a very limited fundamental understanding related to the primary factors controlling analog

resistance change.[3, 20] The analog synaptic properties of HfO_X such as multilevel set and reset states need further investigation. It is worth noting that biological synapses show analog behavior with multilevel synaptic weight changes, and analog conductance (or resistance) change of two-terminal MOs based memristor devices is quite similar.[3] Recent research efforts along these lines have made a lot of progress. For example, Long et *al.*[8] have observed the sharp and gradual reset process in unipolar switching in HfO_2, while a compliance-free, digital set, and gradual-reset has been reported in TaO_x by Abbas et *al.*[10]

Forming a conductive filament (CF) in the MOs involves a creation of oxygen-deficient (or metal rich) region that requires breaking metal-oxygen bonds followed by migration of oxygen anions and/or vacancies; both of these processes are controlled by the local temperature field and the applied electric field.[1, 3, 21] As a result, a “filamentary based” memristor operates at extremely harsh conditions of electric field up to 10 MV/cm and current density ~1 MA/cm^2 or above.[13] It is well accepted that bipolar device behavior is controlled by the motion of negatively charged oxygen ions (or the positively charged oxygen vacancies) through a conducting filament (CF).[22, 23] However, very little is known about how the thermal boundary materials (TBMs) affect the oxygen ions’ drift, diffusion, and CF evolution process.[24-26] The main difficulties in understanding the device behavior is that the filament has been measured to be on order of a nanometer in diameter and re-oxidation of the filament tip only occurs about a nanometer in distance from the oxygen reservoir near the top electrode (TE) as shown in Fig.1 (top).[16, 17, 26-28] Local temperature rises as high as 1000 K have been reported, which depends on the thermal conductivities of the oxide layer, filament, electrodes, and substrate.[14, 25] Since both the drift and diffusion of the oxygen ions and/or vacancies can occur simultaneously, it is very difficult to quantify the digital or analog switching behavior that can occur on the nano-second timescale.[25, 29] A variety of approaches,

including computational and experimental methods, have been used to explain fundamental processes association with vacancy/ion migration at the metal-oxide interfaces.[14, 17, 30, 31] Syu et *al*. showed that the high-speed resistive switching (RS) behaviors of a memristive device is due to only a few atoms involved in the redox reactions and mixed ionic-electronic transport at the interface, which makes experimental study even more complicated.[29] Recently, Kim et *al.* studied TaO_x device behavior using three different TEs, namely: Pd, Ru, and W, with thermal conductivity values in the range of 71.8 to 173 W/m-K, and reported the effect of the TBMs on overall resistive switching.[26] However, the use of different TEs to study the effect of TBMs can be misleading as other properties of the top electrode, like its work function, oxygen affinity *etc.*, can heavily affect the RS. Although TiO_2 and HfO_2 based memristors have been fabricated on flexible (e.g. plastic) substrates,[12, 32] a systematic study of the impact of the thermal conductivity of the substrate has not been performed.

In this work, the performance of 5 nm sub-stoichiometric a-HfO_X ($x \approx 1.8$) based memristor devices, fabricated on either thin SiO_2(280nm)/Si or microscopic glass (~ 1 mm) substrates, are compared and reported. The thin SiO_2(280 nm)/Si substrate has an effective thermal conductivity of 138 W/m-K, whereas the glass substrate has a thermal conductivity of 1.2 W/m-K. Experimental results for electroforming, digital (abrupt) set, analog (gradual) reset and endurance were compared. A Multiphysics COMSOL model that simulates the simultaneous drift, diffusion and thermophoresis of oxygen vacancies was used to estimate the local and temporal temperature profile and its effect on the overall device performance. The comparison of current-voltage (I-V) curves from the COMSOL model and those from the experiments provide the validity of the chosen approach in these models. Our combined experimental and modeling findings provide critical insights into the impact of the long-range thermal environment on memristor operation.

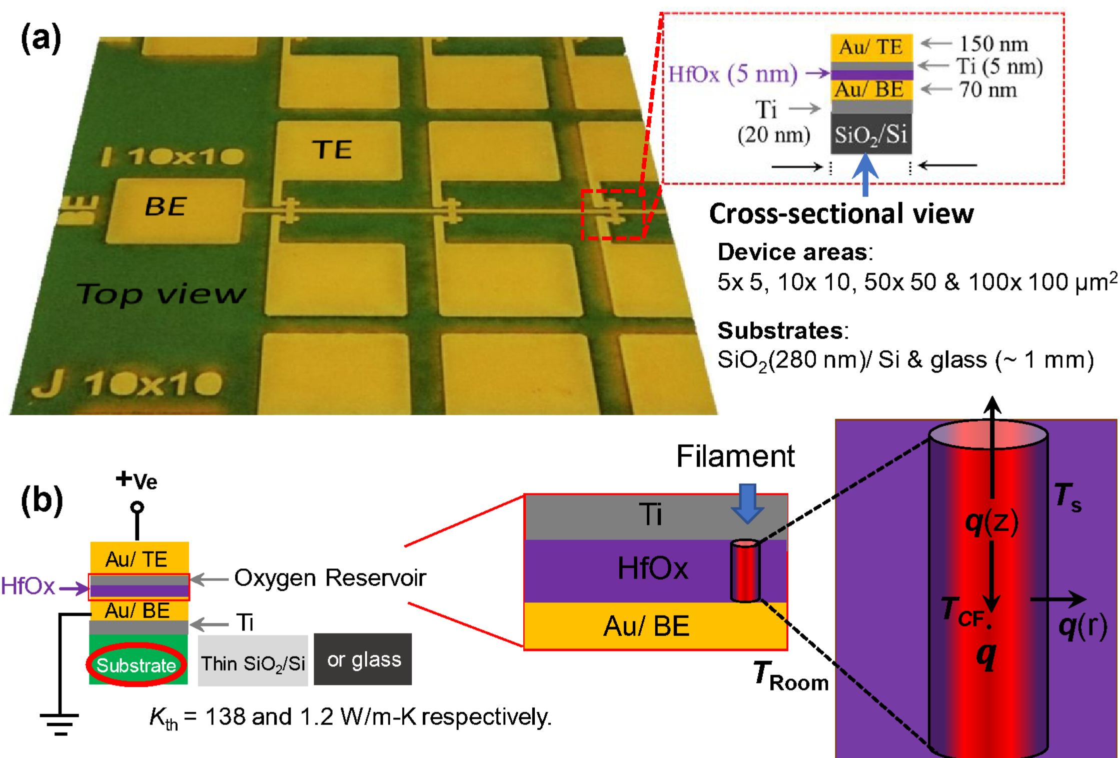

Fig. 1 (a) Schematic of the as-prepared Au (BE)/HfO_x/Ti/Au (TE) devices, 2D views: (left) Top- and (right) cross-sectional views. (b) A typical electrical characterization set up and the process of filament formation: (left to right) substrates thermal properties, device layers, and nanoscale filament formation in HfOx. Arrows showing the heat transfer directions, namely: axial q(z) and radial q(r), from the filament to the surroundings. Note: drawings are not to scale.

RESULTS AND DISCUSSION

Prior to characterizing the resistive switching behavior, it is important to first demonstrate that the substrates did not impact the intrinsic structure and behavior of the materials and devices. Figs. 2 (a) and (b) show the capacitance and initial resistance of the devices, of different areas in the range: 5×5 to 100×100 μm^2, measured prior to forming the devices. Results show that the measured capacitance (at 10 KHz) increases linearly as a function of device area but is independent of substrate for a given area. For example, the capacitance of both the devices on thin SiO_2/Si and glass substrates of sizes 100 and 10,000 μm^2 are measured to be ~ 5.0 and ~500.0 pF, respectively.

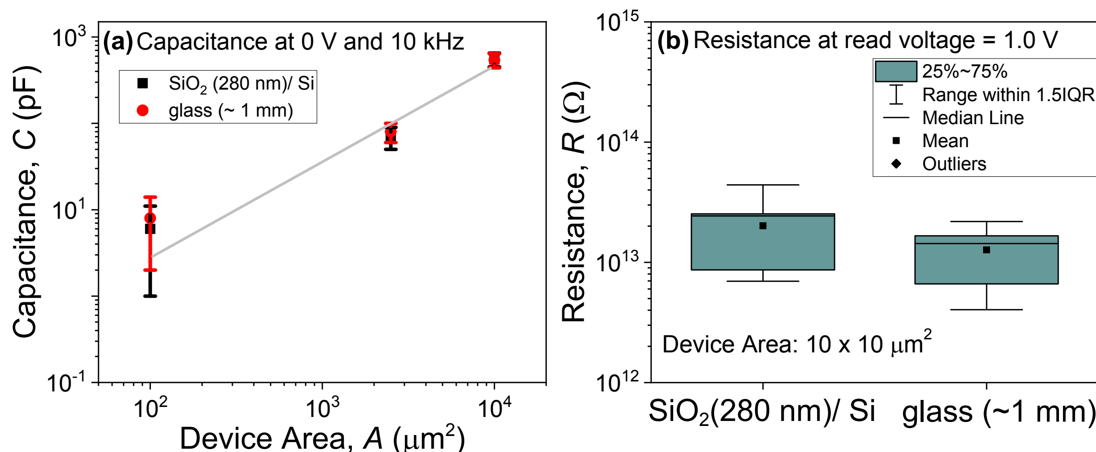

Fig. 2 Electrical properties of the Au (BE)/a-HfO_x/Ti/Au (TE) pristine devices, i.e. before electroforming, deposited on SiO_2(280 nm)/Si and glass (~ 1 mm) substrates: (a) Capacitance of three different sizes and (b) Resistance of 10 ×10 μm² size devices as indicated. The error bars are obtained from 18 devices of each specified.

These results agree well with the thickness of oxide layer (~ 5 nm) while considering the devices as a parallel plate capacitor, whose capacitance can be estimated from: $C = (\varepsilon_o \varepsilon_{ox} A)/t_{ox}$; where ε_o, ε_{ox} and t_{ox} are the permittivity of vacuum (= 8.85×10^{-12} F.m^{-1}), dielectric constant (HfO_x ~ 20) and thickness of the oxide layer, respectively. Similarly, the initial device resistance is substrate independent for the given area, A = 10 × 10 μm² (Fig. 2(b)). The capacitance and initial resistance results, therefore, confirm that the intrinsic electrical device behaviors are substrate independent. These results strongly suggest that any differences in forming and switching behavior are not related to differences in the structure of the active materials.

Fig. 3(a) shows representative results for forming, reset, and set cycles of a device on the thin SiO_2/Si substrate. The resistance decreases by approximately nine orders of magnitude from point A to point E (~10^{13} Ω to ~10^4 Ω). The current from point A to point E at ~3.5 V is small (<10^{-11} and associated with the pristine device behavior without a filament. From ~3.5 V to ~4.0 V (point B to point C), there is a formation of an initial filament resulting in a significant increase in the

current by approximately two orders of magnitude. From point C point D (~4.0 to 4.6 V in this example), the current fluctuates. This may indicate that there is a competition of ion-electron migration due to thermal and electrical fields resulting in an increase or decrease in the filament number or size. This step plays a critical role in determining the overall resistance or size/number of the filament(s). Statistical result shows that the forming voltage (V_f) for both thin SiO_2/Si and glass substrates is approximately the same as shown in Fig. 3(b). However, the filament resistance after ~3 V is substrate dependent (*see* Electronic Supplementary Information, †ESI) and it could be attributed to the local heating near the beginning of filament formation (say, near point D). To make a fair comparison of the RS, a stabilization process is performed after the filament formation, as described in detail in the †ESI (S1 to S3).

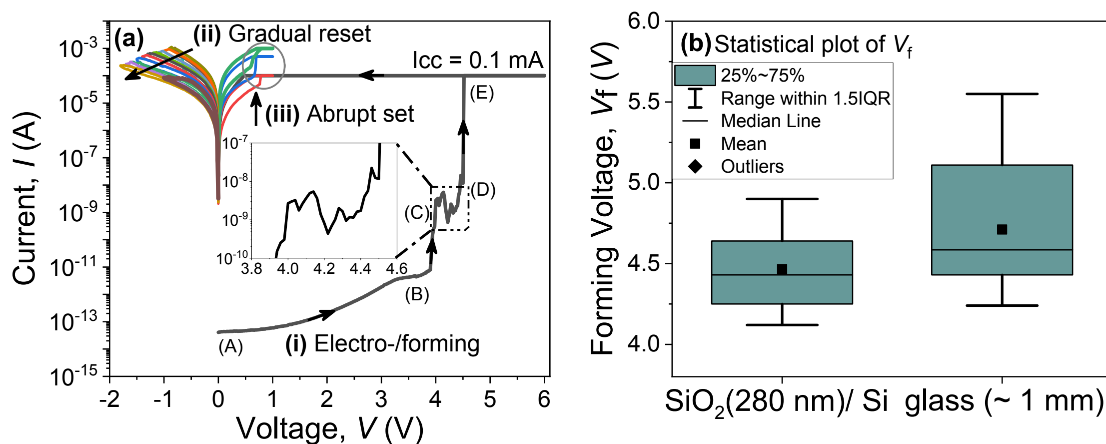

Fig. 3 (a) Electroforming (/or forming; curve (i): (A) to (E)), initial reset (ii) and set (iii) steps of a pristine Au (BE)/a-HfO_X/Ti/Au (TE) device, fabricated on a thin SiO_2(280)/Si substrates. Note that the three steps (i) to (iii) shown in Fig.(a) helps getting stable conductive filament/s and stable resistive switching. (b) Comparison of substrate dependent forming voltage, Vf of 24 devices from each SiO_2(280)/Si and glass (~ 1 mm) substrate.

Fig. 4(a) shows the on state device resistance (R_{on}) immediately following filament formation and stabilization. The glass devices show lower R_{on} than the Si/SiO_2 devices suggesting that the low thermal conductivity substrates assist forming either wider or more filaments. The overall

process of growing wider/more filament(s) could be due to a thermally assisted mechanism during the filament formation or stabilization process. Figs. 4(b), (c) and (d) show the set and reset hysteretic I-V characteristics for maximum reset voltages of -1.0 V, -1.5 V and -1.8 V, respectively. The current following set (reset) for the glass devices is higher (lower) than the Si/SiO_2 devices. Furthermore, the tripping voltage (the voltage at which the device begins to reset) is smaller for the devices on glass as compared to SiO_2/Si. This earlier tripping voltage and smaller LRS (lower resistance state) for the case of glass substrate may be attributed to presence of larger filaments as compared to SiO_2/Si substrates, resulting in a higher current and filament temperature. This means that the filament re-oxidation begins at a lower voltage resulting in a larger HRS (high resistance state), and larger memory window for the glass devices. A higher HRS to LRS ratio (high to low resistance ratio, HLR) of the glass devices, *i.e.* in the range: 4 to 100 with $|V\mathrm{r}| = 1$ to 1.8 V (*see* Fig. S4(b) in the †ESI) confirmed the better performance of the devices on glass.

The digital reset/set of the devices is well explained in the literature with the help of atomically thin barrier layer that is created/destroyed during the reset/set processes.[29] However, there is still lack of a detailed mechanism for the smooth analog reset response of the HfOx based memristor. A more detailed mechanism will be discussed later, in the next section, with the help of a Multiphysics COMSOL simulation results.

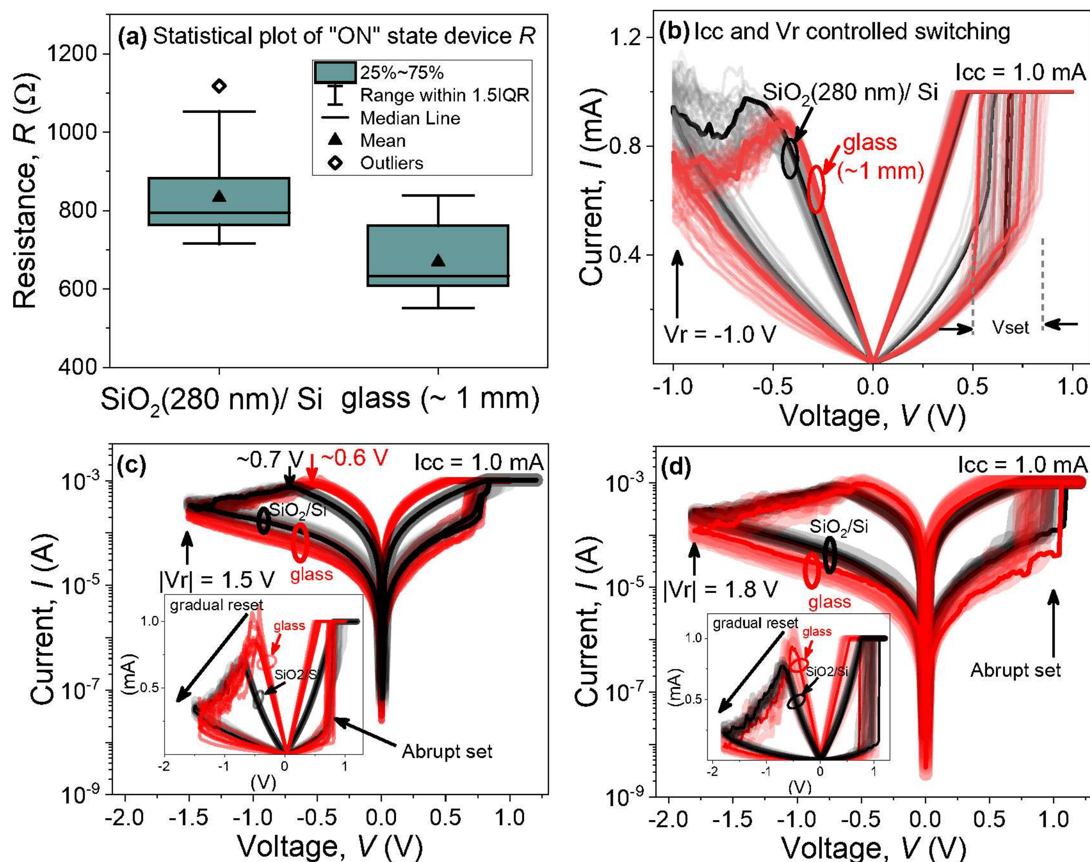

Fig. 4 Substrate dependent resistive switching performance comparisons of the Au/a-HfO_X/Ti/Au (TE) devices: (a) Initial set or ON state device resistance after forming and stabilizing the filament/s and (b)- (d) digital (abrupt) set and analog (gradual) reset switching starting with the same compliance current, Icc = 1.0 mA, but different reset voltages, |Vr| = 1.0 to 1.8 V.

Fig. 5 shows the representative multi-level resistance at various set and reset voltages, each of 100 test cycles for the devices on both thin SiO_2/Si and glass substrates. Results show that all the devices exhibit multi-level resistance (or conductance) values at some appropriate applied voltages. Also, it is evident that the devices on glass substrate retain more distinguishable HRS and LRS values for the same range of set and reset voltages, and they can function without a visible degradation in the operating voltages as shown in Fig.5(a). In other words, the devices on glass substrate exhibited clearly distinguishable memory windows at lower reset voltages (starting from

-0.8 V, in our case), whereas no such reliable separation of LRS and HRS was observed with the devices on SiO_2/Si substrate (results not shown here). As expected, the LRS values of the glass devices are smaller than that of the devices on SiO_2/Si substrate, while the HRS values are greater (*see* Fig.5(a)-(b)). The difference in HRS values becomes more prominent at higher V_r, resulting the higher HLR values of the glass devices as observed in the digital response. Furthermore, it is noteworthy that the cycle-to-cycle variations in the multi-level resistances of the SiO_2/Si devices are slightly higher at the larger reset ($|Vr| \geq 1.5$ V) and set (≥ 1.2 V) voltages. This has previously been attributed to the change in filament size and/or geometry which is extremely sensitive to the stochastic nature of the generation and migration of the oxygen ions and vacancies.[9, 33] Baeumer et *al.* have demonstrated some of the possible sources for filaments' or device variability (*i.e.* including cycle-to-cycle and device-to-device) using photoelectron emission microscopy (PEEM), combined with XPEEM measurements.[33] Previous work has proposed system-level adaptations to account for this device variability.[34] The observed low operating voltages and the multiple HLR values especially of the devices on glass substrate is consistent with the literature of sub-/stoichiometric HfO_X based memristors.[12, 13, 24, 35, 36] The devices on glass substrates exhibited noticeably improved memory window, which agree well with the results from digital switching. The enhanced performance of the devices on glass substrate can be attributed to the fact that both the formation of CF/s and reset switching were favorable with the low heat dissipation from the substrate to the environment. However, it is important to understand that the different filament sizes (and perhaps geometry) for different substrates must be verified with high resolution in-situ transmission electron microscopy (TEM) and/or PEEM studies. To understand these differences in a better way, a 2-D axisymmetric COMSOL model was employed to analyze intermediate

variables such as oxygen vacancy density and temperature, and their effect on the measurable parameters such as current through the device.

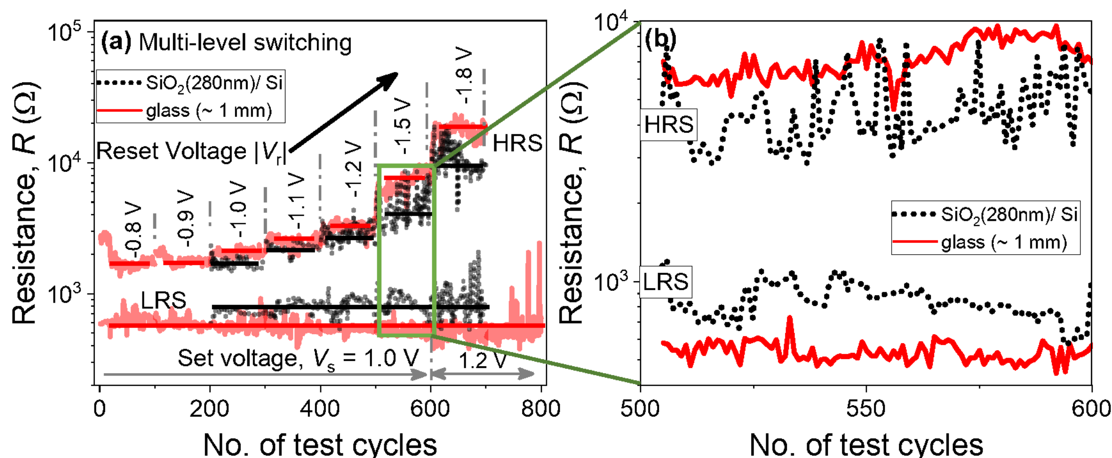

Fig. 5 Substrate dependent analog resistive switching of Au/a-HfOx/Ti/Au (TE) devices: (a) Effect of incremental applied reset voltages (|Vr| = 0.8 to 1.8V), showing multi-level resistive switching starting with different set and reset voltages. (b) (Magnified) Showing the performance of glass and SiO_2/Si devices at 1.0 V (set) and -1.5 V (reset) voltages.

Thermal modeling and experimental validation. The substrate dependent RS performance of the devices with stable CF of known initial size and geometry are discussed in greater details in this section, followed by the experimental results validation. The basic hypothesis of this thermal modeling is that the RS switching behavior of a filamentary device is controlled by both the applied electric field (***E***) and local thermal field, generated via joule-heating. For this, a COMSOL physical model that is reported in our recently published article[37] has been used to analyze the intermediate variables such as local temperature and oxygen defect (vacancy) concentration, so that their role in the device performance can be understood. The thermal model considers the drift, diffusion and thermophoresis of oxygen vacancies that are instrumental in creating and suppressing the CF. The vacancy conservation that includes these phenomena is solved in conjunction with current conservation and energy conservation equations as described in Eq. (1) through (3).

$$\frac{\partial n_V}{\partial t} + \nabla \cdot (v_V n_V) = \nabla \cdot (D_V \nabla n_V) + \nabla \cdot (S_V D_V n_V \nabla T) \tag{1}$$

$$\nabla \cdot \left(\sigma \nabla \psi + \varepsilon \frac{\partial}{\partial t} \nabla \psi \right) = 0 \tag{2}$$

$$\frac{\partial T}{\partial t} = \frac{1}{\rho c_p} \nabla \cdot (k_{th} \nabla T) + \frac{\sigma}{\rho c_p} (\nabla \psi)^2 \tag{3}$$

In these equations, n_v is the density of oxygen vacancies, v_v is the drift velocity of vacancies, D_V is the diffusion coefficient of the same, S_V is the thermophoresis coefficient, σ is the electrical conductivity, ψ is the voltage potential, ε is the permittivity of the oxide material, T is the temperature, ρ is the density, c_p is the specific heat, and k_{th} is thermal conductivity. Eq. (4) is used to calculate the electrical conductivity of the filament as a function of vacancy density and temperature. The use of this equation results in a metal-like filament behavior for high concentration of vacancies and an insulator-type behavior for small number of vacancies. The dependence on temperature at small number of vacancies is amplified using activation energy. For further details of the model, we refer to our recently published work by Pahinkar et *al*.[37]

$$\sigma = \frac{(\sigma_{HfOx} - \sigma_{HfO2})}{n_{V,Max}} n_V e^{\left(\frac{-E_{AC}}{k_B T}\right)} \tag{4}$$

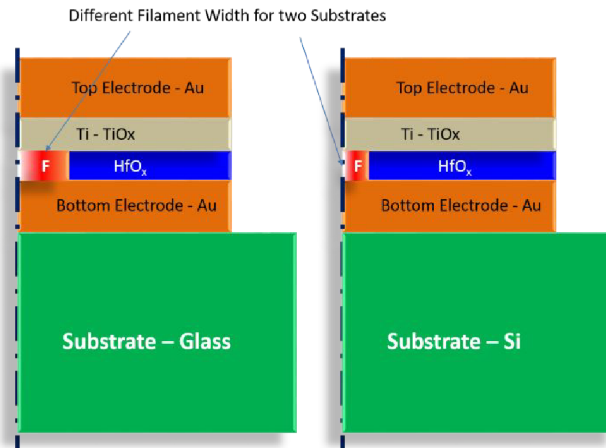

Fig.6. *Illustration of bigger filament for glass substrate (left) and smaller filament for SiO_2/Si substrate (right) considered in the COMSOL simulations.*

Finally, the validity of experimental results is confirmed by taking two different radii of CFs, namely: 3 nm for SiO_2/Si and 4 nm for glass substrates, which are more realistic than taking a single size filament as discussed above. It is crucial to note that different shapes and sizes of the filament/s impacts heavily on the electrical performance of a device, including the I-V curves. A couple of nanometers to tens or even hundreds of nanometers conducting channels are reported in the literature for HfO_x based devices, while the additional effects including different biasing conditions can also affect these sizes remarkably.[2, 29] Therefore, we used the experimental I-V curves to deduce a combination of the electrical conductivity as a function of defect density and filament size, resulting a closely matching I-V profiles. Fig. 7 shows a comparison of I-V curves from the experiments and the model simulations demonstrating a good agreement, especially on the reset side. The earlier tripping voltage of the glass device further confirm the validity of this model: Bigger or wider CF of glass device as shown in Fig. 6, with lower initial resistance, utilizes more power (= V^2/R) forcing the CF to rapture earlier or vice versa.

Table 1 shows the thermophysical parameters considered in the COMSOL simulations that represent the two different substrates and Table 2 shows additional parameters used in the simulations. While the specific heat and density of the two materials are comparable, the thermal conductivity of the thin SiO_2(280 nm)/Si is more than two orders of magnitude greater than that of glass.

Table 1. Thermophysical properties of substrate materials considered in COMSOL simulations.

Parameters	**Glass**	**SiO_2/ Si**
Density, ρ (kg m^{-3})	2230	2320
Specific heat, c_p (J kg^{-1} K^{-1})	840	710
Thermal conductivity, k_{th} (W m^{-1} K^{-1})	1.2	138

The simulation results closely follow the substrate dependent trend for both reset voltage and the memory window and this pattern can be confirmed through the examination of the intermediate variables in the models such as oxygen vacancies and local temperature. The difference in the slope of I-V curves on the HRS side could be attributed to the empirical treatment of the current dependence on temperature. The faster decline in the current of the glass device after the tripping voltage clearly represents higher HRS compared to the SiO_2/Si device. The difference in the two slopes of the I-V curves, namely: from -0.5 V to -1 V and -1 V to 0 V, may indicate that the device reset switching is not only controlled by the CF size but also the substrate's thermal properties. Thus, the observed higher HRS and memory window of glass devices can be attributed to the negligible heat loss, resulting an earlier rapture and re-oxidation of the CF/s. Similarly, a relatively higher electrical power consumed by the devices on SiO_2/Si substrate, that is within the same operating set/ reset voltages, further verifies the higher heat transfer from the filament/s or devices through the SiO_2/Si substrate of as shown in Fig. S5 in the †ESI. Fig. 8 (a, b) sheds light on how the insulating or dielectric barrier is created during the reset stage and breakdown of the barrier takes place during the digital set stage. Because negatively charged oxygen ions move from the capping layer Ti into the filament region and a barrier layer, close to the BE, is created at the end of the reset stage as shown in Fig. 8(a). This barrier layer has a lower electrical and thermal conductivity than the region elsewhere and becomes the bottleneck for the current flow. This layer also increases the local temperature gradient, it being the region of the high potential drop. Thus, an HRS is achieved. When the polarity is reversed to execute the set stage, the temperature increases initially with the current in the off-state and when the temperature reaches a threshold after which the vacancies are mobile, drift and diffusion acting the in the same direction nearly instantaneously cause the breakdown of the barrier layer as seen in Fig.8(b). It can also be seen

that the oxygen ions enter the Ti layer after set, which can be inferred from the fact that the number of vacancies in the Ti layer have dropped. This is consistent with the observed abrupt set for all devices. In conjunction to this, a continuous metal rich filament reestablishes in the HfO_X layer at the end of the set stage.

Table 2. Constants and physical parameters used in set/reset simulations.

Parameter	***Value***
$n_{V,Max}$	2×10^{27} m^{-3}
f	2×10^{10} Hz
a	10^{-10} m
E_a	1.5 eV
$E_{AC,Max}$	0.125 eV
ρ	9680 Kg m^{-3}
c	60 J kg^{-1} K^{-1}
k_{HfOx}	5 W m^{-1} K^{-1}
k_{HfO2}	0.5 W m^{-1} K^{-1}

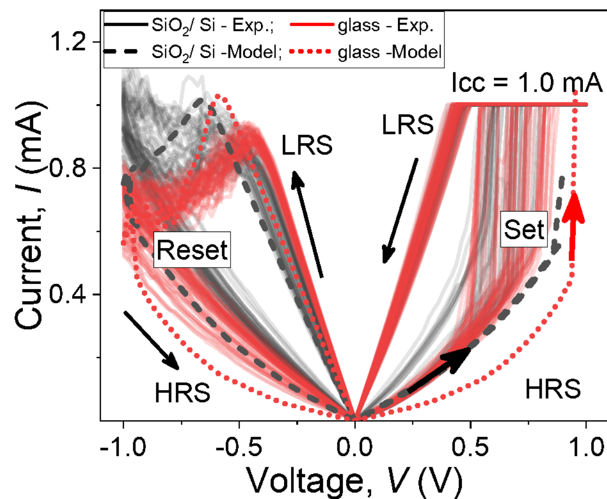

***Fig.** 7 Substrate dependent comparison of I-V plots for thin SiO_2(280 nm)/Si and glass substrates obtained from the experiments and COMSOL model simulations. Note that different sizes of conducting filaments (CFs), namely: 3 and 4 nm in diameter, were used in the modeling for SiO2/Si and glass substrates respectively.*

The role of substrates dependent temperature field on the defect concentration in HfO_X or the oxygen vacancy activation and movement resulting different RS performance was also studied. Fig. 8(c) and (d) show the comparison of the filament tip temperature (at the interface between Ti and HfO_X) and the exposed surface of TE temperature, as a function of voltage, respectively. When the simulations for glass and thin SiO_2 (280 nm)/Si substrates begin with the same initial conditions, the temperature of both the filament tip and the TE in the glass substrate is marginally higher than that in the SiO_2/Si substrate. This is clearly attributed to more heat remaining near the device for the same power (the current and voltage are the same for both substrates), because of the glass thermophysical properties. This means that the temperature required for onset of the migration of vacancies is achieved earlier in the glass device than that in the SiO_2/Si device. As

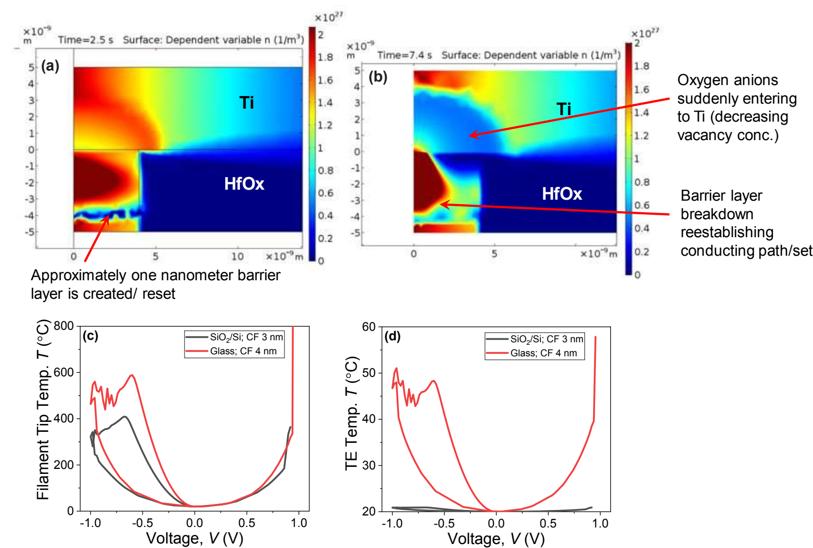

Fig. 8 *(Color online) Oxygen vacancy distribution (a) at the end of the reset stage (b) at the end of the set stage for glass substrate. Substrate dependent temperature of (c) filament tip and (d) top electrode (TE) surface, plotted with the applied voltage for thin SiO_2/ Si and glass substrates. Note that 3 and 4 nm of conducting filaments (CFs) were used in the COMSOL modeling for SiO_2/Si and glass substrates respectively*

the migration begins creating the dielectric barrier, the current begins to drop lowering the temperature as we observed from the experiments (*see* Fig. 7). Although, the difference in the

temperature profiles of filament tip in the set side are not significant for our devices, the impact of substrate material on the TE temperature is more tangible. As seen from Fig. 8(d), the temperature rise in the glass substrate to be more than 40 °C, while that in the SiO_2/Si substrate is less than 5°C. This behavior is obviously due to different fractions of thermal power going upward toward the TE and downward toward the substrate for different substrates. The glass substrate provides more resistance to heat transfer than SiO_2/Si, hence more fraction of the total thermal power in the filament goes toward the TE for glass, thereby showing an appreciable temperature rise. While this study has focused on the fundamental understanding of the impact of thermal boundary materials on analog reset, future work will explore the practical impact of these materials on the set behavior of the device and neuromorphic computing applications and behavior such as long-term potentiation and depression.[38, 39]

Finally, the models were simulated to confirm that the factors considered in the present model that affect the oxygen anions and/or vacancies migration can indeed reproduce the non-volatile nature of the 'memory' or internal resistance of the device. Fig. 9 shows the typical gradual reset I-V curves for a series of $|V\mathrm{r}|$ in the range: 0.5 V to 1.0 V for a glass substrate. The ion migration and barrier layer creation at every voltage step is remembered by the device perfectly validating the approach considered, when compared with the experimental results (*see* Fig. S3(a)). Hur et *al*. also reported a physical model for a bipolar resistive switching behavior, with an experimental validation, for multi-level resistance of Pt/Ta2O5-x/TaO2-x/Pt devices.[42] However, to the best of our knowledge, our type modeling for the non-volatile reset has not yet been reported in the literature for a-HfOx based memristor. The use of this modeling approach to further validate nanoscale ion transport phenomena as a function of current flow and temperature field for HfOx and other MOs exhibiting similar properties is thus warranted and ongoing.

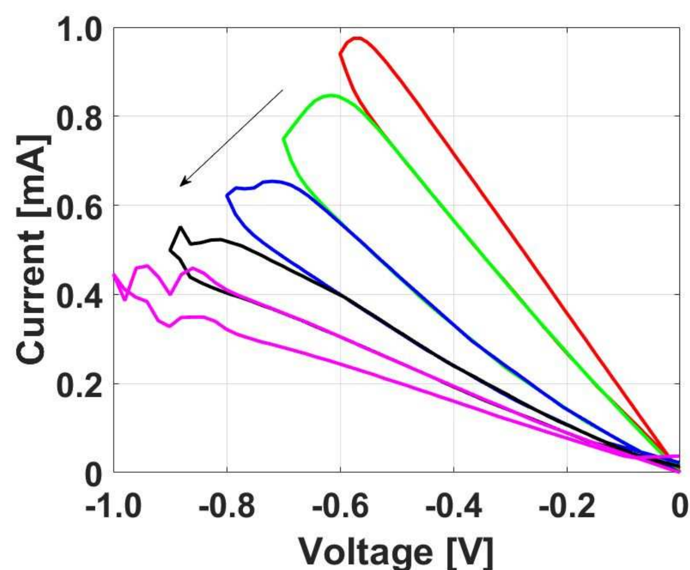

Fig. 9 *The I-V curves from the COMSOL model showing gradual reset with a non-volatile resistance memory.*

CONCLUSION

In summary, Au (BE)/a-HfO_X(5 nm)/Ti/Au (TE) memristor devices were fabricated on two different substrates, thin SiO_2(280 nm)/Si and glass, and characterized to study substrate dependent device behavior. The reported memristor device fabrication technique is simple, scalable, and highly reliable (almost 100% device yield in our case). Our study showed that the bipolar RS, both digital and analog, of the devices is dependent on the thermal diffusivities of the substrates. Devices on glass substrates showed the best RS switching performance, including a wider memory window and a lower reset voltage, than the devices on SiO_2/Si substrates. This is attributed to the low thermal conductivity of the glass, enabling the device to hold the temperature and hence improve performance due to favorable diffusion of oxygen ions at the HfO_X -Ti interface. Comprehensive computational modeling results confirm that the oxygen ions move back and forth between the Ti "capping layer" and the HfO_X "active oxide layer" during reset and set stages. The

movement of ions is reported as a primary function of applied electric field, thermophoresis, and diffusion, while the kinetics are governed by the material properties of the substrates. Our results indicate that the a-HfO_X based memristor devices can be a promising candidate for neuromorphic computing. However, for commercial production, besides the requirement of device size and behavior, other physical parameter and limitations such as compatibility of substrates, device packaging *etc.*, could affect the RS switching, and therefore, it may require an extensive study to further improve the analog response of these devices.

Experimental Section

Device fabrication. All devices were fabricated on about 1"x 1" square size cleaned substrates. The Si (Orient: <100>, test grade) wafer were procured from University Wafer, and the surface was thermally oxidized to create ~ 280 nm thick SiO_2, using dry oxidation at 1000 °C. While the microscope glass slides (Gold Seal Catalog No. 3010) were used as received. The sneak current path free devices of different sizes were fabricated for different experiments (details are presented in the result section). Prior to spin coating the substrates with negative photoresist, NPR (NR-71 3000P), we cleaned the substrates with organic solvents and piranha solution, then dried with N_2 blower. As described in our recent paper, both the bottom and top electrodes (BE and TE) were patterned using a maskless aligner (Heidelberg Instruments MLA 150),[40] followed by the metal depositions using e-beam evaporation (20 nm and 5 nm Ti underneath the 70 nm BE and 150 nm TE respectively, deposited at the fixed deposition rates 1.0 Å/s). Both the BE and TE layers were deposited using 99.999% Au source at ultra-high vacuum (~$3x10^{-6}$ Torr) and the Ti layers were deposited without breaking vacuum using 99.95% Ti source pellets (Kurt j. Lesker). Note that the 20 nm adhesion layer of Ti film was deposited to improve the adhesivity of Au layer, while the 5 nm Ti was used as a buffer layer (/or oxygen getter capping layer) to improve the oxygen diffusion,

as described in the literature.[5, 31] The HfO_X (~ 5 nm) was synthesized using atomic layer deposition (ALD), Cambridge Nanotech Fiji F202 system. Thermal ALD process was used at 250 °C, with the Tetrakis (dimethylamido) hafnium (TDMA-Hf) and DI water as oxygen precursors. The pulse times for both the precursors (water = 0.06 s and TDMA-Hf = 0.25 s) were fixed for whole deposition cycles. Before depositing the HfO_X film on the actual device's substrate, the deposition rate was confirmed with a test run to ensure the accuracy for the final thickness and used the optimized rate to estimate total number of cycles needed (*i.e.* 45 cycles at 1.12 Å/cycles for 5 nm). Then, the final thickness and the uniformity of the HfO_X films were also confirmed with the multi-point thickness measurements using an ellipsometer (J.A. Woollam M2000), measured to be 5.0 ± 0.1 nm (with uniformity 2%). After the BE and TE deposition, lift-off processes were performed with acetone at room temperature for a period of at least 8 hours. Also, the samples were sonicated for about 30 secs before the final rinse off to remove the PR completely. Finally, the HfO_X film, outside the crossbar region, was etched by reactive ion etch (RIE) starting with SF6/Ar mixture (flow rates: 30/5 sccm) for a minute, setting the RF power at 200 W and the pressure at 40.0 mTorr. It is noteworthy that the as-prepared devices were characterized for the electrical properties without any post-fabrication treatments.

Materials and Device Characterization. As-deposited HfO_X films were characterized for some of the important physical and chemical properties that are required, or at least helpful, to investigate the device RS behavior. For example, amorphous phase was confirmed with glancing angle X-ray diffraction (XRD) measurements (PANalytical Materials Research Diffractometer, MRD), with Cu Kα (λ = 1.540598Å) and 2θ in the range from 20°-80°, at a step size of 0.01°. And, X-ray photoelectron spectroscopy (XPS) was performed for chemical composition using a Thermo Scientific K-alpha XPS system with a monochromated Al Kα X-ray source and a hemispherical

analyzer in constant analyzer energy mode (50 eV pass energy, 0.1 eV step size, and a beam size of 400 μm). From the XPS analysis, the Hf:O ratio was estimated to be 1:1.8, which corresponds to a stoichiometric amorphous $HfO_{1.8}$.

Electrical characterization. All electrical measurements were performed using a Keithley 4200-SCS (Semiconductor Characterization System) and a Cascade Microtech probe station at room temperature and ambient conditions. As reported in our previous work, we characterized the devices with and without an external transistor to confirm if the transistor is required to avoid the possible damages to the devices: For example, permanent damage of the conductive filament or the performance degradation.[41] Bias was applied to the TE while the BE was grounded. For DC sweeping voltage ramping was also fixed (= ±0.02 V) for all measurements in both positive and negative potential windows. Initial device characteristics were compared by measuring the capacitance-voltage (C-V) and initial resistance of the pristine devices, of all four different sizes as mentioned above. Then, the switching performance of 10 x 10 μm^2 size devices, fabricated on both thin SiO_2(280 nm)/Si and glass substrates, were measured and analyzed. Please note that all the test devices, on both glass and SiO_2/Si substrates, were characterized without using the thermal paste; and this can cause a slight change in the device behavior that might be not easy to quantify.

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†***Electronic Supplementary Material (ESI)***: Substrate dependent conductive filament (CF) formation; The CF/s stabilization; The current-voltage (I-V) curves of stabilized CF/s; Substrate dependent switching with the stable CF/s at different reset voltages; and Substrate dependent power consumption. This material is available free of charge *via* the Internet at http:// http://www.rsc.org.

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Table of Contents (TOC):

Long-range thermal environment makes significant impact on resistive switching in amorphous-HfOx (x ~ 1.8) memristors; and the substrate of low thermal conductivity improved both the digital and analog switching performance.