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Facile fabrication of sponge-like porous micropillar arrays via electrochemical process

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A large variety of synthetic methods have been developed for hierarchical porous materials, by which the performance of a wide range of applications can be dramatically enhanced. Herein, hierarchical porous micropillar arrays is demonstrated by employing electrochemical etching to silicon micropillars. The approach relies on the steering of current flow through the three-dimensional silicon-electrolyte interface to enable nanopores to grow on the entire surfaces of the micropillars simultaneously. The pores grow perpendicular to the surfaces of micropillars, whereas the pore diameter and porosity vary depending on the locations of the surfaces. The finite element analysis shows that the spatial variation of the pore diameter and porosity is determined by the distribution of current density. Further, the thickness of the porous layer can be tuned by etching time so that a sponge-like porous structures is conveniently obtained by regulating the etching time. In addition to the effect of current density flowing through the etched surfaces, the growth of pores also depends on the crystal orientations of the etched surfaces. The etching results on square micropillar arrays and microgroove arrays show that the growth direction and rate of nanopores inside the microstrucutre also depend on the exposed crystal planes. The facile characteristics of the fabrication method can serve as an effective route for a wide range of applications of porous materials with enhanced capabilities.

Introduction

Nanostructured silicon is of great interest to a wide range of research and applications, including drug delivery[1,2], biosensors[3-6], electrochemical batteries[7-9], microfluidics[10,11] and heat transfer.[12,13] Depending on the applications, silicon can be tailored into different structural morphologies to implement specific functionalities. For example, with a relative high porosity and inner volume, mesoporous silicon has been used as the carrier of different payloads such as proteins, enzymes, and drugs. On the aspect of biosensors, the nanoporous silicon biosensors have been developed as high-sensitive optical platforms for the detection of molecules since its first demonstration more than 20 years ago. For electrochemical batteries, mesoporous silicon particles have also been utilized as the anode in lithium-ion batteries due to its high specific capacity and anti-pulverization behaviour. For microfluidics, nanostructured silicon membranes have been integrated into microfluidic devices to realize the separation of the molecules with different diameters. It has also been demonstrated that pool boiling heat transfer can be significantly enhanced by decorating silicon nanowires on a smooth silicon surface.

Due to the versatility of nanostructured silicon, strategies to fabricate nanostructured silicon including anodic oxidation[14,15], galvanic etching[16,17], stain etching[18] and metal-assisted chemical etching[19,20] have been widely studied over the past decades. In general, current processing strategies can be classified into two categories: electrochemical etching process and electroless etching process. The electrochemical etching method is mostly used to form porous structures, such as nanoporous membrane and micro particle with nanopores on it. Stain etching and metal-assisted chemical etching belong to the electroless method, mostly used to fabricate silicon nanowires. For the electroless etching, the etching process is crystal-orientation dependent, and the silicon nanowire propagates primarily in the <100> orientation.[21] Although the etching orientation can be altered by adding different chemical oxidants (e.g. nitric acid and hydrogen peroxide) into the etching solution[13,22], the etching process is difficult to control and less reproducible than the electrochemical etching.[23] Recently, design and fabrication of hierarchical structures on different materials have attracted great attention, because of the great potential in surface engineering, thermal management, electrochemical battery, and drug delivery applications, etc. However, it is difficult to directly fabricate hierarchical structures on silicon substrate using the aforementioned conventional methods. To date, a variety of novel hierarchical porous silicon structures have been developed by the fabrication methods that can be classified into two categories: the bottom-up approach and the top-down approach.[24-31] For example, three dimensional hierarchical macro-/ mesoporous silicon has been realized using a bottom-

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up method. This novel structure can effectively accommodate volume expansion upon lithiation, which is promising for the anodes of batteries.[24] The top-down method to obtain hierarchical porous silicon structures relies on the tailoring of silicon substrate to be etched.[28-30] For example, Ruminski et al. demonstrated the preparation of a nonplanar multi-layered porous silicon that is conformal to the original surface topology using microcontact printing and electrochemical etching.[29] More recently, Krueger et al. reported the fabrication of hierarchical porous silicon structures with lateral nanopores to serve as gradient refractive index micro-optics.[32] However, the structural feature was not revealed in detail and a systematic investigation on the mechanism for the structure formation was not reported. To our best knowledge, anisotropic formation of nanopores on micropillar arrays has been seldom reported. In this work, we report a facile scheme employing electrochemical etching on pre-patterned silicon substrate for the fabrication of a novel hierarchical nanoporous microstructure, namely sponge-like porous micropillar arrays. In contrast to the conventional electrochemical etching processes applied to planar silicon substrates, we apply the electrochemical etching process to non-planar microstructured silicon substrates to create nanopore hierarchy onto the microstructures. By systematic characterization of the detailed structural features including the spatial variation of pore morphology and the anisotropic alignment of pores, a formation mechanism governed by the current density and exposed crystal plane is proposed.

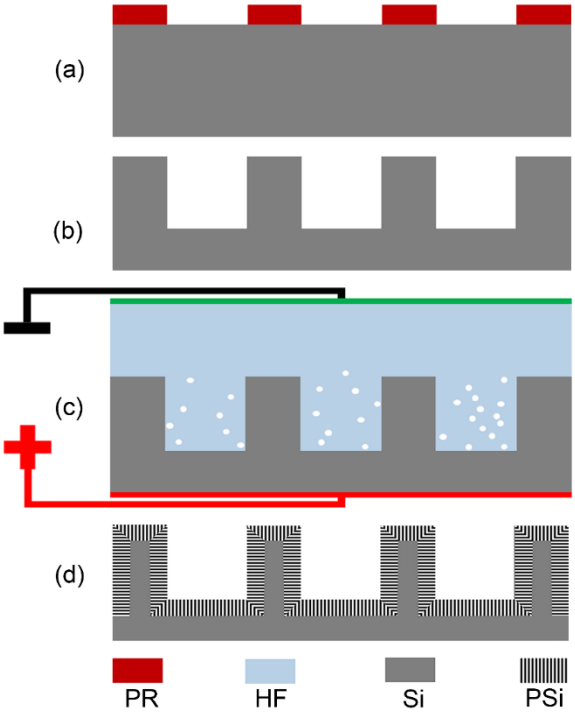

Fig. 1 Schematics of fabrication process. (a) Patterning of photoresist (PR) by photolithography. (b) Formation of micropillar arrays of silicon by deep reactive ion etching (DRIE) process. (c) Electrochemical etching in hydrogen fluoride (HF) solution under constant anodic current condition. (d) Illustration for sponge-like porous microstructure arrays.

Fabrication scheme

Fig. 1 shows the fabrication process of the proposed scheme for sponge-like porous micropillar arrays of silicon (see Experimental section for details). Micropillar arrays are first obtained by the photolithographic process (Fig. 1a) and deep reactive ion etching (DRIE, Fig. 1b) on silicon substrate. Then, the as-prepared sample is immersed in a hydrogen fluoride (HF) solution under anodic bias condition in order to create a nanoscale porous layer over the surface of micropillar arrays (Fig. 1c). During the etching, all surfaces including the top, sidewall, and bottom surfaces are in contact with the electrolyte and the reaction occurs on all surfaces simultaneously. The thickness of the nanoporous layer depends on the time of electrochemical reaction. With a prolonged reaction time, the micropillar arrays will be transformed to a sponge-like porous structure.

Results and discussion

Current distribution around a microstructure

The formation of pores in electrochemical etching process depends not only on the crystal orientation of the etched surface but also on the current flow through the interface.[10,33] To analyse the feasibility of the proposed scheme, finite element analysis has been conducted to compute the electric field and current distribution over the microstructured silicon surface (see FEA Methods and Fig. S1 in Supplementary Information for detailed simulation method and model). As shown in Fig. 2a, the electric potential distribution is distorted around the micropillar structure because of the presence of the three-dimensional (3D) micropillar geometry. As a result, the current flow is steered by the protruding microstructure through the non-planar silicon-electrolyte interface and perpendicular to the silicon-electrolyte interface, as indicated by the arrows in Fig. 2a. The current distribution reveals that the current flow can be led through a perpendicular path to the interface by tailoring the shape of the silicon electrode. In addition to the current direction, the current density is also a key parameter during the electrochemical reaction. In order to obtain the current density distribution, the electric field distribution was first computed. Similar to the edge effect in a capacitor, the electric field distribution should also be non-uniform, especially around the corners of the silicon electrode. Fig. 2b shows the electric field intensity reaches the maximum at the top convex corner of the microstructure and reduces monotonically along the sidewall to the minimum at the bottom concave corner. Over the top surface, the electric field intensity decreases from the edge to the centre. According to Ohm's law, the current density, which is directly proportional the electric field, is computed for the sidewall, top, and bottom surfaces, respectively (Fig. 2c, 2d, and 2e). Although the current direction is perpendicular to the interface, the current density flowing through the interface varies spatially. For the growth of porous silicon, pore morphology depends highly on the applied current density.[35,36] Thus, the non-uniform distribution of the current density flowing across the interface may imply the variation of

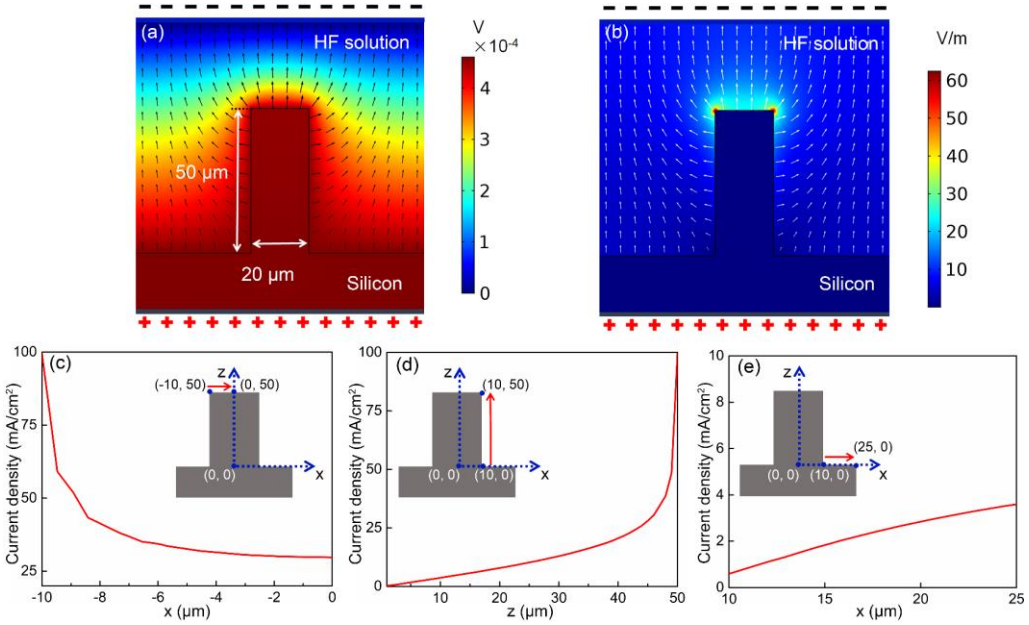

Fig. 2 Finite element analysis results. (a-b) The distribution of electric potential and electric field along the microstructured silicon surface, respectively. (c-e) Current density distribution along the top surface, sidewall, and bottom surface, respectively. The red arrows in Fig. 2c-2e indicate the directions in which the current density changes.

pore morphologies over the silicon electrode. Additionally, simulations with micropillars of three different aspect ratios were conducted under identical boundary conditions to investigate the effect of geometrical parameters on the current distribution along the surface（see Fig. S2 in Supplementary Information). The results show that the current still flows perpendicularly through the interfaces regardless of the micropillar's aspect ratio. Besides, the changing trends of the current density across the interface are also consistent with each other independent of the aspect ratio. It should be noted that the current density reaches the maximum at the top corner, which appears to have a positive correlation with the aspect ratio (Fig. S3). It suggests that the aspect ratio should not be too high to prevent excessive current around the edge, thereby avoid electropolishing. Considering the coupling effect of electrical field within the multiple micropillar structures, we also examined the situation of two adjacent micropillars and performed further simulation for the coupling effect (Fig. S4). The results show that although the electric field coupling has impact on the current distribution between the adjacent micropillars, the overall picture shows the same changing trend with the case of a single micropillar.

Pore formation and distributions around the micropillar

Fig. 3 shows the fabrication results of 30-min electrochemical etching of the silicon micropillar arrays. The micropillar arrays were designed to have a hexagonal distribution with diameter of 20 μm, pitch of 50 μm, and height of 50 μm. As shown in Fig. 3a, the original geometry and size of the micropillar arrays are not changed significantly by the electrochemical etching. The nanoscopic scallops along the sidewall resulted from the DRIE process is still retained even after the electrochemical etching. Meanwhile, the results show that nanoscale pore structures with diameter less than 50 nm are created over all surfaces by the electrochemical etching, especially in lateral direction along the sidewall (Fig. 3c-3e) and vertical direction on the top (Fig. 3a and 3b) and bottom (Fig. 3f) surfaces. To verify the effects of non-uniform distribution of current density on pore morphologies, the pore diameter and porosity over the surfaces have been statistically estimated from SEM images taken from five different locations of the micropillar's surfaces (Fig. 3a-3f), as shown in Fig. 4. The values of pore diameter and porosity for 30-min-etched surface decrease gradually from the top region to bottom, with the maximum differences of around 23 and 15%, respectively. The surfaces etched for 10 and 50 min also show the similar trend. The variation tendency of pore diameter and porosity are in good consistence with the simulated distribution of current density (Fig. 2c-2e). According to previous studies[34,35], pore morphology and porosity are highly related to the applied current density. The spatial variation of the pore diameter and porosity shown in this study is attributed to the variation of the current density over the micropillared surfaces, where the 3D micropillar structures disturb and distort the electric filed non-uniformly. While the maximized and highly concentrated current density is present around the sharp edge of the top corner, the formation of nanopores is still effective at the edge area (Fig. 3b). Although the current density reaches the maximum at the top pillar edge, it is still below the critical current density (J_{ps}), above which electrochemical polishing will occur.[36] Meanwhile, we have also conducted the electrochemical etching on micropillar arrays with the aspect ratio of 5, which is twice the aspect ratio shown in Fig. 3. It also shows that electropolishing occurs at the upper corner of the micropillar (Fig. S5). According to the simulation results, the maximum current density around the upper corner has a positive correlation with the micropillar's aspect ratio. It also

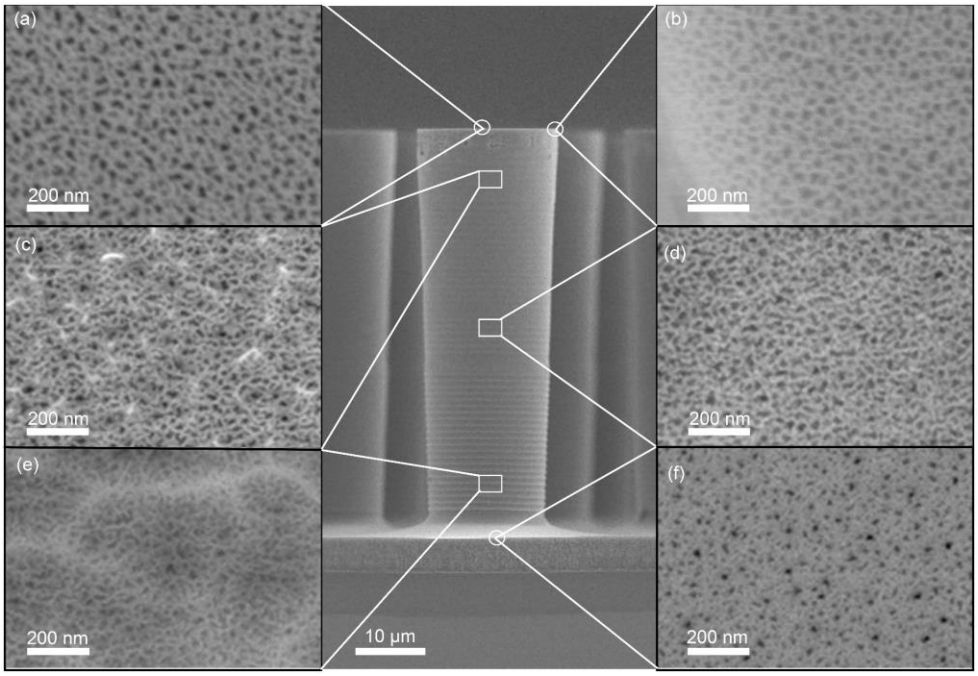

Fig. 3 Scanning electron microscope (SEM) images of the porous micropillar arrays etched for 30 min. (a) Top-view of pore distribution in the centre of top surface; (b) Top-view of pore distribution on the top edge. (c-e) Side-view of the pore distribution on the upper (45 μm from the bottom), middle (25 μm from the bottom), and lower location (5 μm from the bottom) along the sidewall, respectively. (f) Top-view of pore distribution on the bottom surface.

suggests that the current density flowing through the top corner is high enough to lead to the electropolishing. Moreover, the pore diameter and porosity tend to increase slightly with the increase in the etching time. It is attributed to the further polishing effect on the pore walls with the prolonger etching time.

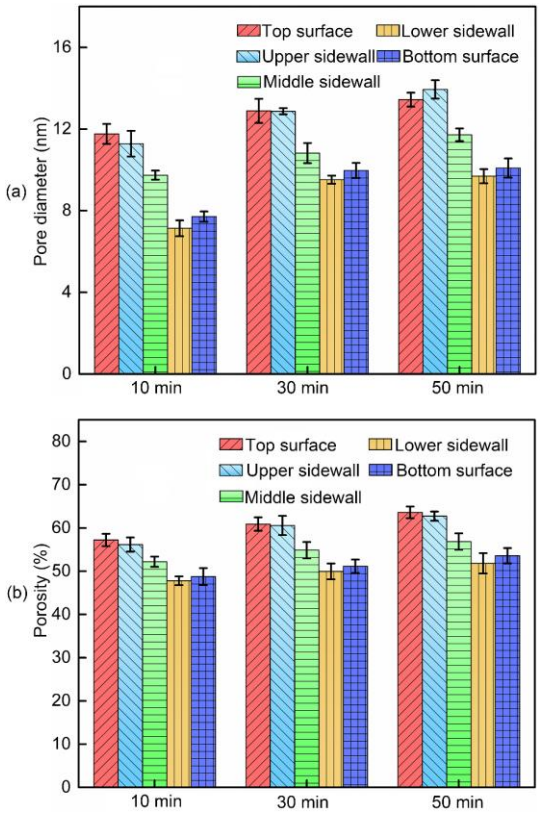

Fig. 4 Spatial variation of (a) the pore diameter and (b) porosity along the surfaces for different etching times.

Morphological details inside the circular micropillar

In order to investigate the propagation of pores inside the microstructure, the micropillar was broken to expose its cross-section plane. Fig. 5 shows the SEM images of the exposed surfaces at ~5 μm above the bottom surface. In 10 min of electrochemical etching (Fig. 5a), only a thin (~1.2 μm) layer around the micropillar was converted to be porous. The close-up view of the porous layer (Fig. 5b) reveals that the pores grow radially in lateral direction, agreeing well with the direction of the electric current flow predicted by the finite element analysis. However, when the electrochemical etching time increased to 30 min (Fig. 5c), it is found that the pores grow mainly along the <100> direction rather than along the radial direction. The 3D microstructures make the silicon surface exposed to the applied electric field with different crystal orientations. The electrochemical etching for crystalline silicon is preferred on the <100> crystal orientation than all other crystal orientations. Due to the anisotropy, the thickness of the porous layer is not uniform around the micropillar but shows the variation depending on the <100> and <110> crystal orientations, i.e. 4.6 μm and 5.3 μm, respectively. It is unique that the 3D geometry of the micropillar makes the silicon surface have multiple crystal orientations exposed to the electrolyte, as opposed to only one crystal orientation for the case of a two-dimensional (2D) planar surface, resulting in the anisotropic nature of the porous structures around the silicon micropillar. According to the {100} stereographic projection for silicon wafer, a continuously curved sidewall of the micropillar should expose an infinite number of crystal planes that are classified as (x, y, 0). As the etching proceeds on the circular

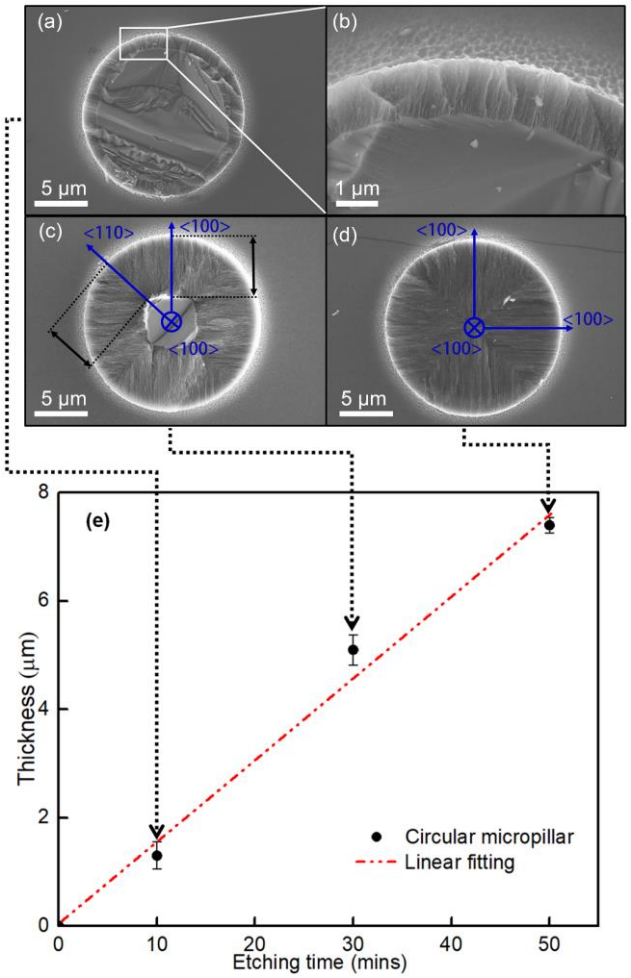

Fig. 5 SEM images of the pore distribution inside the micropillar after different electrochemical etching times: (a) 10 min; (b) close-up view; (c) 30 min; (d) 50 min. The exposed surfaces are at the height of ~5 μm. The blue arrows in (c) and (d) indicate the crystal orientations of the crystalline silicon substrate. (e) Change in the thickness of the nanoporous layer with respect to the etching time. The dashed line is the result of linear fitting.

micropillar, the pores propagate preferentially along the <100> direction. Therefore, it would be reasonable to assume that the pore will also propagate preferentially along the <100> direction on micropillars with curved sidewalls. As the electrochemical etching time lasted further up to 50 min (Fig. 5d), the whole micropillar was converted to be porous, showing the more dramatic effect of the anisotropy in the formation of pore structures around the silicon micropillar. Fig. 5e shows the change of the thickness of a nanoporous layer with respect to the etching time. It is observed that the measured thickness increases linearly over the etching time, with an etching rate of about 0.15 μm/min. In addition to the etching time, the thickness of a porous layer increases with the applied current density.[37,38] The result shows that the thickness of the porous layer can be well controlled by the regulation of the etching time under the constant current density. In the case of the top and bottom surfaces exposing only (100) planes, the direction of the pores does not change but keeps the perpendicular direction to the surfaces, regardless of the etching time, while the thickness of the porous layer increases with the etching time (see Fig. S6 in Supplementary Information).

Effect of exposed crystal planes on growth of nanopores

To study the influence of different exposed crystal planes on the growth of nanopore within microstructures more systematically, we further performed electrochemical etching on substrates patterned with square micropillar arrays and microgroove arrays, using identical etching recipes to the circular micropillar arrays. Fig. 6 reveals the morphology and distribution of nanopores inside the microstructures achieved at different etching times. For the square micropillar depicted in Fig. 6a, the four sides are equivalent (110) planes leading the nanopores to grow perpendicularly to them with same etching rate. According to previous studies, pores always proceed in <100>-equivalent crystallographic directions independently of the exposed orientation.[39,40] One possible explanation is that, in this case, the direction of current flow plays a more dominant role in determining the direction of pore growth than the crystallographic direction. In Fig. 6b, the exposed sides of the square micropillar are equivalent (100) planes. In this case, the etching results show that the pores still grow perpendicularly to the sidewall. Comparison of the two groups represented in Fig.6a and 6b indicates that the pores grow perpendicularly to the sides of the square micropillar regardless of the exposed plane. However, the pore depth is greater in the case of (100) planes than that of (110) planes (Fig. S7), implying the etching rate is faster along the <100> crystal orientation than the <110> crystal orientation. Similar to the circular micropillar, with the increase in the etching time, the middle solid part of the square micropillar is depleted gradually. When the etching time is long enough, the pores self-limit on two intersecting diagonal planes, dividing the entire square micropillar into four fully porous areas. It should be noted that the etching thickness on the square micropillar over etching time also exhibits a roughly linear relationship (Fig. S7). The pore depth on a square micropillar is greater than that on a circular micropillar with the same etching time. It is attributed to the fact that the current density through the surface of the square micropillar is greater than that through the surface of the circular micropillar, which occurs as a result of the differences in the micropillar's geometry.

Fig. 6c shows the cross-section of the etched microgroove structure. The top surface and sidewalls are (100) and (110) planes, respectively. While pores grow in both <100> and <110> directions, the porous layer is thicker on the top surface with a (100) plane than that on sidewalls with (110) planes. This discrepancy in the etch rate is consistent with the results shown in micropillar structures (Figs. 6a and 6b). It should also be noted that the etch rate is higher in the lower part of the sidewall than in the upper part. When the etching time reached 50 min, only the lower part of the sidewall of the microgroove was converted into sponge-like porous silicon, whereas the non-porous solid silicon is still retained inside the upper part of the sidewall. Although the etching time extended longer, the solid silicon section in the middle was not converted to porous silicon. It indicates the termination of the electrochemical

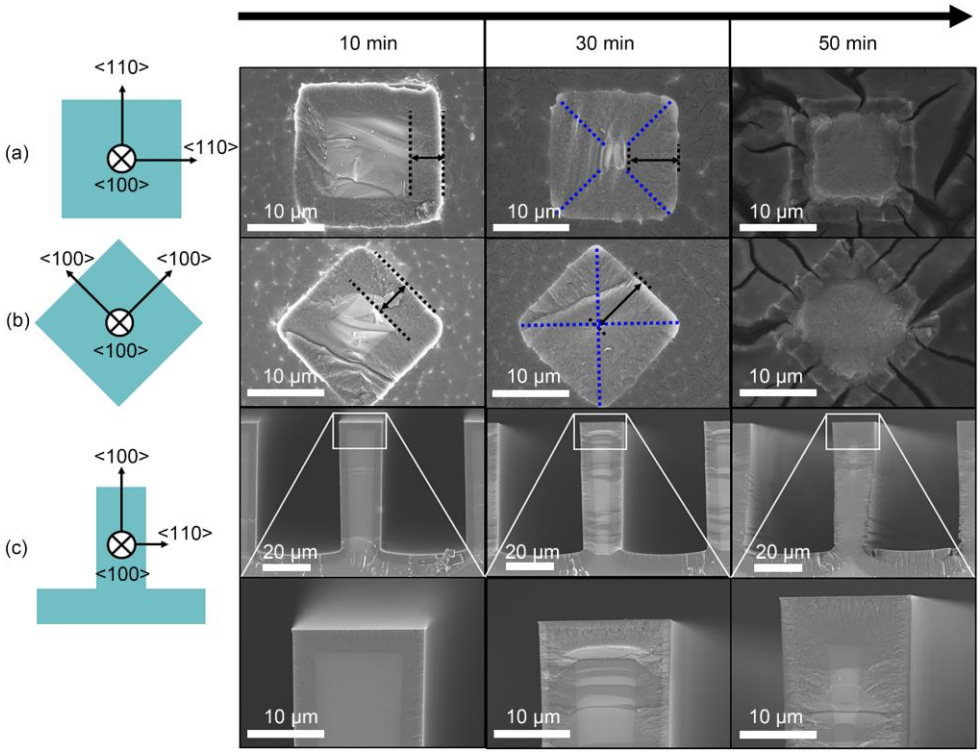

Fig. 6 SEM images of square micropillar and microgroove after the electrochemical etching for different etching times. (a) Square micropillar exposing (110) crystal planes. (b) Square micropillar exposing (100) crystal planes. (c) Microgroove exposing both (100) and (110) crystal planes. The blue dashed lines in Fig. 6a and 6b indicate the projection line of two intersecting diagonal planes.

etching. When the bottom solid silicon is fully transformed into porous silicon, the current path to the upper part is cut so that there is no current flowing to the upper part to sustain the electrochemical etching. It ceases the growth of pores in the upper part of the microgroove structure, leaving the solid silicon in the middle. The result indicates that the complete transformation of solid silicon to sponge-like porous silicon can be limited by the geometry of the microstructure and the crystalline plane of the exposed surface (i.e., etch rate).

Although pores can be formed with the silicon wafer with different crystal orientations such as (110) and (111) wafers, the morphology of the nanopores would be different from that shown on (100) wafers. Several previous works already reported that the directions in which pores grow should not be always the same with the direction of the current flow and not be always perpendicular to the surface.[39-42] As for the {100}, {110} and {111} stereographic projection for silicon (see Fig. S8), micropillars with the same shape on different oriented silicon wafers would expose different crystal planes. For example, square micropillar on (100) wafer would expose four (110)-equivalent planes. However, for (110) wafer, it would expose two (110) planes and two (100) planes. For (111) wafer, it would expose two (110) planes and two (112) planes. The previous works showed that titled pores could be formed on non-orthogonal surfaces and the pores would always prefer to proceed along <100> direction. Although pores would no longer proceed perpendicularly to the exposed planes in such different orientations, the sponge-structured porous silicon can still be realized with the silicon with different crystal orientations.

Conclusions

In this study, we have demonstrated the fabrication of hierarchical porous microstructures by employment of the facile electrochemical etching process to the microstructured silicon surface. The diameters of etched nanopores vary from 8 to 15 nm, which falls in the pore size regime of mesopores. Finite element analysis simulation results show that the current is redistributed by the microstructure and flowed perpendicularly through the surfaces. The pore morphology involving porosity and pore diameter shows close correlation with the distribution of current density. Due to the distinct crystalline orientations of crystalline silicon material, highly ordered and aligned pore structures perpendicular to the exposed surfaces are achieved on the surfaces of 3D microstructures. The fraction of the porous layer with respect to the solid silicon can be conveniently regulated by the etching time. It allows the transformation of solid silicon into sponge-like porous silicon. Depending on the geometry of the microstructure and the crystalline plane of the exposed surface (i.e., etch rate), the conversion of the solid silicon into porous silicon can be self-limited, which can allow the design and fabrication of novel hierarchical porous structures. Given the facile and unique characteristics of the fabrication process, it can be potentially employed for many applications such as long-acting drug delivery, anodes of the electrochemical batteries, micro-optics and wick structure in the phase-change heat transfer applications, where the porous nature of substrate material can greatly benefit the performances.

Experimental section

Preparation of micropillar arrays

The silicon micropillar arrays were fabricated on a highly doped (resistivity of 0.01 Ω•cm) p-type <100>-oriented silicon wafer by using photolithography and DRIE. Before the photolithography process, the wafer was first coated with a thin layer of HMDS (Hexamethyldisilazane) to promote the adhesion of the photoresist to the wafer. The wafer was then spin-coated with a photoresist layer (AZ 6130, Microchemicals) of ~3 µm thick (3000 rpm for 30 s), and soft-baked on a hot plate at 90°C for 150 s. Next, the photoresist was exposed to UV (ultra-violet) light using mask aligner (MA6, Karl Suss, Germany) for 6 s. Then, the photoresist was developed by immersing the wafer in a developing solution (RZX-3038, SUZHOU RUIHONG CO., Ltd.) at room temperature for 6 s. The developed wafer was then hard-baked at 110°C for 2.5 min. The micropatterned photoresist was used as a mask for DRIE. An inductively coupled plasma (ICP) etching (Surface Technologies Systems USA Inc., Redwood, CA) was used for the DRIE process to form the micropillar arrays of silicon. After the DRIE process, the wafer was cleaned in acetone and then isopropanol with ultrasonic to remove the residual polymer. The cleaned wafer was then soaked in piranha solution (H_2SO_4: H_2O_2; 7:3 in volume) for 20 min for further cleaning. The finally obtained arrays of micropillar had a diameter of ~20 µm, depth of ~50 µm and pitch of ~50 µm.

Formation of nanoscale pores around the microstructures

The porous silicon layer was formed on the surface of the microstructures by anodic oxidation in hydrogen fluoride (HF) solution. Before the electrochemical etching process, gallium/indium (Ga/In) eutectic was uniformly applied on the backside of the wafer to ensure homogeneous current distribution during the etching process. A platinum plate was served as the cathode. The sample served as the anode and was oxidized under anodic bias between the two electrodes. For the etching parameters, a constant current density of 10 mA/cm^2 was used. The concentration of the electrolyte was 10wt. % HF in deionized (DI) water. A few drops (~2.5 ml) of wetting agent (Kodak Photo-Flo) was added into the electrolyte. The addition of wetting agent into the electrolyte can prevent the accumulation of hydrogen bubbles on the silicon-electrolyte interface. After the etching procedure, the samples were soaked in ethanol and deionized water for 10 min in each solution. Then the samples were dried by nitrogen gas.

Measurement of surface morphology

Field-emission scanning electron microscopy (SU 8010, Hitachi) was used to observe the surface morphology of the samples. The measurement of pore diameters and porosity was estimated by processing the SEM images in the ImageJ software.

Conflicts of interest

There are no conflicts to declare.

Acknowledgements

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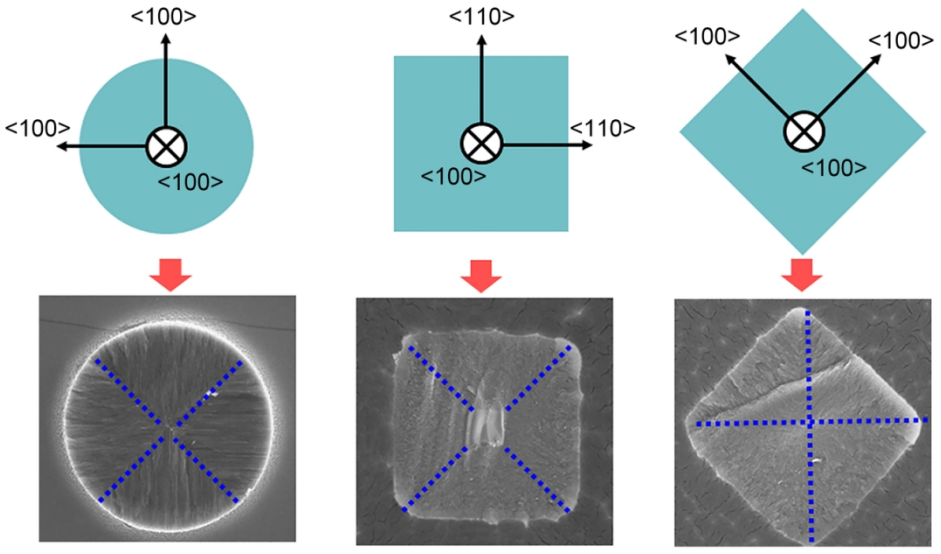

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