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ARTICLE

No hysteresis TIPS-pentacene:polystyrene Blend-based Organic Field Effect Transistor by Extruded Direct Ink Writing and the Application in Resistive Load Inverter Circuit

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Organic field effect transistors (OFETs), with the active layer made from 6,13-bis (triisopropylsilylethinyl) pentacene:polystyrene blend films, were fabricated on rigid (glass) and flexible (polyethylene terephthalate) substrates using motor-controlled extrusion-based Direct Ink Writing printing method. The characteristics of OFETs fabricated at different in-situ annealing temperatures (25, 40, 55, 70 and 85 ℃) were explored. We find that the OFET with 25 ℃ in-situ annealing temperature exhibits better performance with improved carrier mobility of 0.14 $cm^2 V^{-1} s^{-1}$, I_{ON}/I_{OFF} ratio of 2.7×10^3, threshold voltage of 0.14 V, and minimal hysteresis compared to other annealing temperature schemes. Moreover, bending tests were performed on flexible devices using three different bending radii (1/2.54, 0.75/1.91 and 0.5/1.27 inch/cm) which were swept continuously. Results indicate that the ON current monotonically decreases as the bending radius is reduced. In addition, a resistive load inverter circuit, formed by connecting an OFET to an external resistive load, can achieve a gain of 2.6 at a V_{DD} of -80 V and R_L of 100 MΩ. Furthermore, long-term stability of the inverter was investigated over a one-month period. Our analysis shows that there are minimal differences in both the switching threshold voltage and gain, with their one-month variances of 0.77 and 3.13, respectively.

Introduction

As low-cost, low-temperature, large-area, and easy-to-process electronic devices, organic field effect transistors (OFETs) have gained tremendous research interest.[1, 2] OFETs are necessary components in multiple electronic devices, including memory devices, complementary circuits, sensors, and flat-panel displays.[3-7] Compared to organic semiconductors (OSCs) made with traditional vacuum or photolithography methods,[8, 9] the solution-processed OSCs are promising due to their lower fabrication costs, larger area, and higher feasibility for customization. Strong π-π interactions of the solution-processed OSCs not only dewet the film from the substrate but also induce non-uniform morphologies, resulting in low crystallinity and poor electrical performance of the devices.[10, 11] Due to the ability of the blend to phase separate into a layered structure which conserves the continuity, crystallinity and the molecular packing of the small molecule OSC,[12] the OSCs blend with insulating polymers has often been used in OFETs. As a result, the blend can yield film-forming properties, increase device stability and uniformity as well as maintain device mobility.[13-16]

Over the past few decades, various solution-based fabrication methods for OSCs, such as spin-coating, dip-coating, drop-casting, edge casting, zone casting, spray-coating, screen printing, inkjet printing, and roll-to-roll printing, have been investigated.[17-22] While spin coating, which allows for high film uniformity and is controlled by rotation speed and time, can be considered the most commonly used method at the laboratory level, printing technology-based approaches require more attention when considering large-scale industrial production[1]. When it comes to distinguished printing methods in the industry, inkjet printing is the most commonly used because its droplet volume can reach the femtoliter range to reduce the destructive effect of solvents and significantly improve the printing resolution. However, inkjet printing can only print low-viscosity materials and limit the utility of printable materials.[23] Furthermore, the so-called coffee ring effect appears when the suspension's concentration is low, resulting in the non-uniform distribution of particles.[24-27] As an alternative method, the Direct Ink Writing (DIW), due to its low energetic extrusion, can produce a smooth printing surface.[28] In addition, the DIW is considered a simple, adaptable, and low-cost method that is applicable in ambient conditions with moisture and oxygen.[29, 30] Besides supporting a broad range of depositable feedstock materials, such as polymers, alloys and ceramic materials, DIW is also less likely to clog the printing nozzles compared with inkjet printing.[31, 32] These advantages of DIW can facilitate the large-scale production of organic electronics through the automation of industrial process.[33-35] There are different types of DIW methods, such as the ultrasonically-, pneumatically-,[36] electrohydrodynamically-,[37] and extrusion-based. Compared with other different types of DIW printers, the extrusion-based DIW is easier to use since the driving force is directly provided by a stepping motor, which can also substantially reduce the cost of the printer.

In this work, we report on fabricating solution-processed bottom-gate/top-contact OFETs with motor-controlled extrusion-based DIW printed semiconductor layer, which is believe is the first such demonstration. Based on the blend solution of an organic semiconductor, 6,13-bis (triisopropylsilylethinyl) pentacene:polystyrene (TIPS-pentacene:PS), we printed p-type

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OFETs using extrusion-based DIW method at different in-situ annealing temperatures (25, 40, 55, 70 and 85 °C). A comparison study with drop casted devices was conducted. We found that the organic semiconductor deposited by extrusion-based DIW at 25 °C displayed the best performance with maximum mobility of 0.14 $cm^2 V^{-1} s^{-1}$, I_{ON}/I_{OFF} ratio of 2.7×10^3, threshold voltage of 0.14 V, and minimal hysteresis. The X-ray diffraction (XRD) spectra and polarized optical microscopic images of the TIPS-pentacene:PS films revealed the changes of crystallinity and thermal cracks at different in-situ annealing temperatures. Static characteristics and long-term stability of resistive load inverters obtained by connecting an OFET to an external resistive load, are reported. Simulation of the resistive load inverters is provided to validate our experimental data. In addition, bending test was conducted of an OFET under three different bending radii (1, 0.75 and 0.5 inch). The pre-bent and post-bent characteristics of the OFET are analysed in this study.

Experimental

Since small organic molecule - TIPS-pentacene is a high-performance p-type organic semiconductor with good environmental stability, high solubility in most common organic solvents and high field effect mobility higher than 1.00 $cm^2 V^{-1} s^{-1}$,[10, 38-40] it was selected as the organic semiconductor used in our bottom-gate/top-contact OFET devices.PS was selected as the insulating polymer since there is no polar groups.

Chemicals

TIPS-pentacene, PS, acetone, isopropyl alcohol (IPA), and toluene, were all purchased from Sigma Aldrich (St. Louis, MO, USA) and used without any further purification. Parylene dix-SR was given from Specialty Coating systems Inc. The TIPS-pentacene:PS ink was obtained from a 40 mg/mL TIPS-pentacene solution in toluene mixed with a 10 mg/mL of PS solution in toluene, with the volume ratio of 1:1.

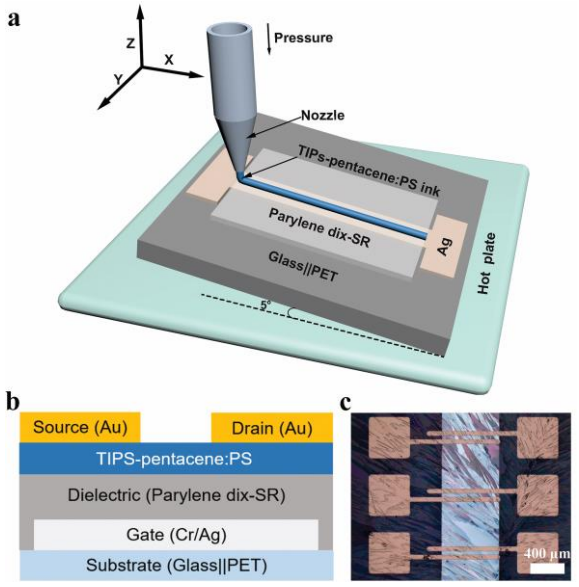

Fig. 1 The schematic of the (a) extrusion-based DIW printing; (b) OFET; (c) physical OFET.

Device Fabrication

In the first step, 25 mm × 25 mm glass or PET slides were cleaned in an ultrasonic bath with deionized (DI) water for 10 minutes, followed by acetone and IPA for 10 minutes, respectively. The device with PET (polyethylene terephthalate) substrate was prepared (same way with glass substrate) for the mechanical bending test. In the second step, a bilayer gate of chromium (Cr) and silver (Ag) was deposited on the substrate by thermal evaporation (Integrated Physical Vapor Deposition and Glovebox, Lesker Nano 36) through a shadow mask with a thickness of 5 nm and 100 nm, respectively. In the third step, Parylene dix-SR film, acting as the dielectric layer, was deposited by a chemical vapor deposition (CVD) method (Parylene Chemical Vapor Deposition, SCS Labcoater 3) to a thickness of 850 nm. In the fourth step, TIPS-pentacene:PS blend ink was extruded from a 0.16 mm inner diameter needle by DIW (Hyrel 3D) on a tilted (~5°) substrate with a printing speed of 200 mm/min,[41] with five different in-situ annealing temperatures (25, 40, 55, 70 and 85 °C), followed by covering with a Petri Dish to slow down solvent evaporation (sometimes referred to as solvent annealing[42]) to up to 6 hours. As shown in Fig.S1 (ESI†), the mean static contact angle is 6.7° between toluene and Parylene dix-SR, indicating the excellent surface wettability of Parylene dix-SR. In the last step, gold (Au), which acts as the source and drain electrodes, was deposited by thermal evaporation through a shadow mask with a thickness of 50 nm. Channel length and width are 100 μm and 700 μm, respectively. Fig. 1a displays the schematic of extrusion-based DIW printing method, Fig. 1b and c display the schematic and physical picture of the OFET. Fig.S2 (ESI†) displays the transfer curves of different tilted substrates and different printing speed. We can find that the optimal printing speed is 200 mm/min with a tilted (~5°) substrate.

Characterization

All electrical performance was measured by a semiconductor parameter analyzer (HP 4155A). The XRD spectra was measured by

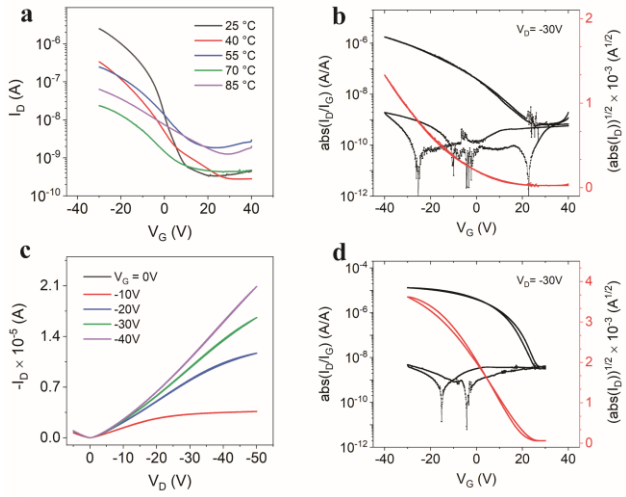

Fig. 2 (a) The transfer curves of OFETs at different in-situ annealing temperatures (25, 40, 55, 70 and 85 °C); (b) transfer and leakage current curves of OFET at 25 °C in-situ annealing treatment; (c) output curves with different V_G with extrusion-based DIW printed TIPS-pentacene:PS film; (d) transfer and leakage current curves of OFET with drop casted TIPS-pentacene:PS film.

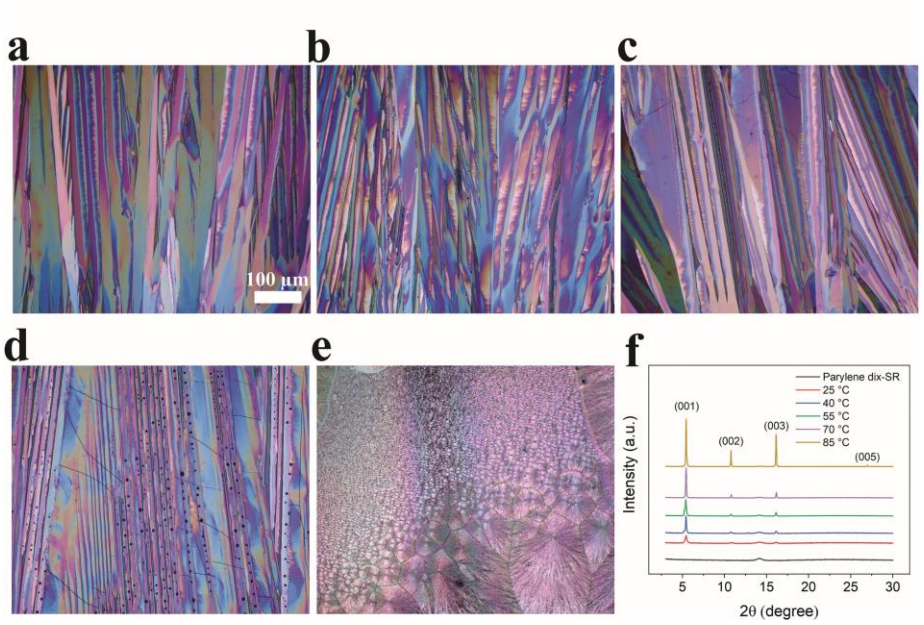

Fig. 3 Polarized (75 degrees) optical microscope images of TIPS-pentacene: PS blend films with different in-situ annealing temperatures (a) 25 ℃; (b) 40 ℃; (c) 55 ℃; (d) 70 ℃; (e) 85 ℃; (f) XRD spectra obtained from different annealing temperatures.

Panalytical Empyrean Powder X-ray Diffractometer. The polarized optical microscopic images were obtained by optical microscope (Zeiss axioscope 5). The static contact angle was measured by an automated goniometer (ramé-hart, 290-F1).

Results and discussion

Fig. 2a shows a family of transfer curves with different in-situ annealing temperatures by the DIW method, with V_D= -30 V. It can be seen that the ON current decreases as temperature increases from 25 ℃ to 70 ℃. Although a slight increase can be seen when the temperature reaches 85 ℃, it is still lower than 25 ℃. Fig. 2b shows the transfer and leakage current of the OFET whose semiconductor layer was deposited by extrusion-based DIW at 25 ℃. The leakage current is as low as 2 nA, which implies that the dielectric layer is insulating properly. The I_{ON}/I_{OFF} ratio of the OFET is 2.7 × 10^3, the charge carrier mobility is 0.14 cm^{-2} V^{-1} s^{-1} and the threshold voltage is 1.46 V. Moreover, the device exhibits almost no hysteresis, indicating negligible charge trapping in the dielectric layer and TIPS-pentacene/dielectric interface. Fig. 2c shows the output curves with different V_D by DIW printed TIPS-pentacene:PS film, with Fig. 2d showing the transfer and leakage current curves of devices fabricated with drop casted OSC. It can be seen that the OFET with drop casted TIPS-pentacene:PS film has the mobility of 1.00 cm^{-2} V^{-1} s^{-1}, threshold voltage of 21.86 V, and I_{ON}/I_{OFF} ratio of 3.3 × 10^3. Compared to drop casted TIPS-pentacene:PS blend OSC in this work and spun-cast, as well as the blade-coated and inkjet printed devices from other groups, as shown in Table S1,[10, 43-47] the OFET with the extrusion-based DIW printed TIPS-pentacene:PS blend demonstrates threshold voltage of 1.46V, which is much better than the other techniques. In addition, there is negligible hysteresis, indicating very low charge trap density at the phase separated interface.[48] While, the devices with other techniques either only showed a single scan or had poor hysteresis. These can be explained by extrusion-based DIW method as it can continuously draw out the ink, leading to the increased continuous crystals in the channel.[36, 37] These observations suggest that extrusion-based DIW is more effective in the deposition of organic semiconductors. In addition, Fig.S3 (ESI†) also shows the transfer characteristics of OFET with TIPS-pentacene:PS blend film and neat TIPS-pentacene. Compared to TIPS-pentacene:PS blend film, the OFET with neat TIPS-pentacene exhibits inferior characteristics, namely higher threshold voltage of 12.71 V, and poor hysteresis, and I_{ON}/I_{OFF} ratio of 10.04. This can be explained by noticing that the TIPS-pentacene:PS blend solution process can induce a vertical phase separation,[13-16, 49] resulting in formation of semiconductor-top and insulator-bottom bilayer structure/double-layer dielectric. In this case the bottom-gate/top-contact device, the top segregated TIPS-pentacene and PS rich layer

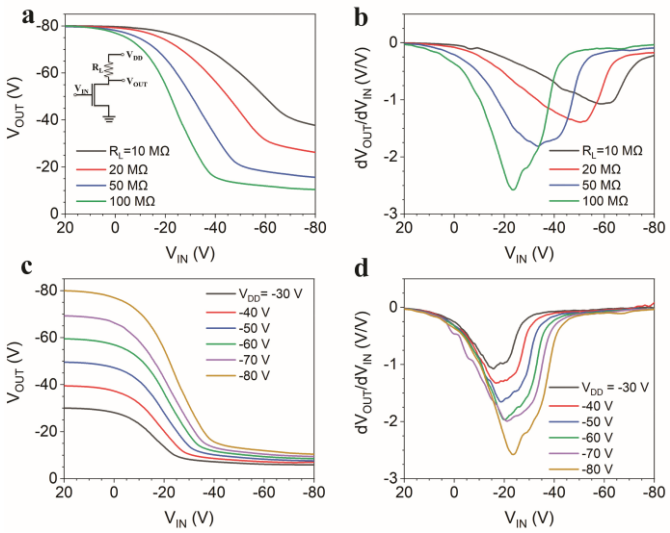

Fig. 4 Voltage transfer characteristics of the inverter circuit with (a) varying resistive loads with V_{DD} = -80V, the schematic of the resistive load inverter circuit (inset) (c) varying V_{DD} with R_L= 100 MΩ;(b) The static gains were obtained with (c) varying loads (d) varying V_{DD}.

acts as the dielectric-semiconductor interface, which is further confirmed by a lower capacitance density of TIPS-pentacene:PS blend devices compared with neat TIPS-pentacene devices, leading to higher charge carrier mobilities.[50, 51] At this dielectric-semiconductor interface, the electrical performance improvement can be explained by reduced dipolar disorder and carrier localization at the interface due to a less polar, low-k polymeric dielectric (PS is 2.6), reducing the broadening of density of states and eventually the trap state density.[50, 52-56]

In order to explore the effect of in-situ annealing temperature on TIPS-pentacene crystals, polarized (75 degrees) optical microscope images were obtained. Fig. 3 shows the TIPS-pentacene:PS blend films printed at different in-situ annealing temperatures, from 25 ℃ to 85 ℃. It can be observed that the thermal cracks start to appear when the temperature reaches 55 ℃, as displayed in Fig. 3c. When the temperature reaches 70 ℃, the thermal cracks are more pronounced. The thermal cracks will grow with the growth process of TIPS-pentacene crystal, which severely restricts the charge transport. Thus, the ON current will decrease as the temperature increases. Interestingly, ribbon-shaped crystals start to disappear at 85 ℃ since the solvent evaporates significantly quicker after printing compared with other temperatures (the boiling point of toluene is 110.6 ℃). Fig. 3f shows the XRD spectra with different annealing temperatures, indicating the (00*l*) peak intensities becoming stronger as the temperature increases, indicating higher crystallinity. However, compared with the crystallinity and a relatively large device channel length of 100 um, thermal cracks have a dominant impact on the charge transport in these device (channel length is 100 μm)‡. Therefore, the device with 25 ℃ in-situ annealing temperature exhibits the best electrical performance. Fig.S4 (ESI†) shows the polarized (75 degrees) optical microscope images of the TIPS-pentacene:PS blend film at 25 ℃ in-situ annealing temperature, which are ribbon-shaped "flakes" over several hundred micrometers long and around 40 micrometers wide. In addition, the vertical phase separation of the TIPS-pentacene:PS blends contribute to the high degree of orientation. During the film formation phase separation of the PS and the small molecular material occurs, leading to formation of a continuous highly crystalline TIPS-pentacene molecules with the π-π stacked molecular layers oriented parallel to the film surface.[12, 13, 16, 46, 57] The uniform ribbon-shaped crystals were likely the result of a tilted substrate and the phase separation which are beneficial to the transport of the charges.[58] Furthermore, the surface is covered by the crystals and the color variation was caused by the variation of the TIPS-pentacene crystal orientation.[59]

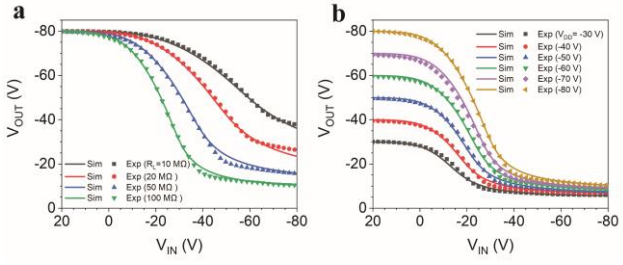

Fig. 5 Comparison of the simulated and experimentally characterized voltage transfer characteristics with (a) varying resistive loads and with (b) varying voltage loads.

For the purpose of testing the utility of our devices as circuit components in the electronic application, the resistive load inverter circuit was investigated. The OFET was connected to an external resistive load (R_L) with different values arranged from 10, 20, 50 to 100 MΩ. Fig. 4a shows the voltage transfer characteristics of the OFET inverter circuit with varying resistive loads, with fixed V_{DD} = -70 V. It can be found that a high output voltage, V_{OUT} = -70V or ON state is obtained when the input voltage is low, and a low output voltage, V_{OUT} = -9.8V, or OFF state is observed when the input voltage is high. The responding switching threshold voltages (V_m) where V_{IN} equal to V_{OUT} with 10, 20, 50, and 100 MΩ resistances are -53.8 V, -48.2 V, -40.4 V, and -35.4V, respectively, which shows that the inverting characteristics of the resistive load inverter is enhanced as the resistive load increases. Fig. 4b shows that the voltage gains (dV_{OUT}/dV_{IN}) extracted from Fig. 4a are 0.9, 1.3, 1.7, and 2.1, respectively, indicating that the gain is improved as the load resistance increases. The inverter with 100 MΩ resistive load shows the best switching characteristics compared with 10, 20, and 50 MΩ. This can be explained by the significantly high voltage drop across the inverter with 100 MΩ resistive load which thus shows the best inverter operation. Fig. 4c presents the voltage transfer characteristics of the OFET inverter circuit with varying supply voltages and a fixed resistive load (R_L= 100 MΩ). It can be found that the inverting performance is enhanced when the supply voltage V_{DD} increases. As shown in Fig. 4d, the gain of the inverter is improved when V_{DD} increases, with the gain of 1.1, 1.3, 1.7, 2.0, 2.1, and 2.6 when V_{DD} is equal to -30V, -40V, -50V, -60V, -70V and -80V, respectively.

Simulation of OFETs is of great importance for the design verification and fault detection of manufactured large-scale analog circuits. Compared to transistors made from regular crystallized inorganic semiconductors (e.g., Si, Ge, etc.), the modelling of polymerized OFETs remains in an extensive research stage due to the presence of multiple trap states between the conduction and valence bands of polymerized semiconductors.[60, 61] To achieve reliable simulation of organic inverting circuits, we employ a generalized solid-state model in conjunction with a fitted equation for subthreshold currents to describe the full-regime transconductance and output characteristics of the OFETs.[62, 63] The compact OFET

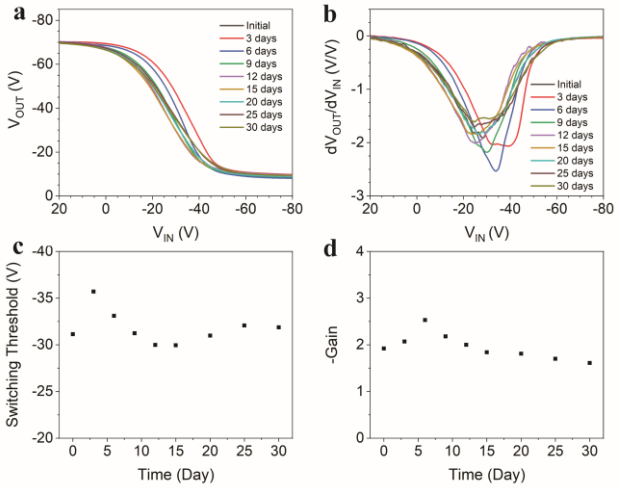

Fig. 6 The voltage transfer characteristics of the resistive load inverter circuit with R_L=100 MΩ, V_{DD} = -70V in one month; (b) static gains were obtained from (a); (c) the switching thresholds and (d) gains in one month.

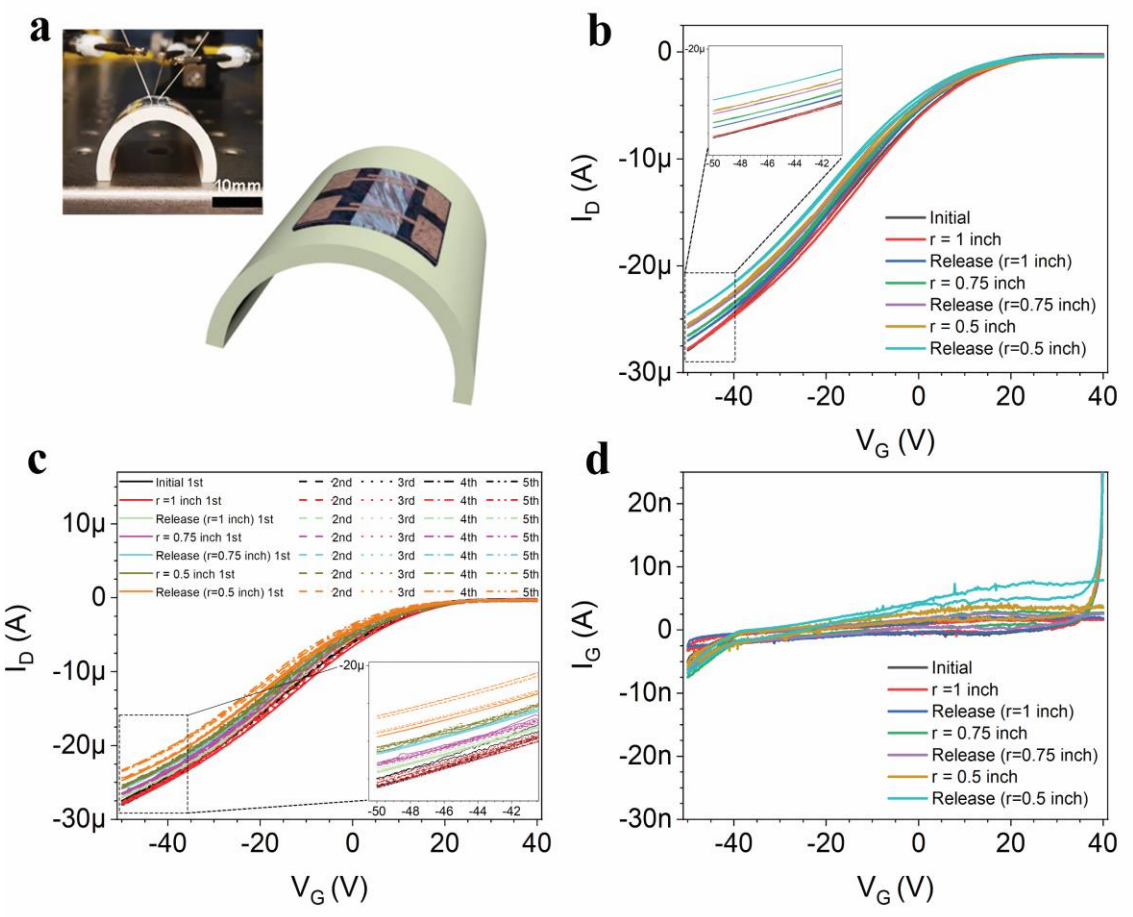

Fig. 7 (a) An OFET during the bending test; (b) the average transfer curves of the device with 1-, 0.75- and 0.5-inch bending radius at V_D = -30V; (c) all the five separate transfer curves of each state; (d) average leakage currents with 1, 0.75- and 0.5-inch bending radius at V_D = -30V.

model is then utilized as the basic circuit module to form the integrated circuit model of our organic load resistive inverters. Fig.5a and b presents the comparison of the simulated (lines) and the experimentally characterized voltage transfer curves (symbols) of a load resistive inverter operating at different resistive and voltage loads, respectively. It can be found in Fig.5 that the simulated transfer curves are in good agreement with the experimental data. These findings not only demonstrate the accuracy of the circuit model we used for organic load resistive inverters, but also verify the correctness of the design, fabrication and characterization procedures performed in this study.

The long-term stability performance of the resistive load inverter was also evaluated. Fig.6 shows the long-term stability of the inverter circuit with R_L=100 MΩ and V_{DD} = -70V. The voltage transfer characteristics of the inverter circuit were measured every three days in the first 15 days after fabrication, and every five days for the remaining 15 days. It can be observed from Fig.6a that there are slight changes in the transfer curves during one month period, and also in the gains as shown in Fig.6b. Fig.6c and Fig.6d display the variation of switching threshold voltage and gains of the inverter in one month, with small variances of 0.77 and 3.13 (defined as the square root of the variance), respectively. In Fig.6a, we can also find that the curve monotonically shifted towards smaller V_{IN} during the first 15 days, and then remained largely unchanged. This observation indicates good stability of the OFETs, while the slight changes can be explained by the accumulation of water absorption into TIPS-pentacene or at the interfaces.

To explore the effects of mechanical strain and stress, the flexible OFET was bent to 1, 0.75- and 0.5-inch bending radius continuously. The OFET undergoes the initial state, followed by a slight tensile bending strain state with a bending radius of 1 inch and a recovery state, then a lighter tensile bending strain state with a bending radius of 0.75 inch and the corresponding recovery state, and finally a tensile bending strain state with a bending radius of 0.5 inch and its recovery state. Fig.7a displays OFET during the bending test. An average transfer curve was obtained for each state with a total of five separate measurements. Fig.7b shows the typical average transfer characteristics of the device in each process as the bending strain decreases gradually. Fig.7c displays five separate transfer curves of each states. It can be observed that the ON current monotonically decreases as the bending radius decreases from 1 inch to 0.75 inch and then 0.5 inch, this can be attributed to microcracks of TIPS-pentacene crystals during the bending. The microcracks in the channel raise the density of trap states in the bandgap of OSCs, leading to reduced mobility of charge carriers.[64] Moreover, the current decrease between “initial state” followed by “release state” is always smaller than “bending state” followed by “release state”. More specifically, compared to the decrease of currents between “Initial” and “r = 1 inch”, between “Release (r = 1 inch)” and “r = 0.75 inch”, and between “Release (r = 0.75 inch)” and “r = 0.5 inch”, the

decrease of currents between "r = 1 inch" and "Release (r = 1 inch)", between "r = 0.75 inch" and "Release (r = 0.75 inch)" , and between "r = 0.5 inch" and "Release (r = 0.5 inch)" are more significant. This can be explained by the formation of additional microcracks in TIPS-pentacene and more TIPS-pentacene delamination from Parylene dielectric can be caused during the release process than the bending process. The average leakage current curves with different bending states are shown in Fig.7d. It can be observed that the leakage current stays below 8 nA, although there is a slight increase after the mechanical strain. This indicates that the good insulating performance of the dielectric layer is preserved after the strain.

Conclusion

In this study, motor-controlled extrusion-based DIW method was applied for the first time to deposit organic semiconductor of TIPS-pentacene:PS blend for fabrication of OFETs. Our study shows that the carrier mobility is 0.14 $cm^2 V^{-1} s^{-1}$, I_{ON}/I_{OFF} ratio is 2.7×10^3, the threshold voltage is 0.14 V, with minimal hysteresis. Compared to the OFET with drop casted TIPS-pentacene, the threshold voltage and hysteresis are both enhanced. In addition, a resistive load inverter circuit, formed by connecting an OFET to an external resistive load, can achieve a gain of 2.6 at a V_{DD} of -80 V and R_L of 100 MΩ. Furthermore, the long-term stability of the inverter shows good performance with small variances of 0.77 and 3.13 of switching threshold voltage and gain over a one-month period. The devices also show good mechanical stability evaluated at three different bending radii. OFETs with DIW printed organic semiconductor show good electrical performance, and long-term and mechanical stability, indicating it is promising in circuit application. In the future, the fully printed OFET by extrusion-based DIW will be developed.

Author Contributions

H.B. performed the experiments and analysis and prepared the manuscript; Y.Y. performed the simulation part and contributed to preparation of the manuscript; R.M.V. and R.A.N supervised this work and contributed to writing of the manuscript. R.M.V. provided funding for this work.

Conflicts of interest

There are no conflicts to declare.

Acknowledgments

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Notes and references

‡ Relatively large crystals would likely favour devices with smaller channel lengths, that would be unaffected by formation of thermally induced cracks. However, our long-term goal is the fabrication of entire devices, including electrodes, using DIW, placing a restriction of minimal feature size. Hence our goal of 100 μm channel lengths.

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