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ARTICLE

Post-annealing optimization of the heteroepitaxial La-doped $SrSnO_3$ integrated on silicon via ALD†

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Wide band gap (WBG) alkaline-earth stannate transparent oxide semiconductors (TOSs) have attracted increasing attention in recent years for their high carrier mobility and outstanding optoelectronic properties, which have been applied to wide applications such as flat-panel displays. However, most alkaline-earth stannate are grown by molecular beam epitaxy (MBE), there are some intractable issues about tin source including the volatility with SnO and Sn sources and the decomposition of SnO_2 source. In contrast, atomic layer deposition (ALD) serves as an ideal technique for the growth of complex stannate perovskite with the precise stoichiometry control and the tunable thickness at the atomic scale. Herein, we report the La-$SrSnO_3/BaTiO_3$ perovskite heterostructure heterogeneously integrated on Si (001), which uses ALD grown La-doped $SrSnO_3$ (LSSO) as a channel material and MBE grown $BaTiO_3$ (BTO) as a dielectric material. The reflective high-energy electron diffraction and X-ray diffraction results indicate the crystallinity of each epitaxy layer with a full-width-at-half-maximum (FWHM) of 0.62°. *In-situ* X-ray photoelectron spectroscopy results confirm that there was no Sn^0 state in ALD deposited LSSO. Besides, we report a strategy for the post-treatment of LSSO/BTO perovskite heterostructures by controlling the oxygen annealing temperature and time, with a maximum oxide capacitance C_{ox} = 0.31 μF/cm^2 and a minimum low-frequency dispersion for the devices with 7 h oxygen annealing at 400 °C. The enhancement of capacitance properties is primarily attributed to a decrease of oxygen vacancies in the films and interface defects in the heterostructure interfaces during an additional *ex-situ* excess oxygen annealing. This work expands current optimization methods for reducing defects in epitaxial LSSO/BTO perovskite heterostructures and shows that excess oxygen annealing is a powerful tool for enhancing the capacitance properties of LSSO/BTO heterostructures.

1. Introduction

Wide band gap (WBG) transparent oxide semiconductors (TOSs) have been extensively investigated as the conductive channel of thin-film transistors (TFTs) for flat-panel displays, organic light-emitting diodes (OLEDs), and touch-responsive screens.[1–3] In particular for the most commonly used TOSs, the derivatives of In_2O_3, such as indium tin oxide (ITO),[4] indium gallium zinc oxide (IGZO),[5] and indium tin zinc oxide (ITZO),[6] have been widely studied.[7] As the indium element is a scarce earth resource, In_2O_3-based TOSs are not cost-effective and sustainable, and the toxicity of indium makes In_2O_3-based TOSs not environment-friendly and harmless.[8,9] As alternatives alkaline-earth stannate TOSs [$ASnO_3$ (A = Ca, Sr, Ba)],[10–12] have attracted much attention recently with superior performance in near-infrared region (NIR) transparency and mobility compared with In_2O_3-based TOSs at room temperature (RT).[13,14]

To further enhance the conductivity and enlarge the band gap tuning range, numerous studies introduced lanthanides, especially lanthanum (La), into $BaSnO_3$ (BSO) and $SrSnO_3$ (SSO) single-crystal films as A-site dopants.[15–21] In 2012, Kim *et al.* demonstrated that bulk La-doped BSO single-crystal mobility[22] could reach up to 320 cm^2/Vs compared to 120–180 cm^2/Vs of La-doped BSO single-crystal thin films at RT.[23–25] The high mobility enables the integration of BSO or La-doped BSO as the conductive channel with various high-κ perovskites, such as $SrTiO_3$ (STO),[26] $BaHfO_3$,[27] $LaInO_3$,[28] $BaTiO_3$ (BTO),[29] as the gate dielectric. By utilizing only the perovskite oxides, the BSO-based heterojunctions perform superior to conventional semiconductor material systems such as Si and AlGaN/GaN in the high-frequency power field.[29,30] Additionally, STO and BTO perovskites can be grown epitaxially on Si (001)[31,32] and can be compatible with Si-based CMOS technology, providing an expanded route to design next-generation devices for perovskite heterojunctions integrated on Si.[33,34] However, the defects at the interface caused by the perovskite lattice mismatch may restrict the device's performance. With strain defined as $((a_{sub} - a_{film})/a_{film})$, the lattice constant of 4.116 Å[35] for BSO leads to −5.1% and −2.5% strain on STO (3.905 Å)[36] and BTO (4.012 Å)[37,38], respectively, at RT. In the La-doped BSO

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system, the mismatch would further expand since the lattice constant of La-doped BSO increases with La concentration.[18,22] In comparison with BSO, SSO is more suitable for heterostructure growth due to better lattice matching. The SSO perovskite is an orthorhombic structure (*Pbnm* space group) with a pseudo-cubic unit cell parameter of 4.038 Å,[39,40] which leads to −3.3% and −0.6% strain on STO and BTO at RT, respectively. Thus, SSO is more promising to mitigate strain-related interface defects than BSO in heterostructures, especially with BTO. In addition, the larger band gap of SSO than BSO (4.10–4.46 eV *vs.* 2.93–4.05 eV, experimental values)[18,41–45] gives SSO a better NIR/visible-light transparency and higher breakdown voltage.[13,46]

For high film quality, previous studies on SSO were mostly achieved by molecular beam epitaxy (MBE).[46–48] However, for stannate perovskite growth, MBE has shown volatility issues with SnO and Sn sources, and difficulty for the SnO_2 source to achieve stable film stoichiometry.[40] Furthermore, the elevated thermal budget of MBE is incompatible with CMOS back-end-of-line (BEOL) processes, constraining the use of alkaline-earth stannate TOSs. The advantages in atomically smooth surface, accurate stoichiometry control, adjustable thickness at the atomic scale and the ability to achieve conformal deposition on 3D structure make atomic layer deposition (ALD) particularly appealing for researchers.[49] Therefore, instead of MBE, ALD is an ideal technique for the growth of complex stannate La-doped $SrSnO_3$ (LSSO), especially.

In this work, we report crystalline LSSO epitaxial growth on BTO by ALD. As the perovskite heterostructure, LSSO is selected as the conductive channel, and BTO is selected as a dielectric. To integrate crystalline LSSO/BTO on Si, a thin crystalline STO buffer layer is deposited by *in-situ* MBE to reduce the lattice mismatch between BTO and Si and prevent SiO_2 formation during the following growth.[34,50,51] We use MBE to grow BTO on STO buffered-Si for better crystallinity than ALD in this work, which could reduce the impact of defects induced in BTO layer so we could focus the study of defects in ALD-deposited LSSO. For the LSSO/BTO system, oxygen vacancies in the films and defects at the interfaces could degrade the mobility of LSSO and make BTO barrier leaky. Hence, we also introduce the additional *ex-situ* post-annealing in excess oxygen to systematical study the impact of post-annealing on LSSO/BTO heterostructures via frequency-dependent transport measurements of capacitance *vs.* voltage.

2. Experimental

N-type Si (001) (As-doped, R_s = 0.001–0.005 ohm·cm, MTI Corporation) was used as the substrate for film growth. Film depositions and X-ray photoelectron spectroscopy (XPS) analyses took place in an ultra-high vacuum system (UHV) comprised of a DCA 600 MBE chamber, a custom-built ALD reactor, and an analysis chamber with XPS capability. Samples could be transferred between chambers through a UHV transfer line maintained at 1×10^{-9} Torr.[52]

A stack of films, 19 nm LSSO/20 nm BTO/2 nm STO buffer layer, was deposited on Si (001). STO-buffered Si preparation is described in detail previously, which allows epitaxial integration of the following oxides.[31,53,54] Subsequently, the BTO growth was performed by MBE at 750 °C by shuttering the Ba and Ti effusion cells. The oxygen pressure was maintained at ~5×10^{-6} Torr, and Ba and Ti rates were controlled to be 3.73 Å/ML and 1.13 Å/ML, respectively. The BTO film was crystalline as-deposited and was cooled down to 200 °C in the same oxygen environment after the desired film thickness was reached. Afterward, the sample was transferred *in-situ* to the ALD chamber for LSSO deposition. The ALD LSSO growth was conducted at 180 °C under 1 Torr with ultrahigh purity argon as carrier and purge gas. Strontium bis(triisopropylcyclopentadienyl) (at 130 °C),

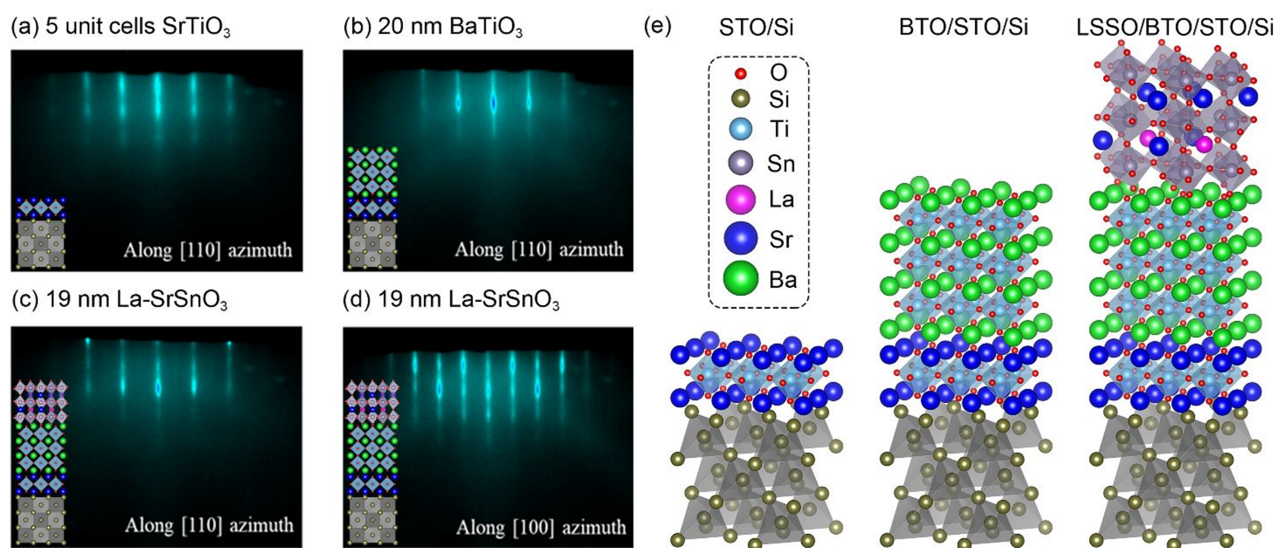

Fig. 1 RHEED images of (a) 5 unit cells of $SrTiO_3$ buffer layer, (b) 20 nm $BaTiO_3$ film, (c) and (d) 19 nm La-$SrSnO_3$ film on LSSO/BTO/STO-buffered Si. Images (a), (b), and (c) were taken along [110] azimuth, while image (d) was taken along [100] azimuth. The inserted figures of (a), (b), (c), and (d) are the schematic of heterostructure fabrication. (e) Schematics of the crystal structures of STO-buffered Si, BTO/STO-buffered Si, and LSSO/BTO/STO-buffered Si.

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tetrakis(dimethylamino) tin (at 40 °C), and tris(N,N′-diisopropylformamidinato) lanthanum (at 110 °C) were used as the precursors for Sr, Sn, and La, respectively; deionized water (at RT) was used as the co-reactant. Among these three precursors, tetrakis(dimethylamino) tin shows a narrower ALD temperature window. A detailed ALD growth process of SnO_2 has been studied in our previous work.[40] According to the growth rate of SnO_2 films at various temperatures, a narrow ALD plateau has been found in the range of 170–180 °C. Moreover, the dose time of precursors have been carefully optimized for ALD process, which consequently confirmed no CVD behavior during the LSSO ALD process. More details about ALD stannate growth can be found in our previous work.[40] In addition, to obtain good crystallinity of LSSO film, the thickness of LSSO was selected as 19 nm in this work. Nonetheless, thinner LSSO film could be realized absolutely by ALD due to its self-limiting or self-saturating reaction. The La doping in SSO film can be controlled by adjusting ALD cycle ratios. In this work, the La dopant was 0.8%. The ALD LSSO film was amorphous as-deposited, and *in-situ* post annealing for 10 min at 750 °C in oxygen (P = 1 × 10^{-5} Torr) was performed to crystallize the film.

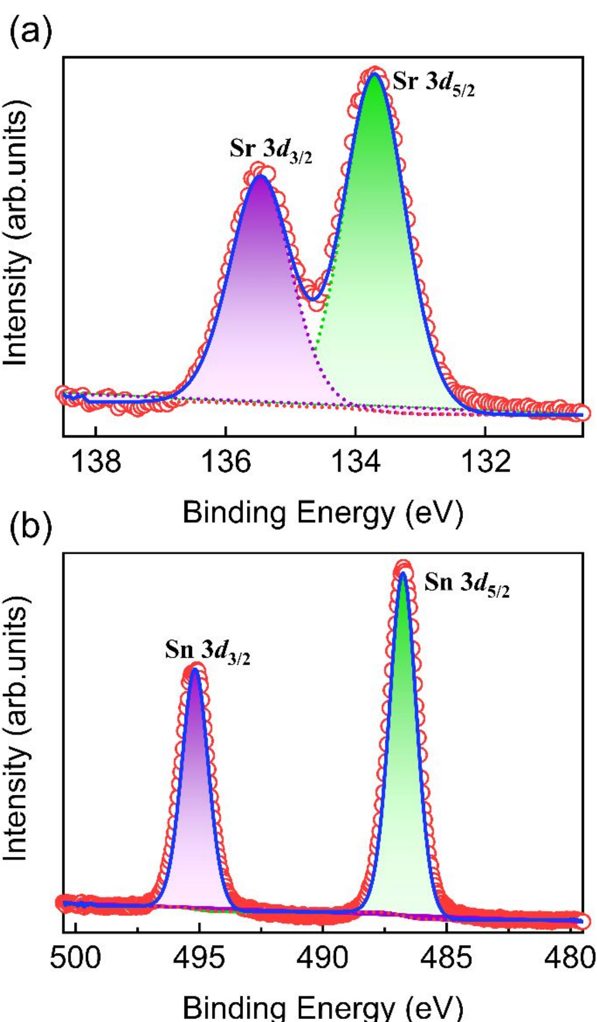

Fig. 2 X-ray photoelectron spectra for Sr 3*d* (a) and Sn 3*d* (b) in the 19 nm LSSO/20 nm BTO/2 nm STO-buffered Si stack after *in-situ* post-annealing at 750 °C in oxygen (P = 1 × 10^{-5} Torr).

In-situ reflective high-energy electron diffraction (RHEED) and XPS were conducted to monitor the film surface order and analyze the film composition, respectively. The XPS system uses a monochromatic Al Kα source with a photon energy of 1486.6 eV and a VG Scienta R3000 analyzer. For *ex-situ* analyses, the film thickness was obtained by fitting X-ray reflectivity (XRR) data using GenX,[55] X-ray diffraction (XRD) and asymmetrical reciprocal space mapping (RSM) were used to obtain unit cell parameters of films. XRR, XRD, and RSM measurements were conducted by using a Rigaku Ultima IV diffractometer with a thin film attachment and a Cu Kα X-ray source.

Prior to electrical measurements, completely crystallographic LSSO/BTO heterostructures samples were subjected to additional *ex-situ* various annealing conditions in a furnace flowing with oxygen (P = 150 Torr) to decrease defects in the films and interfaces. Then, a Ti/Pt circle electrode was deposited by the electron beam evaporation through a shadow mask with a diameter of 280 μm. Finally, the frequency-dependent transport measurement was evaluated using an Agilent B1500A semiconductor parameter analyzer from 1 kHz to 100 kHz.

3. Results and discussion

3.1 Characterization of Crystalline LSSO/BTO/STO-Buffered Si

Fig. 1 shows the RHEED image of each layer in LSSO/BTO/STO-buffered Si. The streaky RHEED pattern indicates the crystalline surface order of the film. The 5 unit cells of the crystalline STO buffer layer (Fig. 1a) is established on Si (001) as template to integrate the LSSO/BTO stack. A 20-nm-thick crystalline BTO, as demonstrated in Fig. 1b, was deposited at 750 °C by MBE on STO-buffered Si, followed by a 19-nm-thick ALD-grown LSSO film crystallized at 700 °C. Fig. 1c and 1d illustrate the crystalline LSSO film, with La:Sr:Sn = 0.8:47.7:51.5, along [110] and [100] azimuth, respectively. The rocking curve analysis of the overall film stack at 44.5° 2θ for LSSO (002)/BTO (002) reflection shows a full-width-at-half-maximum (FWHM) of 0.62° (ESI Fig. S1†), which also indicates the good crystallinity of each layer. The crystal structures of STO-buffered Si, BTO/STO-buffered Si, and LSSO/BTO/STO-buffered Si are shown in Fig. 1e.

The composition of films and the chemical states of the elements in oxide films were identified by *in-situ* XPS. XPS results do not show visible carbon or nitrogen signals in LSSO films, demonstrating that the ALD growth process does not introduce carbon or nitrogen dopants into the films. Sr 3*d* and Sn 3*d* spectra are shown in Fig. 2a and 2b, respectively. The fine spectra peaks of Sr $3d_{5/2}$ and Sr $3d_{3/2}$ are situated at 133.7 and 135.4 eV, respectively, as demonstrated in Fig. 2a. The Sn $3d_{5/2}$ and Sn $3d_{3/2}$ peaks are found at the binding energy of 486.8 and 495.2 eV with a peak separation of 8.4 eV (Fig. 2b), which is consistent with the value reported previously.[56] Typically, Sn^0 formation is a thorny issue in the SSO growth process. According to Fig. 2b, no obvious Sn^0 state (485.0 eV)[56] is found in the LSSO XPS result, which confirms that the in-situ post-annealing in O_2 pressure of 1 × 10^{-5} Torr is effective in preventing Sn^0 formation

in the stannate.[40] In addition, due to the low La doping concentration (0.8%), no obvious La signal was detected by XPS. Out-of-plane XRD was employed to obtain the unit cell parameters of films. In Fig. 3a, the film peaks of LSSO (001)/BTO (001) and LSSO (002)/BTO (002) indicate that both LSSO and BTO films are single crystalline. The 2-nm-thick STO buffer layer is too thin to have strong enough intensity, and the signal could be buried under LSSO/BTO signal due to their close peak positions. To differentiate the peak position of LSSO and BTO, a slow 2θ–ω XRD with a scan rate of 1°/min was conducted in the range of 40°–50° 2θ, as the insert shown in Fig. 3a. The peak positions of LSSO (002) and BTO (002) are 44.53° 2θ and 44.87° 2θ, as shown by the arrows in Fig. 3a, leading to the out-of-plane lattice constants are 4.066 Å and 4.037 Å, respectively. The XRD result is also in good agreement with the RSM result. As illustrated in Fig. 3b, LSSO (103) and BTO (103) are observed, Q_y is used to calculate the in-plane unit cell parameter (a), and Q_z is used to calculate the out-of-plane unit cell parameter (c). The measured unit cell parameters are a = 4.069 Å and c = 4.066 Å for LSSO film and a = 4.022 Å and c = 4.042 Å for BTO film. Based on the unit cell parameters, both LSSO and BTO films are

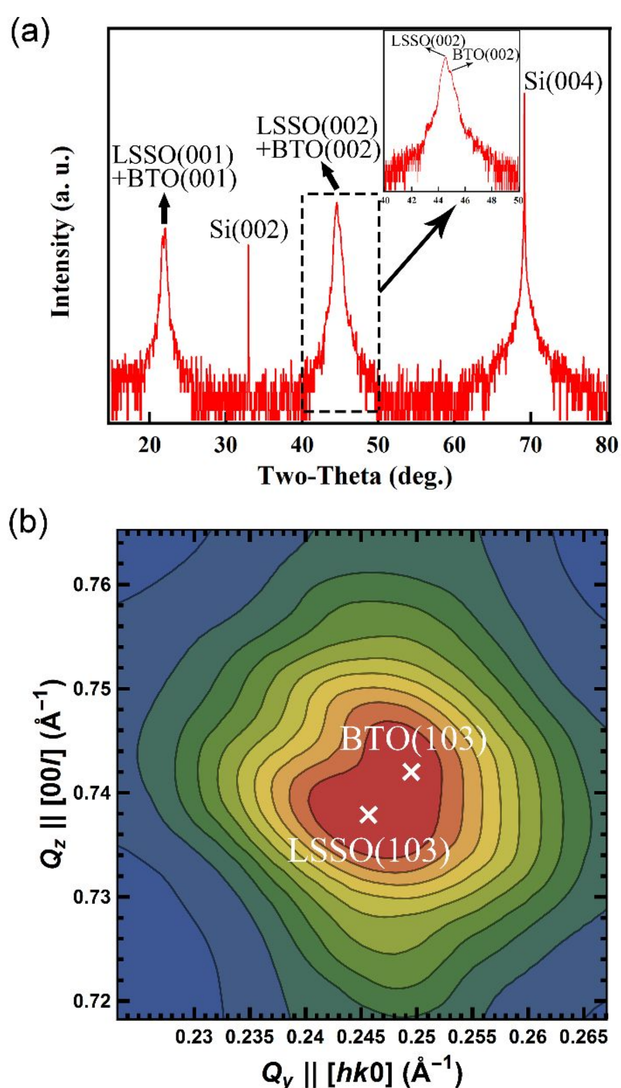

Fig. 3 (a) Out-of-plane XRD of a 19 nm LSSO/20 nm BTO/2 nm STO-buffered Si stack scanned by 4°/min. The inserted figure is the small-range (40°–50° 2θ) XRD scanned by 1°/min. (b) RSM of a 19 nm LSSO/20 nm BTO/2 nm STO-buffered Si sample.

relaxed, which could result from the high-temperature crystallization annealing process in O_2 (750 °C) and thick film thickness. The LSSO lattice constant is slightly larger than the reported ALD SSO lattice constant (a_{pc} = 4.050 Å)[40] due to the incorporation of La dopant.[18,22]

3.2 Electrical measurement part

The LSSO/BTO heterostructure devices made from LSSO/BTO/STO-buffered Si stack samples were annealed at various temperatures under 150 Torr of flowing O_2. Fig. 4 shows the schematic structure of LSSO/BTO heterostructure devices and the frequency-dependent transport measurement system. The *ex-situ* annealing parameters of LSSO/BTO heterostructure stack samples are listed in Table 1. Device A was not subjected to annealing. For Devices B–F, the annealing temperature ranged from 400 °C to 600 °C, and the annealing time ranged from 3 h to 7 h.

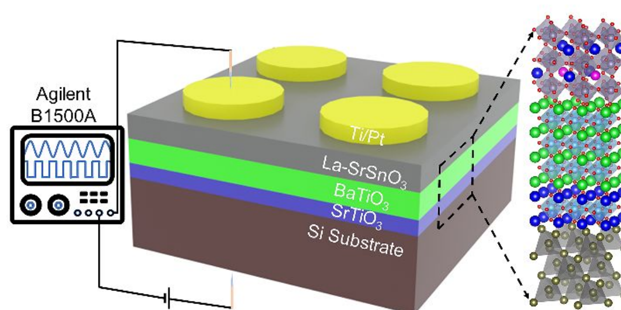

Fig. 4 Schematic structure of LSSO/BTO heterostructure devices characterized by Agilent B1500A semiconductor parameter analyzer. The dotted black square corresponds to the crystal structures of LSSO/BTO/STO-buffered Si samples.

Frequency-dependent transport measurements of capacitance (C) *vs.* voltage (V) were carried out for Devices A–F at RT. There are no prominent C–V characteristics in device A, which was not subjected to *ex-situ* annealing (ESI Fig. S2†). For Device A, even though an *in-situ* post-annealing step (10 min at 750 °C, oxygen partial pressure $P = 1 \times 10^{-5}$ Torr) was conducted to complete its crystallization, there was still a significant density of defects in the heterostructures leading to no prominent C–V characteristics. Thus, longer annealing times at a higher O_2 pressure are necessary to decrease the oxygen vacancies and interface defects for LSSO/BTO heterostructures.

Table 1 *Ex-situ* annealing parameters of LSSO/BTO heterostructure samples A–F.

Sample	Annealing temperature (°C)	Annealing time (h)
A	N/A	N/A
B	400	3
C	400	5
D	400	7
E	500	5
F	600	5

Compared to Device A, Device B shows better C–V characteristics (ESI Fig. S3†), but the tremendous amount of

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noise and some abnormal trends still demonstrate the high defects density of films and interfaces. Fig. 5a and 5b show the *C*–*V* characteristics for devices C and D at frequencies from 1 kHz to 100 kHz. The capacitance is normalized by dividing the minimum. Strong frequency dispersion is observed in the depletion regime ($V < 0$ V) for Devices C and D. As the interface traps will contribute to the intensity of the frequency dispersion effect because these defects only respond to lower-frequency AC signals instead of high-frequency AC signals,[57] the interface trap capacitance generated from capture/release electrons by the interface traps is negligibly small at high-frequency.[58,59] Hence, there should be a minor frequency dispersion phenomenon for perfect heterostructure interfaces in low-frequency scans, which means the dispersion intensity in low-frequency range could reflect the density of interface defects. A stronger low-frequency dispersion phenomenon appears in Device C compared to Device D, which reflects more interface defects in Device C. The significant decrease of interface defects in Device D is due to the excess oxygen passivating the interface defects during the longer annealing time at 400 °C. Moreover, the accumulation regime ($V > 0$ V) also shows a frequency dispersion effect in Devices C and D, as shown in Fig. 5a and 5b. The frequency dispersion in the accumulation regime may be related to border traps,[60] which refer to traps in the dielectric close to the interface.[57,59] Based on the previous report,[61] the charges exchange will happen between border traps in a dielectric with mobile carriers in the semiconductor bands through tunneling.[59,61] The response of border traps dominates in the accumulation region at low frequencies;[59] thus, the dispersion degree analysis for *C*–*V* of Devices C and D was conducted in the range from 1 kHz to 10 kHz. As shown in Fig. 5c, the capacitance of Device C degrades from 100% to 65% with the frequency increased from 1 kHz to 10 kHz, but the capacitance of Device D shows weak dependence on the frequency in the low-frequency range. This behavior further confirms the presence of more border traps in Device C than in Device D, which shows that a longer annealing time at 400 °C could reduce more border traps in the LSSO/BTO heterostructure. Besides, the worse *C*–*V* result of Device B further confirms this conclusion. Hall measurement for Device D after 7 h annealing at 400 °C reveals that the 19 nm heteroepitaxial LSSO film on BTO has an effective carrier concentration of $n = 5.55 \times 10^{19}$ cm^{-3} and mobility of $\mu = 8.44$ cm^2/Vs.

Nonetheless, as differs from Devices C and D, the *C*–*V* result of Devices E and F shows no saturation in the accumulation regime, and even no prominent phenomenon of the low-frequency dispersion (ESI Fig. S4 and S5†). Compared with *C*–*V* curves of Devices B, C, and D, there is a right shift of the *C*–*V* curves of Devices E and F annealed at high temperature (> 500 °C). It is noted that the applied voltage was controlled below 4 V because the increasing gate leakage would phase into considerable while $V > 4$ V. Long-time annealing above 500 °C vanished most oxygen vacancies but created fixed negative charges at the heterostructure interface. Thus, the interface defects dominated by fixed negative charges are responsible for the absence of saturation plateaus in accumulation for Devices E and F.[62] In particular, Device E with 500 °C annealing shows a slight saturation tendency but not for Device F with 600 °C annealing, which also confirms that higher temperature annealing creates more fixed negative charges. Further investigation should be directed to clarify the physical origins of fixed negative charges in LSSO/BTO heterostructures that appear to be caused by long-time annealing above 500 °C. In

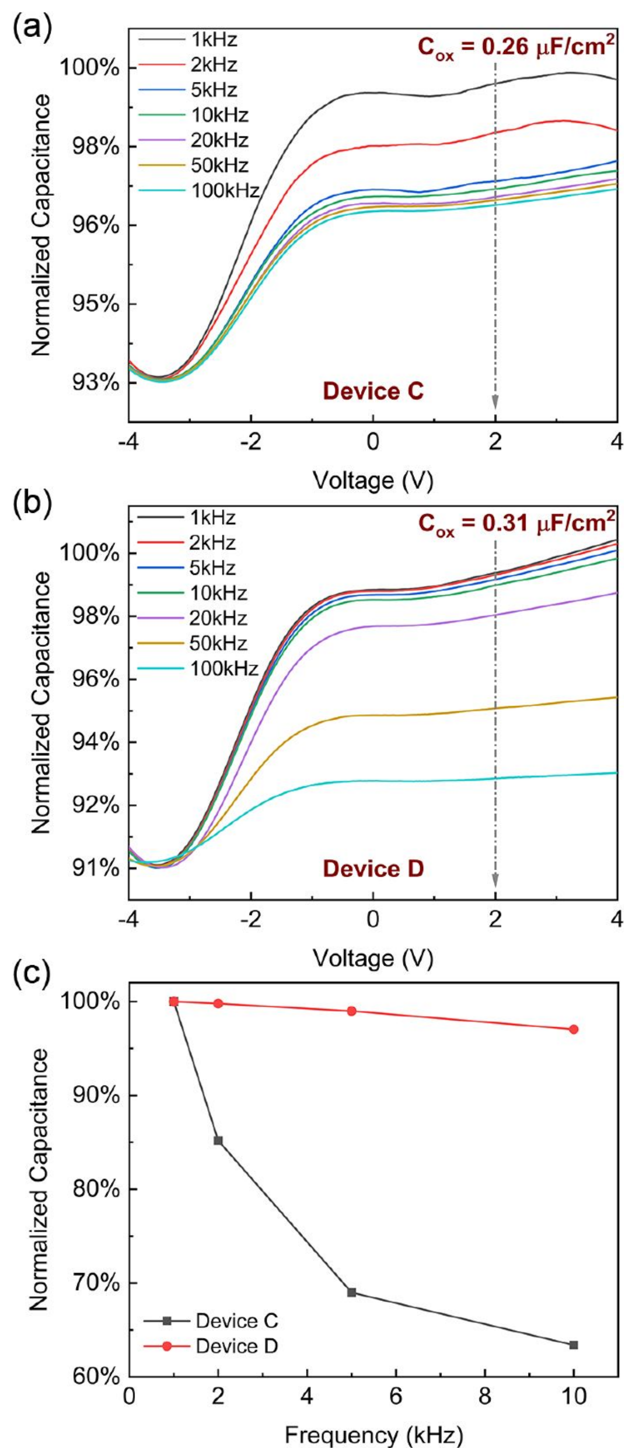

Fig. 5 (a) and (b) are capacitance–voltage (*C*–*V*) characteristics of Devices C and D with frequencies from 1 kHz to 100 kHz. The capacitance is normalized by dividing the minimum. (c) The dispersion degree analysis for *C*–*V* of Devices C and D in low-frequency range with $V = 2$ V.

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conclusion, the absence of saturation plateaus in the accumulation regime for Devices E and F demonstrates that long-time annealing above 500 °C might be overloaded for the post-treatment of LSSO/BTO heterostructures.

Generally, the oxide capacitance (C_{ox}) approached the maximum capacitance (C_{max}) in accumulation, where the measured capacitance saturates with the low-frequency *C–V* scan in typical Si/SiO_2-based MOS. Fig. 6 shows the summary of C_{ox} with the 1 kHz *C–V* scan for Devices B, C, and D, annealing with 3 h, 5 h, and 7 h at 400 °C, respectively. According to the data, C_{ox} = 0.14 μF/cm², 0.26 μF/cm², and 0.31 μF/cm² are exported from the *C–V* measurements for Devices B, C, and D, respectively. As for Devices E and F, the C_{ox} cannot be extracted due to the absence of saturation in *C–V* results. With the increase of annealing time at 400 °C, C_{ox} increases from 0.14 μF/cm² to 0.31 μF/cm² due to fewer oxygen vacancies and interface defects in the LSSO/BTO heterostructure. This indicates that the decrease of oxygen vacancies and interface defects was carried out slowly during long-time *ex-situ* annealing at the applicable temperature. The leakage current density is lower than 10^{-5} A/cm² at 1 kHz in the whole range of V = −4 V~4 V, which is below the low power limit of 1.5 × 10^{-2} A/cm² with the applied field of 2.5 MV cm^{-1} and meets the MOSFETs gate limit requirement (10 A/cm²) [63] (ESI Fig. S6† is the leakage current density–voltage (*J–V*) characteristics of device D). The leakage of LSSO/BTO heterostructure could bear comparison with the congeneric ABO_3 perovskite high-κ dielectrics in similar conditions, such as $SrTiO_3$ (10^{-4} A/cm² with the applied voltage of 7.5 V),[63] $Ba_xSr_{1-x}TiO_3$ (10^{-1} A/cm² with 1 V),[64] $LaAlO_3$ (10^{-6} A/cm² with 4 V)[65] and $SrHfO_3$ (10^{-3} A/cm² with 1.5 V).[66]

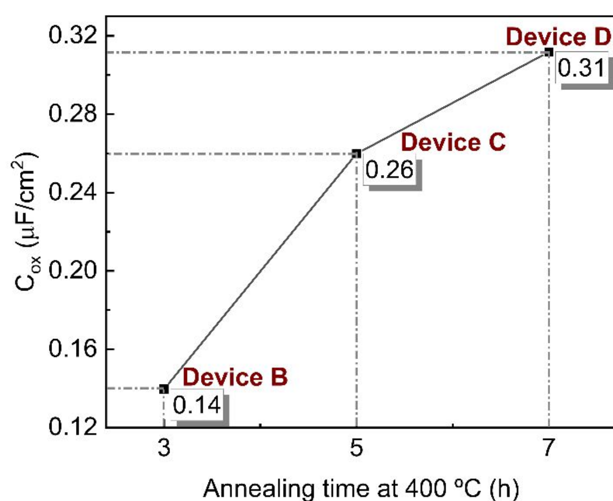

Fig. 6 Summary of oxides capacitance C_{ox} in the accumulation regime with 1 kHz *C–V* scan for Devices B, C, and D. The capacitance is normalized by the area of the top circle electrode with a diameter of 280 μm.

4. Conclusions

In summary, we have successfully demonstrated the epitaxy of La-$SrSnO_3$/$BaTiO_3$/$SrTiO_3$-buffered Si perovskite heterostructure, with LSSO deposited via ALD. Additionally, the post-annealing optimization of the LSSO/BTO perovskite heterostructure for defect reduction has been systematically studied through capacitance *vs.* voltage measurement. The RHEED and XRD results indicated the excellent crystallinity of each epitaxy layer with an FWHM of 0.62°, RSM was used to calculate the unit cell parameters of LSSO and BTO films. The obtained unit cell parameters are a = 4.069 Å and c = 4.066 Å for LSSO film and a = 4.022 Å and c = 4.042 Å for BTO film. The XPS results confirmed no Sn^0 state in LSSO after *in-situ* annealing in 1 × 10^{-5} Torr O_2 ambiance. Moreover, we examined the effect of an additional *ex-situ* oxygen annealing process on the *C–V* performance for LSSO/BTO heterostructure devices. The precise control of the *ex-situ* annealing temperature and time with excess oxygen contributes to the explicit promotion of capacitance properties. The maximal oxide capacitance C_{ox} = 0.31 μF/cm² and minimum low-frequency dispersion were obtained in Device D with 7 h oxygen annealing at 400 °C. The promotion of capacitance properties mainly originates from decreased oxygen vacancies in films and interface defects in interfaces. Furthermore, this work shows that long-time annealing at high temperatures (500 °C or 600 °C) degrades the capacitance property due to fixed negative charges generation above 500 °C. These results suggest that the capacitance properties of the LSSO/BTO perovskite heterostructure can be improved by reducing defects in films and interfaces by suitable annealing conditions in excess oxygen.

Author contributions

Y. Zhang and S. Hu: conceptualization, investigation, methodology, data curation, formal analysis, writing – original draft, and writing – review & editing. P. Y. Chen: investigation, methodology, and data curation. J. Y. Zhu, B. J. Chen and R. X. Bai: software and Resources. H. Zhu, L. Chen and D. W. Zhang: validation, visualization, and writing – review & editing. J. C. Lee and Q. Q. Sun: conceptualization, validation, visualization, and writing – review & editing. J. G. Ekerdt.: conceptualization, investigation, formal analysis, funding acquisition and writing – review & editing. L. Ji: conceptualization, investigation, methodology, data curation, formal analysis, supervision, project administration, funding acquisition and writing – review & editing.

Conflicts of interest

There are no conflicts to declare.

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