Chem Soc Rev

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Journal:	*Chemical Society Reviews*
Manuscript ID	CS-REV-08-2018-000629.R1
Article Type:	Review Article
Date Submitted by the Author:	30-Aug-2018
Complete List of Authors:	Kagan, Cherie; University of Pennsylvania,

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Flexible Colloidal Nanocrystal Electronics

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ABSTRACT: Nanometer-scale crystals of bulk group IV, III-V, II-VI, IV-VI, I-III-VI_2, and metal-halide perovskite semiconductors, dispersed in solvents, are known as colloidal nanocrystals and form an excellent, solution-processable materials class for thin film and flexible electronics. This review surveys the size, composition, and surface chemistry-dependent properties of semiconductor NCs and thin films derived therefrom and provides physico-chemical insight into the recent leaps forward in the performance of NC field-effect transistors. Device design and fabrication methods are described that have enabled the demonstration and scaling up in complexity and area and scaling down in device size of flexible, colloidal nanocrystal integrated circuits. Finally, taking stock of the advances made in the science and engineering of NC systems, challenges and opportunities are presented to develop next-generation, colloidal NC electronic materials and devices, important to their potential in future computational and in Internet of Things applications.

INTRODUCTION:

Colloidal nanocrystals (NCs) are fragments, typically $\sim 2 - 20\ nm$ in length, of the crystalline lattice of bulk inorganic solids. To achieve colloidal dispersibility and to facilitate size- or shape-control during synthesis, they are commonly coordinated at their surfaces by organic or inorganic ligand shells [Fig. 1a].[1–3] Advances in synthetic methods now enable NCs to be prepared from group IV, III-V, II-VI, IV-VI, I-III-VI_2, and metal-halide perovskite semiconductors.[4–6] NCs are also often known as quantum dots, since for many compositions these particles are smaller than the semiconductor electron, hole, and/or exciton Bohr radii and confinement effects collapse the continuous density of states of bulk solids into discrete "atomic-like" electronic states.[1,7] The scientific community has prized colloidal semiconductor NCs for their rich chemical physics. Academic and industrial researchers have exploited NCs for their size-dependent properties in optoelectronic devices[8] and television manufacturers have commercialized semiconductor NCs for their near unity quantum yield of luminescence in displays.[9]

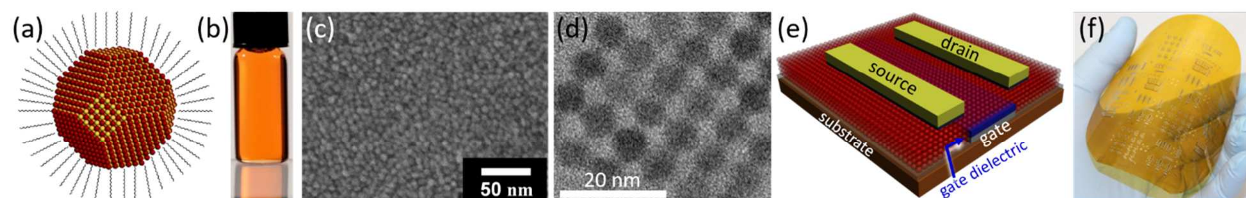

Figure 1. (a) Schematic of a single NC and (b) photograph of a dispersion of colloidal 4 nm diameter, SCN-capped CdSe NCs. (c) Scanning electron micrograph of a glassy thin film of 4 nm diameter, SCN-capped CdSe NCs (after annealing at 250 ^{o}C) and (d) an ordered domain in a thin film of 6 nm diameter, SCN-capped PbSe NCs. (e) Schematic of a NC thin film FET and (f) photograph of an array of CdSe NC integrated circuits fabricated on a 4" diameter, flexible, Kapton substrate. (b) is reproduced from Ref. 10 with permission from the American Chemical Society, copyright 2011. (c) is reproduced from Ref. 11 with permission from the American Chemical Society, copyright 2012. (d) is reproduced from Ref. 12 with permission from the American Chemical Society, copyright 2014. (f) is reproduced from Ref. 19 with permission from the American Chemical Society, copyright 2015.

As colloids, these NCs are dispersed in solvents [Fig. 1b][10] providing a solution-processable class of materials that can be coated, cast, and printed to form glassy [Fig. 1c][11] and ordered

(with nanometer to micron scale domain sizes depending on processing method) [Fig. 1d][12] thin film NC assemblies on rigid and flexible substrates.[13–15] In this review, we briefly introduce the synthesis, deposition, and electronic properties of colloidal NCs, as needed to describe the structure and electronic function of semiconductor NC thin films; for greater detail, we refer the interested reader to a number of excellent reviews of these topics. Here, we focus on the chemical-physical properties and fabrication methods that have led to rapid improvement in the performance of semiconductor NC thin films in field-effect transistors (FETs) [Fig. 1e], from device mobilities of $\mu_{FET} < 1\,{cm^2}/{Vs}$ to $\mu_{FET} > 10\,{cm^2}/{Vs}$, and their demonstration as device level building blocks of flexible NC electronic circuitry [Fig. 1f].[8,16–19]

COLLOIDAL NANOCRYSTAL SYNTHESIS AND DEPOSITION:

Non-aqueous, solvothermal synthetic methods are the most common routes developed to prepare compound semiconductor NCs. Briefly, NC precursors are injected at high-temperature into[20] or mixed at low-temperature and heated up in a flask[21] containing a high boiling point solvent and coordinating long-chain organic ligands to nucleate and mediate particle growth. These methods allow NCs to be tailored in size (with many syntheses yielding size distributions of <5%), shape, and internal structure and yield organic-ligand capped NCs that may be dispersed post-synthesis in solvents.[2,14,22,23] Elemental, group IV NCs are harder to prepare using wet-chemical methods, since they typically require higher synthesis temperatures that exceed the boiling point of organic solvents. High-temperature (>1000 ^{o}C) reductive processing of sub-stoichiometric thin films is used to nucleate and grow group IV NCs embedded in an oxide matrix.[24–26] Subsequent HF containing etchants are employed to harvest hydrogen-terminated NCs that can be reacted with alkenes to form organic-ligand capped NCs and colloidal dispersions. Non-thermal plasma

synthesis has also been shown to be a particularly effective route to prepare group IV NCs.[27] Collision between hot, free plasma electrons and gaseous NC precursors produce reactive radicals and ions and the high temperatures needed to nucleate and grow NCs. Plasma synthesis yields "bare" NCs that are collected on a substrate. These NCs can be used directly, noting that these compositions typically form oxide shells over time, or they may be ligated after synthesis to deagglomerate and disperse product NCs in solvents.

Colloidal NC dispersions may be deposited and patterned over large substrate areas by solution-based methods such as spin- or dip-coating, drop-casting, doctor-blading, and ink- and transfer-printing and imprinting.[15] The deposited thin films consist of ordered or randomly packed NC assemblies in which the distance between NCs (*i.e.*, interparticle distance d) is defined by the intervening ligand shell. The ligands commonly used to synthesize and disperse NCs yield assemblies with $1nm < d \lesssim 2nm$. At these interparticle distances, NCs are weakly electronically coupled, as electron and hole wavefunctions have little overlap, and charge transport is poor.[18,28]

To increase the conductivity of NC thin films for use in electronic and optoelectronic devices, methods have been developed to reduce $d < 1nm$ to more strongly couple the NCs by exchanging the ligands used in synthesis for shorter organic (*e.g.*, aliphatic or aromatic thiols or amines)[18,29,30] or compact inorganic ligands (*e.g.*, hydrazine,[16] metal chalcogenide complexes,[31] chalcogenides,[32] halides,[33] pseudohalides[10,34], or halometallates[34]) or to strip the ligands entirely.[35–38] There is an excellent recent review on NC surface chemistry by the Talapin and Hyeon groups.[39] These methods rely on introducing a new ligand that is competitive with the

original ligand for the NC surface and the selection of solvents in which the original ligands are highly soluble. For some NC and ligand chemistries in which the new ligand can electrostatically or sterically stabilize the NCs in solvent, it is possible to create a dispersion of NCs capped with the new ligand by adding a solution of the new ligand to a dispersion of the synthesized NCs. Figure 1b shows a photograph of a 4 nm diameter CdSe NC dispersion capped with the inorganic ligand thiocyanate (SCN), that is used to exchange well-known tri-octylphosphine oxide ligands used in NC synthesis.[10] These compact ligand-stabilized colloidal NC dispersions can then be deposited to form thin films with $d < 1nm$ [Fig. 1c].[11] For almost all NC compositions, ligand exchange or stripping can be realized by immersing a thin film assembly of NCs with the original ligands ($1nm < d \lesssim 2nm$) in a solution of the new ligand or a clean solvent to yield a NC film with $d < 1nm$ [Fig. 1d].[12,35,40] However, the lost ligand volume in the thin film solid often creates cracks. These cracks may be filled by multilayer NC deposition and exchange.[41]

RELATIONSHIP BETWEEN ELECTRONIC STRUCTURE AND CHARGE TRANSPORT IN COLLOIDAL SEMICONDUCTOR NANOCRYSTAL THIN FILMS:

Recent improvements in NC FET performance have arisen from advances in synthetic control of NC composition and size and in exploitation of NC surface chemistry to tailor d and doping in NC thin films.[8,17,18] The chemical-physical properties of NC thin films defines their electronic structure; *i.e.*, the energy, density and occupancy of states that dictate majority carrier type, concentration, and mobility important to charge carrier transport and ultimately to design of NC thin film channel materials for FETs. Charge transport has been probed spectroscopically and in the platform of the NC FET. Given the focus of this review on NC FETs and circuits, we choose figures that show the correlation between the chemical-physical properties of NC thin films with

their FET behavior, and with device metrics of mobility (μ_{FET}), current modulation $\left(\frac{I_{ON}}{I_{OFF}}\right)$, threshold (or turn-on) voltage (V_T), hysteresis (quantified by ΔV_T, the shift in V_T with the direction of the voltage sweep), and subthreshold slope (S). Spectroscopic studies which have contributed substantially to our understanding of charge transport in NC thin films are referenced.

The electronic structure or energy vs wavevector ($E\ vs\ k$) diagram of colloidal NCs is derived from that of the parent semiconductor composition and size-effects of quantum confinement.[1,7] Near the conduction and valence band extrema, bulk semiconductors are approximated by parabolic bands with curvature that defines the electron and hole effective masses [Fig. 2a, blue lines]. For strongly confined NCs, where the NC size is small compared to the electron and hole Bohr radii, carriers can be treated independently as a particle-in-a-box, where the NC composition dictates the bulk effective mass and the NC size and shape define the box dimensions and geometry. Quantum confinement effects, *i.e.*, the finite number of unit cells N with lattice constant a, quantize the allowed values of k to $\frac{2\pi m}{Na}$ where m is an integer (found by using periodic boundary conditions to represent the NC and Bloch's theorem such that $\Psi(x) = \Psi(x + Na) = exp(ikNa)\Psi(x) \Rightarrow exp(ikNa) = 1$) [Fig. 2a, green circles]. The first conduction $1S_e$ and valence $1S_h$ band states (where S refers to the wavefunction symmetry and e and h index the electron and hole) shift to larger values and the separation between states increases with decreasing NC size, giving rise to the well-known size-dependent band gap $E_{g,NC}(r) = E_{g,bulk} + \frac{\hbar^2\pi^2}{2r^2}\left[\frac{1}{m_e^*} + \frac{1}{m_h^*}\right] - \frac{1.8e^2}{\varepsilon_\infty r}$ seen in NC absorption and luminescence spectra, where r is the radius and ε_∞ is the static dielectric constant of the semiconductor.[1,42] The bulk band gap (1st

term) is increased by the confinement energy (2nd term) and, in large NCs, reduced by Coulombic electron and hole correlation (3rd term). The size-tunability of the band gap from large, bulk-like to small, ~2 nm NCs depends on the semiconductor electron (m_e^*) and hole (m_h^*) effective masses or, as easily visualized, the curvature of the semiconductor E vs k diagram [Fig. 2a].[43]

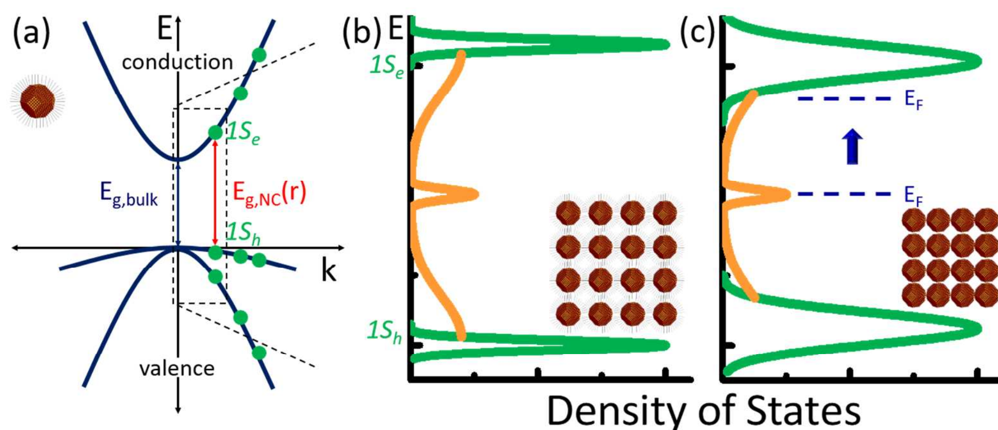

Figure 2. (a) Schematic energy (E) *versus* wavevector (k) diagram of a three-dimensional, bulk semiconductor (blue lines), showing the conduction and valence, light and heavy hole bands separated by the band gap energy $E_{g,bulk}$. For zero-dimensional, NCs small in size compared to the bulk carrier and exciton Bohr radii, quantum confinement effects quantize the allowed k-values (green circles) such that the first allowed k-values ($1S_e, 1S_h$) give rise to the larger effective band gap $E_{g,NC}(r)$. Schematic density of states diagrams highlighting the first conduction ($1S_e$) and valence ($1S_h$) band states (green lines) in thin film arrays of quantum confined NCs (schematic insets) capped by (b) ~ 2 nm ligands, as used in synthesis, and (c) by short, < 1 nm ligands, introduced by exchanging the ligands used in synthesis for compact organic or inorganic ligands. Tail and deeper mid-gap states (orange lines) are created by dangling bonds at the NC surface and by interfaces in NC devices. The Fermi energy (E_F) depends on the NC thin film doping concentration. (b, c) are adapted from Ref. 17 with permission from Springer Nature, copyright 2015.

In thin films of quantum confined NCs, each NC contributes a density of states of $g(E)_{NC} = M_{C,V} 2\delta\left(E - E_{C,V}\right)$ where $M_{C,V}$ is the number of equivalent conduction band minima or valence band maxima and $E_{C,V}$ is the energy of the discrete, lowest energy, conduction or valence band states.[1,7] $M_{C,V} = 1$ for group II-VI, most III-V, and I-III-VI_2 materials and $M_{C,V} = 4$ for IV-VI systems, as the conduction and valence band extrema are at the Γ-point and L-point,

respectively, notably increasing $g(E)_{NC}$ in IV-VI NC materials.[16] For Si and Ge, $M_V = 1$ and $M_C = 6$ and $M_C = 4$, respectively,[44] and $M_{C,V} = 1$ for metal-halide perovskites. In weakly coupled NC thin films, in which the NC ligand shell creates $d > 1\ nm$ [Figure 2b], the density of states of the constituent NCs add to give $g(E)_{NC\ film} = [NC]\sum g(E)_{NC} = [NC]\sum M_{C,V} 2\delta(E - E_{C,V})$. $g(E)_{NC\ film}$ is broadened by an approximate Gaussian distribution in $E_{C,V}$, which arises in large part from the NC size distribution and more subtly from influences such as differences in NC surface chemistry (*e.g.*, the number and type of surface atoms and ligands).[17] The inhomogeneous distribution in $E_{C,V}$ and broadening of $g(E)_{NC\ film}$ is seen in the linewidth of the $1S_h - 1S_e$ transition in optical absorption spectra and gives rise to variations in the energy landscape, or "site" energy, that are deleterious to charge transport in NC films,[45] motivating synthetic development of more molecular NC samples. $g(E)_{NC\ film}$ also depends on the concentration of NCs as $[NC] = {}^{PF}/_{V_{NC}}$. PF is the NC packing fraction (*i.e.*, PF=0.74 for close-packed and PF=0.64 for randomly close-packed NC assemblies) and $V_{NC} = \frac{4}{3}\pi\left(r + {}^{d}/_{2}\right)^3$ where r is the NC radius. The effective density of conduction and valence band states is then $N_{C,V} = 2M_{C,V}[NC]$. For NCs large compared to the Bohr radii, the well-known, three-dimensional density of states and therefore the effective density of states of the bulk semiconductor are "diluted" by the smaller volume fraction of atoms in the NC film.

In more electronically-coupled NC thin films with $d < 1\ nm$ [Fig. 2c], interaction between electron and hole wavefunctions on neighboring NCs increases and broadens the density of states,[46–50] and without sources of disorder is expected to give rise to band formation akin to that

in atomic solids.[17,18,51] However, in addition to the distribution in $E_{C,V}$ from dispersity in the NC sample, described above, most NC thin films with $d < 1\,nm$ studied to-date are glassy or have small ordered domains [Fig. 1c,d] and variations in d and in NC organization contribute energetic and positional disorder to the "site" energy. Current fundamental chemical physics and device research aim to develop processes that form periodic NC superlattices over large areas with short or no ligands, as is well developed with longer ligands.[13] Recent success has been seen upon ligand stripping in IV-VI NC materials.[35,40,52] That said, the dramatic improvement in charge transport and in NC FET performance is seen by reducing d in NC films, even in the presence of structural disorder.

The increased conductivity for shorter d is seen as the tunneling rate for charge $\Gamma \sim exp[-\kappa d]$ increases exponentially as d decreases and as the decay length of the carrier wavefunction $\kappa^{-1} = \left(2m^{*}\Delta E/\hbar^{2}\right)^{-1/2}$ increases, where ΔE is the energy barrier height between the NC and ligand.[8,16] Figure 3 shows a comparison after electrically-insulating 6 nm diameter, oleic acid capped PbSe NC thin films (with $d \sim 2\,nm$) are exchanged with different short organic ligands that create $d \sim 0.5 - 1\,nm$ [*e.g.*, benzene- and ethane-dithiol (BDT and EDT) and mercapto-propionic acid (MPA)] and compact inorganic ligands that yield $d < 0.5\,nm$ [*e.g.*, halides and the pseudohalide SCN] and then integrated as the semiconductor channel in FETs with various workfunction source and drain electrodes.[12] Transfer characteristics of EDT-exchanged [Fig. 3b] and SCN-exchanged [Fig. 3c] PbSe NC FETs are representative of the behavior seen for the classes of organic- and inorganic- ligand exchanged films. Regardless of the electrode metal selected, across the voltage range probed, the current levels in organic-ligand exchanged NC devices are $\times\, 10 - 10^{3}$ smaller than those of the inorganic-ligand exchanged NC devices,

consistent with the lower $10^{-4} - 10^{-1}\ {cm^2}/{Vs}$ ligand-length dependent μ_{FET} reported for organic-[53] *versus* μ_{FET} of $10^{-2} - 1\ {cm^2}/{Vs}$ for inorganic-ligand capped NC devices.[16,41] Note these mobilities should be considered as a guideline as they do not account for effects of unintentional doping[54] or for errors due to significant device hysteresis, particularly for organic-ligand exchanged NC devices.[12,45] The current-voltage characteristics for the organic-ligand exchanged NC devices are ambipolar and largely independent of the metal source and drain electrode workfunction [Fig. 3b], consistent with the high resistivity of the NC channel dominating the device resistance. This is in contrast to the metal workfunction dependent current polarity and magnitude for inorganic-ligand exchanged NC devices [Fig. 3c], where resistance from barriers to charge injection at the metal-NC interface are significant in comparison to the lower channel resistivity.

Temperature- and NC-size and length-dependent charge transport studies, reviewed elsewhere,[17] have shown that carrier motion in organic-ligand capped NC films operates *via* thermally-activated nearest neighboring hopping with an activation energy $E_A \sim 25 - 100\ meV$ near room temperature. Interestingly, smaller diameter NC films show lower conductivity, even though the wavefunction leakage κ^{-1} would increase,[45,55] and is accounted for by an increased self-charging energy $\propto {1}/{\varepsilon r}$ and inhomogeneity in $E_{C,V}$. As the NC film is densified for small d in inorganic-ligand capped NC films, the self-charging energy is expected to become small. If the exchange coupling energy $\beta \sim h\Gamma$ is large compared to the site-to-site variation in $E_{C,V}$ and the self-charging energy, a transition from localized to more extended electronic state formation is expected,[56–59] and evidence of band-like transport in high mobility NC films has been seen experimentally.[60–65]

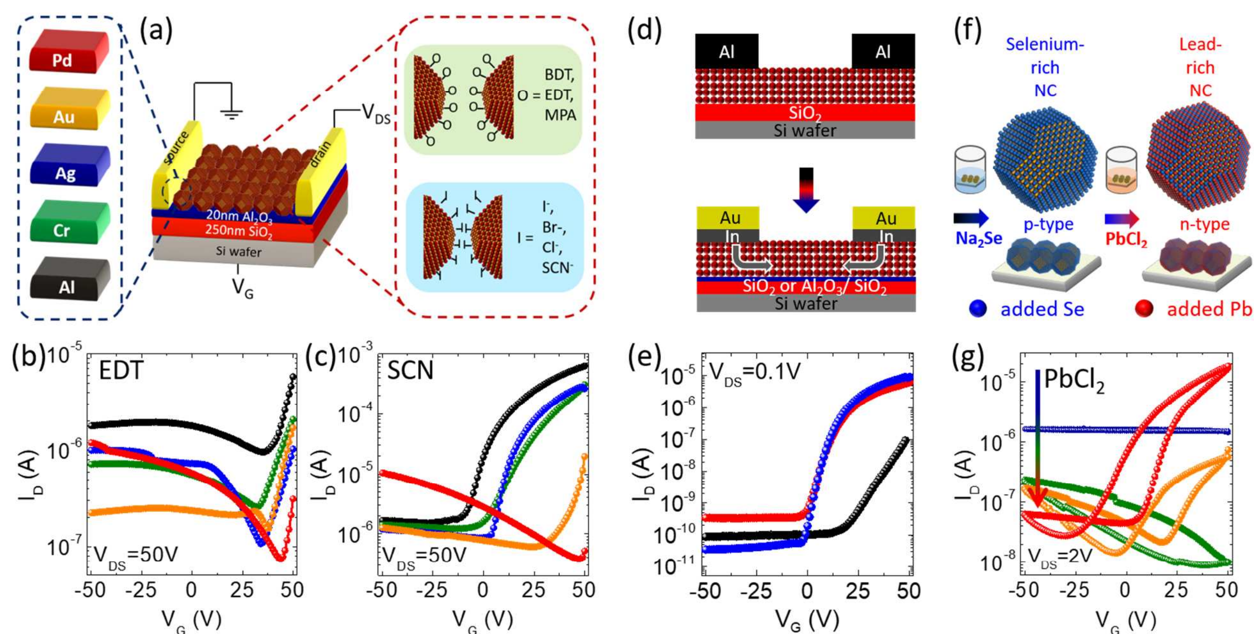

Figure 3. (a) Schematic of a FET fabricated with various metal source and drain electrodes (left box) and with semiconducting channels composed of NCs capped by (right box) short organic ligands [benzendithiol (BDT), ethanedithiol (EDT), mercaptopropionic acid (MPA)] (green box) or compact inorganic ligands (blue box). FET transfer characteristics with various contact metals (b) for EDT- and (c) SCN-exchanged, 6 nm diameter PbSe NC channel materials. (d) Schematic and (e) transfer characteristics of 4 nm diameter, SCN-capped CdSe NC FETs fabricated with (black) Al and (red) In/Au source-drain electrodes and an SiO_2 gate dielectric layer, and (blue) In/Au source-drain electrodes and an Al_2O_3/ SiO_2 gate dielectric stack. (f) Schematic of a solution-based, post-synthesis colloidal atomic layer deposition processes using metal salts to tailor NC thin film stoichiometry and thereby tune carrier type and concentration, allowing n-type and p-type FET fabrication. (g) FET transfer characteristics for 6 nm diameter PbSe NC channels upon (blue) Se-enrichment, by immersion in solution of Na_2Se, and subsequent Pb-enrichment, by immersion in a solution of $PbCl_2$ at 65 ^{o}C for (green) 1 h, (orange) 6 h, (red) and 12 h. (a-c) are adapted from Ref. 12 with permission from the American Chemical Society, copyright 2014. (e) is adapted from Ref. 11 with permission from the American Chemical Society, copyright 2012. (f, g) are adapted from Ref. 82 with permission from the American Chemical Society, copyright 2014.

In NC films, the large surface-to-volume ratio of the NCs creates the potential for a substantial density of tail and deeper mid-gap states within the NC thin film band gap [Figure 2b,c (orange lines)],[11,17,58,66] akin to that found in amorphous semiconductors.[67] These states may arise from surface dangling bonds or impurities[39,68] and non-stoichiometry created by atomic excess at the NC surface.[69] These intra-gap states may be "plugged" or shifted out of the band gap by adding

atoms or ligands to the NC surface. For example, introduction of organic ligands and/or overgrowth of an inorganic shell are well-known strategies to electronically passivate NC surface states.[70–72] In NC devices, like in organic and inorganic thin film devices, intra-gap electronic states may also be introduced at metal-semiconductor and semiconductor-gate dielectric heterointerfaces.[17]

Electronically, unlike in bulk single crystals where carriers occupy and move with the mobility of the conduction or valence band, intra-gap states in NC films create a dependency of the energy and mobility of carriers on the position of the Fermi energy (E_F) [Fig. 2c].[73] The energy distribution of carriers depends on the product of the density of states and the Fermi-Dirac function.[44] In NC films, as in amorphous semiconductors,[67,74] if E_F is coincident with deep mid-gap states, then charge will be localized in these states. However, if E_F is shifted toward $E_{C,V}$ by doping, or electrostatically by the gate voltage in NC FETs, for sufficient kT (where k is Boltzmann's constant and T is temperature) charge will be distributed in high density, high mobility conduction or valence band states.

The methods used to electronically dope colloidal NC thin films for integration in FET devices depends on their synthetic route. Much like impurity doping of bulk semiconductors, colloidal NCs prepared by plasma routes are typically substitutionally-doped by introducing dopant precursors during synthesis.[27,75] There have been recent developments to introduce impurities in the NC core during solvothermal synthesis,[74,76–79] however it has proven more challenging.[80,81] Commonly these NC systems are doped by modifying their surface chemistry with additional atoms, ions, or ligands in the last steps of synthesis or after film deposition, taking advantage of

the large surface-to-volume ratio of NCs.[10,54,69,82,83] These surface species act as “remote dopants” that transfer charge to the core, akin to modulation doping in semiconductor heterojunctions.[84–86] The ligand chemistry at the NC surface also affects the absolute energy of $E_{C,V}$[87] and therefore controls the efficiency of charge injection in NC FETs.[12,88]

Figure 3d,e shows the dramatic influence of doping on device characteristics by comparing the transfer characteristics of SCN-capped, CdSe NC FETs fabricated by thermal evaporation of Al electrodes and of similar workfunction In electrodes (capped by Au).[62] The NC FETs are annealed at 250 °C, which further reduces d as SCN decomposes to leave a S-rich surface and, uniquely for devices with In-electrodes, drives In diffusion over large $100\ \mu m$ channel lengths. Indium is known as a low ionization-energy *n*-dopant in bulk CdSe and has been used historically to dope polycrystalline CdSe thin film FETs.[89] The increase in electron concentration (Δn) upon doping in the FETs is readily seen by the negative shift in threshold voltage as $\Delta V_T \propto \Delta n$ and the increase in I_{ON} for In-doped devices. The shift in E_F results in an increase in μ_{FET} from $\sim 10^{-2} - 10^{-1}\ {cm^2}/{Vs}$ for devices with Al contacts to $\mu_{FET} \sim 20\ {cm^2}/{Vs}$ for devices with In electrodes. The increase in μ_{FET} and a reduction in device hysteresis (not shown) are consistent with electronic passivation of intra-gap states and with doping, allowing carriers to access a higher density, higher mobility density of states.

Material stoichiometry and therefore vacancy formation is also known to influence carrier type and concentration in bulk, compound semiconductors.[90] The large surface-to-volume ratio of NCs allows substantial control over material stoichiometry and provides another route to dope NC thin films.[54,69,86,91] Thermal evaporation of metal and solution-based addition of metal salts

alter NC thin film stoichiometry and therefore doping levels. PbSe provides an interesting example as it has a mirror-like $E\ vs\ k$ diagram such that $m_e^* = m_h^*$.[92] Stoichiometry can be used to tune from undoped to degenerately *n*- or *p*-doped NC films.[54] Figure 3f,g show an example of the influence of stoichiometric control of carrier type and concentration on the transfer characteristics of 6 nm PbSe NC FETs as Se-rich films are *p*-type and Pb-rich films are *n*-type.[82]

Interestingly, while methods are being developed to dope NC thin films, the efficiency of doping is often low.[54,74] This is attributed to concentrations of unidentified traps,[80] self-compensation,[80,93–95] and dopants that are ineffectively bound,[54,81] consumed by surface redox reactions, and/or bound but not ionized.[96] Studies have shown that dielectric confinement effects increase the ionization energy of dopants in low-dimensional materials.[97] Doping efficiency is important as increased concentrations of impurities are expected to increase carrier scattering and be deleterious to charge transport in devices. Infilling the NC thin film with high dielectric constant materials is seen to increase doping efficiency $\times 10$.[98] High levels of doping are also needed as an insulator-to-metal transition and high mobility charge transport is theorized and seen experimentally to require carrier concentrations of ~10^{19} cm^{-3}, higher than that in bulk semiconductors.[17,99,100]

Exceptionally high, near-bulk $\mu_{FET} > 400\ \frac{cm^2}{Vs}$ have been reported by the Talapin group upon sintering colloidal semiconductor CdSe NCs ligated with chalcogenidometallate ligands that serve as "molecular-scale solders."[101,102] These mobilities exceed those typically reported for polycrystalline thin films, providing an intriguing potential advantage for interfacial chemical design and nanostructuring of materials and an avenue for solution-based processing of high-

performance electronic materials. However, the current chemistry requires use of corrosive hydrazine and the largest mobilities are found for high annealing temperatures that are incompatible with plastic substrates targeted for flexible electronics.

Table I provides examples of high-performance NC FET characteristics reported for group IV, III-V, II-VI, IV-VI, and I-III-VI_2 semiconductors. In general, these high μ_{FET} are found by reducing d and by doping (in comparison to a similar table assembled in the year 2010),[18] and is to-date found for CdSe, PbSe, and InAs NC channels. In part, this difference in composition may arise from the community's long history in exploring and developing colloidal CdSe NCs, as a synthetically and spectroscopically accessible model material to study size-dependent properties, and IV-VI NCs, as infrared absorbing materials to complement Si in optoelectronic devices.[103,104] Interestingly, so far, empirical observation shows the element in the middle of the family, *i.e.*, Se or As, has proven "just right." Also, Table I is full of examples of high μ_{FET} *n*-type FETs, with fewer examples of *p*-type FETs. This difference in FET polarity may arise from the inherent asymmetry in the band structure, which typically yields $m_e^* > m_h^*$,[44] and in effects of self-compensation,[95] that can be traced back to their parent semiconductor.

Table I. Example Nanocrystal Field-Effect Transistor Characteristics

Group	Material	Treatment	NC diameter (nm)	μ_{FET} (cm^2/Vs)	$\frac{I_{ON}}{I_{OFF}}$	Ref.
IV	Si	none	10-20	$\mu_n \sim 10^{-5} - 10^{-6}$	10^2	105
	Ge	400 °C anneal	6	$\mu_n = 0.02$	$>10^3$	105
		600 °C anneal	6	$\mu_p = 0.006$	$>10^3$	105
III-V	InP	$Sn_2S_6^{4-}$, 350 °C RTA	3.8	$\mu_n = 0.09$	10^2	106

	InAs	$Cu_7S_4^-$, 350 °C RTA	4.5	$\mu_n = 16$	10^3	106
	InSb	S^{2-}	4.5	$\mu_n \sim \mu_p = 1.5 - 6 \times 10^{-4}$	<10	107
II-VI	ZnO	230 °C anneal, $Zn(NO_3)_2$ + $C_2H_4(NH_2)_2$, 230 °C anneal	10 ×65 rods	μ_n =0.6	>10^5	108
		In-doped, 400 °C anneal	3-5	μ_n =5	>10^4	109
	CdSe	$In_2Se_4^{2-}$, 200 °C anneal	3.9	μ_n =16	10^4	60
		SCN^-, In-doped, 250 °C anneal	3.9	$\mu_n = 27$	10^6	11
		$[Cd_2Se_3]^{2-}$, 350 °C anneal	4.7	$\mu_n = 400$	10^4	102
IV-VI	PbS	N_2H_4	8.5	$\mu_n = 0.1$	>10^3	110
		CH_3NH_3I + PbI_2	~3	$\mu_n = 0.1$	10^6	111
	PbSe	N_2H_4	9.2	$\mu_n = 0.95$	10^3	16
		CH_2O_2	6.1	$\mu_p \sim 10^{-2}$	<10	112
		SCN^-, Pb-doped	6	$\mu_n = 10$	10^2	54
		SCN^-, Se-doped	6	$\mu_p = 0.4$	>10^1	54
		S^{2-}, $PbCl_2$	6	$\mu_n = 7$	>10^2	12
		S^{2-}, ALD Al_2O_3 75°C	6.3	$\mu_n > 7$	10^3	113
		CH_3NH_3I, 120 °C anneal, benzyl viologen	3.6	$\mu_n = 0.64$	10^3	114
	PbTe	N_2H_4	~5	$\mu_n = 0.95$; $\mu_p = 0.15$	NR	115
I-III-VI$_2$	CuInSeS	$C_2H_4(SH)_2$	NR	$\mu_p > 10^{-3}$	NR	116

*NR=not reported. Note: colloidal nanowires or nanobelts are not included.

Above, emphasis has been placed on the choice of semiconductor NC material to improve device I_{ON}, *ie.*, routes to increase carrier concentration and mobility. However, $\frac{I_{ON}}{I_{OFF}} > 10^4$, and for display applications, $I_{OFF} \sim pA$ are needed.[89] Comparison of II-VI and IV-VI NC FETs in Figure

3[11,12,82] and of reported InAs NC FETs[64] shows lower I_{OFF} and greater $\frac{I_{ON}}{I_{OFF}}$ for FET devices made from wider band gap NC films. In FETs, the carrier concentration can be modulated by the gate field from the doping level, which can only be as low as the intrinsic carrier concentration $n_i = \sqrt{N_C N_V} exp\left(-\frac{E_g}{2kT}\right)$ in undoped films, to where the film becomes metallic. The size-dependent band gap of colloidal NCs opens up a potentially wider range than in the bulk of semiconductor compositions suitable for FETs.

As discussed below, the optimization in FET design and the demonstrations of NC electronic circuits, have therefore almost exclusively used semiconductor channels composed of CdSe NCs, for their high *n*-type μ_{FET} and $\frac{I_{ON}}{I_{OFF}}$ to realize *n*-type metal oxide semiconductor (NMOS) electronics, and PbS or PbSe NCs, for their high *n*-type and *p*-type μ_{FET} to show complementary metal oxide semiconductor (CMOS) electronics.

COLLOIDAL NANOCRYSTAL FIELD EFFECT TRANSISTOR DESIGN:

Materials selection of the semiconductor channel (described above) as well as of the metal and insulator used to form the electrodes and gate dielectric layer affects the energy and density of states at device interfaces and can significantly influence FET characteristics. The best performance NC FETs have been fabricated in the top-contact, bottom-gate geometry. Top contacts provide a more “intimate” metal-NC interface[117] and the bottom gate offers greater simplicity in fabrication of devices incorporating “emerging” materials.

The interface between metals and non-degenerate semiconductors, particularly those with more covalent character (*i.e.*, a smaller difference in electronegativity between constituent atoms),

notoriously suffer from complete or partial Fermi level pinning.[44] Formation of a high density of interface states creates Schottky barriers that cannot or can only be limitedly controlled by choice of metal workfunction. Since NCs are small fragments of the bulk semiconductor, it is not surprising that the metal-semiconductor NC interface may also be completely or partially pinned. The SCN-exchanged PbSe NC FETs in Figure 3c show partial Fermi level pinning, as the Schottky barrier height can only be tuned by 10% of the difference between the various metal workfunctions, even though the polarity and magnitude of the current can be controlled by choice of metal workfunction.[12,118] Schottky barriers can improve the FET $\frac{I_{ON}}{I_{OFF}}$, however they undesirably suppress device I_{ON}.

Again, taking a lesson from bulk semiconductor devices, where the semiconductor industry creates thin tunnel barriers by heavily doping semiconductors at contact interfaces, the same strategy can be employed in NC FETs. In-doped CdSe NC FETs [Fig. 3d,e] show heavy In-doping through the film thickness (as typical film thickness' in FETs are 40 nm).[62] Output characteristics (shown below) show linear behavior at low bias and no measureable contact resistance in transmission line method characterization. Manipulation of doping concentrations by controlling stoichiometry has also been exploited to engineer Schottky barriers in IV-VI NC devices.[54]

The choice and surface chemistry of the gate dielectric layer in NC FETs presents similar concerns as it does in many other organic and inorganic semiconductors explored for FETs.[119–122] Surface hydroxyl groups on thermally-oxidized, heavily-doped Si wafers, the common starting point for FET fabrication using new materials, are known to create electronic states that tail into

the band gap and increase carrier scattering and trapping.[123] Hiding the SiO_2 surface by deposition of a thin Al_2O_3 layer is seen to cut down the interface trap density to ~65% in CdSe NC FETs [Fig. 3d,e], increasing $\mu_{FET}{\sim}27\ {cm^2}/_{Vs}$ (a 40% increase) and S and significantly reducing device hysteresis.[11] In general, metal oxide (*e.g.*, ZrO_2, HfO_2, and Al_2O_3) gate dielectric layers have been shown to improve NC FET performance,[124,125] and as seen below, exploiting their high dielectric constants and the fabrication of ultrathin films by atomic layer deposition has enabled low voltage device operation. Modification of gate oxide surfaces using self-assembled monolayers is also used and effective. Here the NC community has adopted strategies for gate oxide selection used previously in polycrystalline CdSe FETs and in other thin film FETs.[89,126,127]

DEMONSTRATION AND FABRICATION NANOCRYSTAL CIRCUITS

Improvements in NC FET materials and device design motivate the realization of circuits, connecting multiple devices together to increase the complexity of electronic function. The first reported NC circuits have been constructed by externally wiring together two discrete NC FETs.[124,128] These reports demonstrate the function of the simplest circuit-level building block in an inverter, showing the attributes of switching of high and low input/output voltage and gain needed to realize digital and analog electronics. However, these examples lack the scalability in device number and density required to create more complex circuit topologies and the function found in integrated devices.

Integrated circuits require the fabrication of multiple transistors on the same substrate with minimal variation in device parameters and of vertical interconnect access (VIA) holes to

connect different device layers and form circuit topologies. The first demonstration of nanocrystal integrated circuits (NCICs) builds on previous work using SCN-capped CdSe NCs to construct *n*-type FETs with In/Au source and drain electrodes deposited through a shadow mask [Fig. 3d,e]. However, in place of a thick Al_2O_3/SiO_2 gate dielectric stack on a Si wafer, this work grows ultrathin Al_2O_3 gate dielectric layers on top of Al gate electrodes atop Kapton substrates.[129] This design enabled translation of the high-performance NC FETs operating at high voltages and on rigid Si substrates [Fig. 3d,e] to devices operating at low voltages and on flexible plastic substrates [Fig. 4a,b]. The devices show a linear $\mu_{FET} = 21.9 \pm 4.3\ {cm^2}/{Vs}$ at $V_{DS} = 0.1\ V$ and a saturation $\mu_{FET} = 18.4 \pm 3.6\ {cm^2}/{Vs}$ at $V_{DS} = 2\ V$. At $V_{DS} = 2\ V$, $\frac{I_{ON}}{I_{OFF}} > 10^6$, $V_T = 0.38 \pm 0.15\ V$, $\Delta V_T = 0.25 \pm 0.07\ V$, and $S = 0.28 \pm 0.09\ {V}/{dec}$. To integrate these NC FETs into circuitry, an additive process for VIA formation is developed. Through a shadow mask, Au is selectively deposited on the Al gate lines only in the location of the VIA. A subsequent oxygen plasma treatment and ALD deposition is used to grow high quality Al_2O_3 gate dielectric layers on the exposed Al gate lines, but form an unstable oxide on the Au VIAs, allowing them to retain their high conductivity.

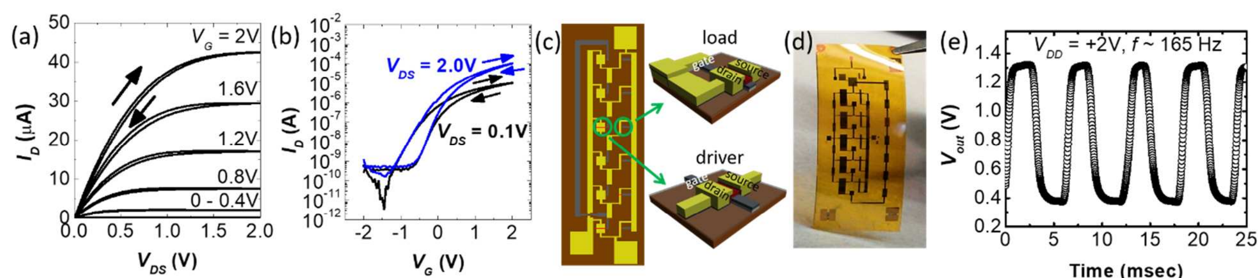

Figure 4. (a) Output and (b) transfer characteristics of a SCN-capped CdSe NC FET with In/Au electrodes and a 30 nm thick Al_2O_3 gate dielectric layer fabricated on an Al gate atop a flexible Kapton substrate. (c) Schematic, highlighting constituent load and driver NC FETs in each stage, (d) photograph and (d) output characteristics of a five-stage NCIC ring oscillator with a sixth-stage buffer operating at a supply voltage ($V_{DD} = 2V$). (a, b, d, e) are reproduced from Ref. 129 with permission from Springer Nature, copyright 2012.

Since the CdSe NC FETs are *n*-type, devices are connected using the VIAs to create inverters in a saturated load design, where one FET serves as the load (since its drain and gate electrodes are connected, $V_{DS} = V_G$ and the FET is always in saturation above V_T) and the other as the driver [Fig. 4c]. Using this process, multiple inverter stages are "strung together" to form five-stage ring oscillators [Fig. 4c,d]. The fifth inverter stage is connected to the input of the first inverter stage, giving the requisite odd number of stages to alternate high/low output/input voltage for ringing. A sixth-buffer stage is added to minimize load and interconnect capacitances introduced by the measurement probes. The ten NC FETs comprising the five-stage oscillator are fabricated over a $2\,cm \times 6\,cm$ area and have sufficiently uniform parameters to operate in concert and yield an output signal with characteristic ringing [Fig. 4e]. The oscillation frequency $= 165\,Hz = \frac{1}{2\times N\times\tau}$, where $N = 5$ for the five stages, giving a signal delay per inverter stage $\tau = 606\,\mu s$. The publication also reports common source voltage amplifiers (not shown) with a NMOS (n-type metal oxide semiconductor) saturated load, where the voltage gain of ~2 is defined by the ratio of the width and length of the driver and load NC FETs. In these first demonstrations of NCICs, the signal delay of the ring oscillator and the $f_{3dB}{\sim}900\,Hz$ bandwidth

(defined by the frequency region where gain is within 3dB of the maximum gain) of the amplifier are limited not by transport in the NC FET, but by parasitic capacitances arising from large overlaps between the gate and source/drain electrodes. The large device dimensions are readily seen in the photograph of the oscillator in Fig. 4d and are inherent to their fabrication. The fabrication of these devices is a tour d' force as each layer of the circuits is defined by shadow masks and aligned using an optical microscope mounted in a nitrogen glovebox. This same fabrication process has also been used to demonstrate integrated NMOS circuits from PbSe NCs.[12] Greater detail of CdSe NCIC characteristics is provided below in description of the next-generation of devices with improved performance.

The report of NCIC operation further prompts the development of fabrication processes that allow the scaling up of device and circuit fabrication over large area substrates and the scaling down of device dimensions to increase device density and the bandwidth and speed of analog and digital circuits. However, NC FETs have typically been fabricated in nitrogen gloveboxes and use dry processes (*e.g.*, evaporation of source and drain electrodes through shadow masks, as shown in all the NC FETs and NCICs described above) as the high surface-to-volume ratio and reactivity of semiconductor NCs makes them sensitive to air and to solvents. IV-VI NCs are particularly sensitive, as even <1 ppm oxygen and water levels in the nitrogen glovebox allow for adsorption of oxygen and *p*-doping of films.[125,130] Figure 5a shows the degradation of high-performance CdSe NC FET behavior (blue) upon ambient air-exposure (green).[131] Similar degradation (not shown) is seen upon solvent exposure, especially for water exposure. The degradation is consistent with evidence of oxygen and water adsorption at the NC and device interfaces creating trap states, akin to those formed upon oxygen adsorption to the surface of

bulk CdSe[132] and for water adsorption at gate oxide interfaces in other thin film FETs.[119,123] Interestingly, for CdSe NC FETs with In metal incorporated in the source and drain electrodes, it has been shown that re-annealing devices in a nitrogen environment allows for water and oxygen desorption and for additional In diffusion to repair the detrimental effects of air or solvent exposure, recovering high-performance NC FET characteristics [Fig. 5a, black].[131] Device repair processes allow circuit fabrication to be taken out of the glovebox and opens up the use of conventional ambient air and solvent based fabrication methods employed in Si processing as well as unconventional techniques being developed for emerging materials.

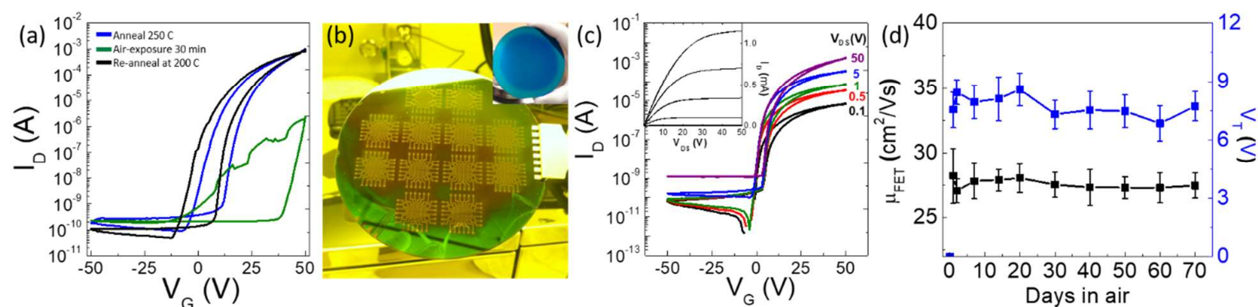

Figure 5. (a) Transfer characteristics of a SCN-capped CdSe NC FET with In/Au electrodes annealed at 250 °C for 10 min (blue), after air-exposure for 30 min (green), and after re-annealing at 200 °C for 5 min. (b) Photograph of (inset) SCN-capped CdSe NC thin films deposited on a 4 inch, Al_2O_3 (20 nm)/SiO_2 (250 nm)/Si wafer, and after lithographic-patterning of source-drain electrodes, to complete fabrication of 144 NC FETs. (c) Representative transfer and (inset) output characteristics and (d) μ_{FET} and V_T following 6 devices as a function of time stored in air for NC FETs encapsulated by 50 nm of Al_2O_3. Figure is adapted from Ref. 131 with permission from the American Chemical Society,

Figure 5b (inset) shows a photograph of a SCN-capped CdSe NC thin film deposited by spin-coating over a 4 inch diameter, Al_2O_3 (20 nm)/SiO_2 (250 nm)/Si wafer. A 1 nm, submonolayer of Al_2O_3 is deposited to prevent delamination during subsequent lithographic processing. Conventional photolithography is used to pattern an array of thermally-deposited In/Au source and drain electrodes on top of the CdSe NC film to complete the fabrication of 144 top contact devices [Fig. 5b]. Photolithography using a common university contact mask aligner allows

reduction in channel lengths down to $\sim 2\ \mu m$, compared to the smallest typical $\sim 30\ \mu m$ channel lengths realized with shadow masks. Using an ALD tool in the cleanroom, 50 nm of Al_2O_3 is deposited to encapsulate the devices. The slow growth of ALD Al_2O_3 at 150 °C is sufficient for In diffusion and repair in a single step. Fig. 5c shows representative output (inset) and transfer characteristics of a lithographically-patterned, Al_2O_3-encapsulated NC FET. Electrical characterization shows all 144 devices are recovered after fabrication and form high mobility devices with a linear $\mu_{FET} = 26.9 \pm 1.3\ {cm^2}/{Vs}$ at $V_{DS} = 5\ V$. Interestingly, the ALD infilling process, introduced by the Law group,[113,133] also reduces inter-related effects of device hysteresis (seen in Fig. 5c), bias stress,[134] and noise[135] and may lower the ionization energy for more efficient NC doping.[98]

Building upon the repair process for CdSe NC FETs that opens up the use of conventional fabrication processes, the next NCIC demonstration uses photolithographic patterning to scale down device dimensions and reduce parasitic capacitances, and scale up fabrication across 4" diameter flexible substrates [Fig. 1f].[19] A new process for VIA fabrication is developed to similarly scale it down in size and scale it up over large areas. Here, gate electrodes are constructed from a metal stack of Ti/Au/Ti/Al as the top Al layer is required to subsequently grow a high quality Al_2O_3 gate dielectric layer by oxygen reactive ion etching (RIE) and ALD deposition, as described above [Fig. 4]. A chlorine etch is used to open the VIA holes. However, since the chlorine etches both the Al_2O_3 and the underlying Al layer, the Au layer is introduced in the metal gate stack to serve as an etch stop that also maintains conductivity with a subsequently deposited Au VIA. The remaining steps are similar, with exception for subtle changes in the In-doping process, to those used to fabricate CdSe NCICs in Fig. 4.

Figure 6 shows examples of photolithographically-patterned, Al_2O_3-encapsulated CdSe NCICs that are fabricated on flexible substrates. Figure 6a,b shows a photograph and voltage transfer characteristics (VTC) of a NCIC inverter, showing the inversion of low (high) V_{IN} to high (low) V_{OUT}. Since these NCICs are based on a saturated load design, the voltage swing in the VTC of 78±1% is equal to $V_{DD} - V_T$ for all V_{DD}, noting V_T depends on V_{DD} as NC FETs have a gate bias dependent mobility derived from $g(E)_{NC\,film}$, as described in Fig. 2c, and also found in amorphous, organic, and hybrid semiconductor devices.[67,126,136] The noise margin [Fig. 6b] is adequately large to support signal switching through logic low/high for multistage digital circuit operation.

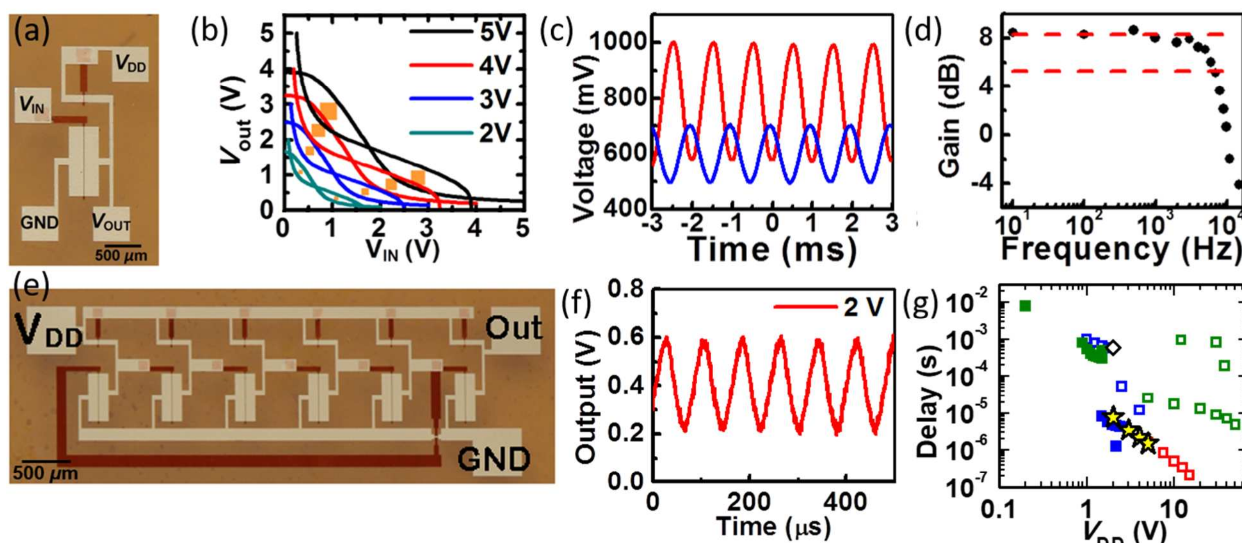

Figure 6. (a) Photograph of a flexible CdSe NCIC inverter fabricated by photolithography and its (b) voltage transfer characteristics, overlaid with its mirror image ($V_{IN} = V_{OUT}$ mirror plane) to show the noise margin (orange squares) as a function of supply voltage V_{DD}. (c) Output waveform (red) of a CdSe NCIC voltage amplifier in response to a 1 kHz, 200 mV sinusoidal input on a 600 mV DC input bias (blue). (d) Bode plot of the frequency response of the NCIC voltage amplifier (black circles). Low frequency voltage gain (red dashed line, top) is used to find the 3 dB bandwidth (red dashed line, bottom). (e) Photograph and (f) output characteristics at V_{DD}=2V of a flexible CdSe NCIC ring oscillator. (g) Comparison of the delay per stage *versus* V_{DD} for solution-processable, semiconducting (green) organic, (blue) carbon nanotube array, and (red) sol-gel metal oxide. Circuits fabricated on (filled symbols) rigid and (open symbols) flexible substrates. Colloidal NCICs on rigid (filled black) and flexible (yellow-filled stars). Figure is reproduced from Ref. 19 with permission from the American Chemical Society, copyright 2015.

The NCIC inverter [Fig. 6a,b] is operated as a common source voltage amplifier [Fig. 6c]. At $V_{DD} = 2V$, a V_{IN} composed of a 1kHz, 200 mV sinusoidal signal superimposed on a 600 mV DC offset is applied. The DC offset is selected so the inverter operates at the point of maximum gain (at $V_{DD} = 2V$). The output signal shows an anticipated gain of -2 V/V and an offset at 780 mV, consistent with the VTCs [Fig. 6b]. The frequency dependence of the voltage gain [Fig. 6d] is used to find f_{3dB}~$7\ kHz$, which is nearly $\times 8$ larger than that of the first generation NCICs, consistent with reduced parasitic capacitances in the lithographically-scaled devices.

Five-stage NCIC ring oscillators (with a sixth-stage buffer) are also fabricated as shown in the photograph in Figure 6e. The output characteristic (at $V_{DD} = 2V$) has an oscillation frequency of 13 kHz, yielding a $\tau = 7.7\ \mu s$, which is $\times\ 100$ smaller than the earlier oscillator in Fig. 4e. The V_{DD}-dependent switching delay of NCICs is compared to that for other solution-processable semiconductors fabricated on rigid and flexible substrates. The small switching delay at low voltages shows the competitiveness of solution-processable, colloidal NC materials for flexible electronics.

NCIC logic NAND and NOR gates, one step more complicated digital circuitry, have also been demonstrated [Fig. 7]. In these circuit topologies, two driver NC FETs A and B are disposed in series and in parallel for the NAND and NOR gates, respectively. V_{OUT} follows the anticipated truth tables for the logic gates, where V_{OUT} is "off" or "0" if V_{IN} on both A and B drivers in the NAND gate is "on" or "1" and V_{OUT} is "off" or "0" if V_{IN} on either A and B drivers in the NOR gate is "on" or "1" [Fig. 7b,c].

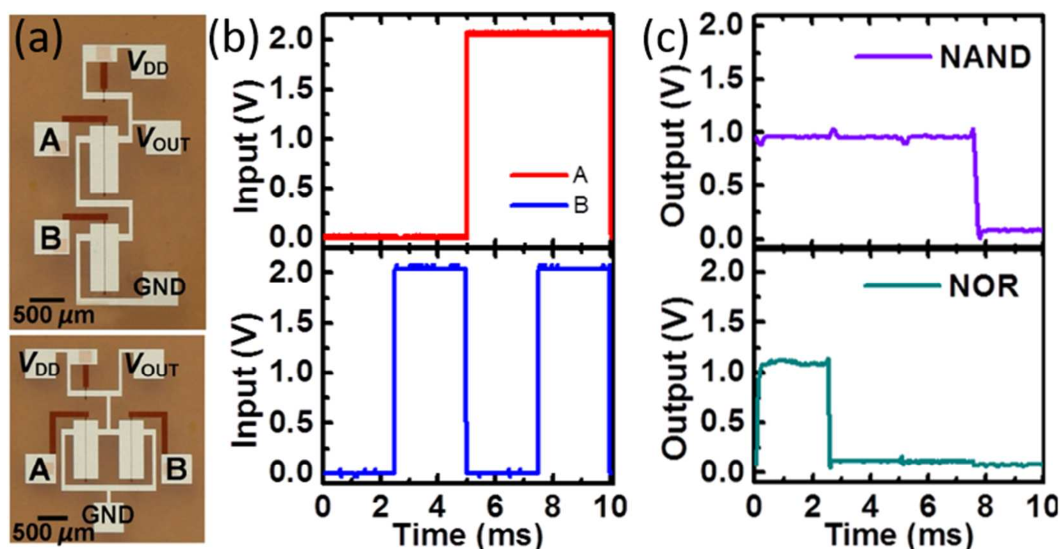

Figure 7. (a) Photographs of (top) NAND and (bottom) NOR logic gates. (b) V_{IN} applied to the A (red) and B (blue) driver NC FETs and (c) V_{OUT} for NCIC NAND (purple) and NOR (green) logic gates with $V_{DD} = 2V$. Figure is reproduced from Ref. 19 with permission from the American Chemical Society, copyright 2015.

The CdSe NCICs detailed above are all NMOS devices. Complementary NCIC inverters have been demonstrated from IV-VI NC materials. The first example exploits the *n*-type and *p*-type NC FET characteristics realized using low-workfunction Al and high-workfunction Au source and drain electrodes to shift V_T [Fig. 3c].[12] The FETs are integrated by sequentially depositing Al and Au so that the Al drain of the *n*-type FET is connected to the Au source electrode of the *p*-type FET. Colloidal NCICs have also been demonstrated by selectively *n*- and *p*-doping adjacent regions of IV-VI materials, in this case colloidal nanowires, through stoichiometric control, by adding excess Pb and Se, respectively.[137] These CMOS NCIC inverters have higher gains of ~15, compared to NMOS devices where gain is limited by the constituent FET device dimensions.

SUMMARY AND OUTLOOK

Recent advances in our fundamental understanding of the chemical-physical properties of size-, composition-, and surface-engineered, colloidal semiconductor NC materials and in our fabrication of their devices have led to the demonstration and scaling of large area, flexible colloidal NCICs. So what's next?

Almost exclusively NCICs have been incorporated CdSe and PbSe NCs, building on the community's expertise in exploring these compositions. CdSe NC thin films are selected for their high n-type μ_{FET} and $\frac{I_{ON}}{I_{OFF}}$ to realize n-type metal oxide semiconductor (NMOS) electronics, while PbSe NC materials are chosen for their high n-type and p-type μ_{FET} to show complementary metal oxide semiconductor (CMOS) electronics. Can we develop new process that are compatible with plastics that exploit the high mobility of sintered CdSe NC films that have estimated MHz switching speeds?[102] For electronics, can we develop p-type NC materials with similar performance to that of CdSe NC films? For consumer and Internet of Things applications, such as wearable, implantable, and integrated devices for health and agricultural monitoring; regulations may limit use of Cd-, Pb-, and As-containing materials. Can we apply what we have learned to expand the range of NC compositions that can be fabricated to form high performance NC FETs and their ICs, or can we develop processes for heterogeneous integration with other solution-processable p-type semiconductors? ALD infilling of NC devices has allowed demonstration of air-stable operation,[131] but this is just the start. Studies are needed to characterize NC FET and NCIC air, water, and mechanical stability in order to ensure device stability in the environments and under the conditions of their application specific operation, and

to explore encapsulation and device design strategies reported in other solution-processable and flexible materials systems.[138–140]

Currently NCICs are fabricated in which only the semiconductor channel is constructed from colloidal NCs and the metal and gate dielectric layers consist of evaporated or ALD grown materials. Recently, it is shown that all device layers could be fabricated from solution-processable, metallic, semiconducting, and insulating colloidal NCs to realize FETs on flexible plastics with excellent performance.[141] Can we develop more complex fabrication processes, using some mix of conventional and ingenious techniques, to meet the vision of on-demand, printed, solution-processable electronics? While in this review the use of conventional resist-based, photolithography is described, a recent report shows that it is possible to design photosensitive NC materials that avoid the detrimental effects of resist chemistry, and yet allows the patterning of a wide range of NC materials.[142] Nanoimprint lithography can also be used to directly pattern NC films without resists.[143]

Finally, if we can take colloidal NCs out of nitrogen gloveboxes and use more fabrication techniques, are there opportunities where NC electronics can augment Si technology? Can we tailor the density of states of colloidal NC materials to design FETs with nonlinearities useful to circuit designers? Can we expand computational power by exploiting the low-temperature processing of colloidal NCICs to build on top of Si electronics and construct circuitry in three-dimensions? Can we exploit the expansive library of colloidal NC metals, semiconductors, insulators, magnets, *etc.* which can be synthesized, assembled, and integrated into devices using

similar processes and add new, useful functions, for example, for integrated optics or quantum sensing or computation?

CONFLICTS OF INTEREST

There are no conflicts to declare.

ACKNOWLEDGEMENTS

The author would like to thank Aaron Fafarman and F. Scott Stinner for critical readings of the manuscript, Nuri Oh for pointing out the high performance of NC selenides and arsenides, and Tianshuo Zhao for help in preparing Table I. The author is grateful for support of this work from the NSF MRSEC under Award No. DMR-1720530.

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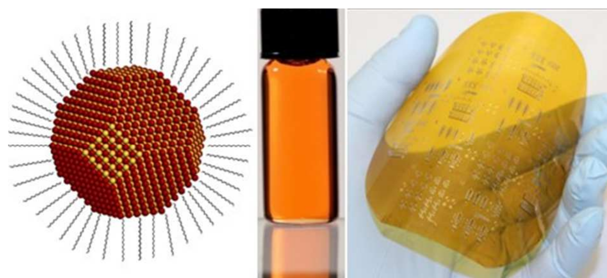
TOC Figure



Colloidal nanocrystals are dispersed in solvent forming "inks" for the solution-based fabrication of flexible nanocrystal electronics.

Photograph and Biography

Cherie R. Kagan is the Stephen J. Angello Professor of Electrical and Systems Engineering, Materials Science and Engineering, and Chemistry at the University of Pennsylvania. She graduated from the University of Pennsylvania with a BSE in Materials Science and Engineering and a BA Mathematics (1991) and from the Massachusetts Institute of Technology with a PhD in Materials Science and Engineering (1996). In 1996, she went to Bell Labs as a postdoctoral fellow and in 1998, she joined IBM's T. J. Watson Research Center. The Kagan group studies the chemical and physical properties of nanostructured materials and their electronic, optoelectronic, optical, and sensing devices. Dr. Kagan is an Associate Editor at ACS Nano.