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ARTICLE

High-density polyethylene — an inert additive with stabilizing effects on organic field-effect transistors

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Organic electronics technologies have attracted considerable interest over the last decades and have become promising alternatives to conventional, inorganic platforms for specific applications. To fully exploit the touted potential of plastic electronics, however, other prerequisites than only electronic functions need to be fulfiled, including good mechanical stability, ease of processing and high device reliability. A possible method to overcome these issues is the employment of insulating:semiconducting polymers blends, which have been demonstrated to display favourable rheological and mechanical properties, generally provided by the insulating component, without negatively affecting the optoelectronic performance of the semiconductor. Here, we demonstrate that binary blends comprising the semicrystalline high-density polyethylene (HDPE) in combination with hole- and electron-transporting organic semiconductors allow fabrication of *p*-type and *n*-type thin-film transistors of notably improved device stability and, in some scenarios, improved device performance. We observe, for example, considerably lower subthreshold slopes and drastically reduced bias-stress effects in devices fabricated with a hole-transporting diketopyrrolopyrrole polymer derivative when blended with HDPE and significantly enhanced charge-carrier mobilities and shelf life in case of transistors made with blends between HDPE and the electron-transporting poly{[N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)2,6-diyl]-alt-5,5'-(2,2'-bithiophene)}, *i.e.* P(NDI2OD-T2), also known as N2200, compared to the neat material, highlighting the broad, versatile benefits blending semiconducting species with a semicrystalline commodity polymer can have.

Introduction

The employment of organic materials in the electronic industry has been historically limited to packaging-, sealing- and adhesive applications owing to their good insulating nature, their mechanical robustness and, in many cases, their low costs. This classical usage of organics has, though, recently been disrupted by the emergence of organic semiconductors leading to a wide range of electronic devices that have been fabricated and reported both in literature and by industry.[1–4]

Organic semiconductors are a relatively large family of materials. This is because of their broad chemical diversity and straight-forward chemical tunability, covering both small molecules and polymers, allowing a nearly unimaginably large number of different materials to be synthesized. While small molecule semiconductors often exhibit excellent charge transport properties, polymers are typically preferred for many applications owing to the ease with which they usually can be processed.[5] Indeed, one of the key reasons that renders many organics attractive for electronic applications is their solution processability, which enables printing of electronic devices with relatively low-tech methodologies at fast rates and, in some cases, over large areas.

Within the large variety of applications, organic thin-film transistors (OTFTs) have become a key device platform for organic semiconductors because they often serve as basic building blocks for printed, flexible, small and large-area circuits, difficult to realize with traditional inorganic semiconductors and wafer-based manufacturing methods.[6] Moreover, the tremendous improvement of charge carrier mobilities that has been realized over the last decade when using organic semiconductors has broadened the spectrum of OTFT applications, from low-frequency operating devices towards fast switching logic circuits.[7,8]

However, in addition to high charge mobilities, other device parameters are of critical importance for many electronic applications, including: low operation voltage, low "OFF"-currents and low gate leakage—all required to reduce the power consumption—as well as a low, stable threshold voltage, important for reliable device function.[9–11] Other characteristics

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that are important to be fulfilled are: good processability and mechanical robustness of the active layer.[12] While in principle semiconducting polymers could exhibit good mechanical properties, in most cases they display a rather small elongation at break; *i.e.* they often are brittle, in strong contrast to most semicrystalline commodity plastics.[13]

The poor mechanical features of many polymer semiconductors are related to their generally low molecular weight. As a consequence, when they are processed from solution, often at highly diluted concentrations, the systems are below the critical overlap concentration (that is: the polymer chains are not entangled),[14] limiting, if not fully preventing, the resulting thin-film structures to be mechanically tough. In addition, the low molecular weight and, hence, the low entanglement density per chain, leads to a low viscosity (few mPa·s),[14] which can cause issues when depositing the material, especially when larger areas need to be covered and the surface wettability is poor.[14,15]

A possible route to overcome these limitations is the addition of insulating commodity plastics to the organic semiconductor to form blends.[16,17] Indeed, semicrystalline commodity plastics typically are mechanically robust, showing high elongations at break, and featuring a wide range of viscoelastic properties. They also are often available in large varieties (*e.g.*, different densities) and at low costs.[18] Blending semiconducting and insulating components at different ratios, thus, allows to tune the overall materials costs, the mechanical features of the resulting structures, as well as their solution viscosity and, therefore, their processability.[16]

Insulating polymers can grant other useful benefits to blends comprising semiconducting components. One of them is the encapsulating effect that they can execute via 'embedding' the semiconductor(s) essentially in a protective scaffold.[19–22] Thereby, selection of a suitable insulating polymer is critical. One crucial parameter is the degree of crystallinity. The crystalline quality and the degree of crystallinity influences many properties of polymers, including their viscoelastic characteristics, their thermal conductivity, as well as their optical and chemical responses. It also affects the materials' barrier properties to gases and vapours, with semicrystalline materials usually outperforming their amorphous counterparts.[23] Hence, semicrystalline insulators appear to be an obvious choice for blends targeted for achieving more stable electronic devices.

Various reports on insulating:semiconducting blends exist, however, most of them are based on the use of amorphous insulating polymers, *e.g.* atactic polystyrene (*a*-PS), a material with very poor barrier properties, and poly(methyl methacrylate) (PMMA).[16,17] Moreover, blending has rarely been applied to high-mobility polymers; and detailed electrical analysis are scarce. Here we show how the electrical performance, especially in the subthreshold region, of blends between the semicrystalline commodity plastic high-density polyethylene (HDPE) with high mobility hole- and electron-transporting materials is enhanced compared to devices prepared with the neat semiconductor. More specifically, blending leads to a drastic increase in performance and stability, combined with a notably smaller sensitivity to environmental factors.

We selected HDPE because it is a widely used bulk plastic, with excellent H_2O-barrier properties. Furthermore, HDPE has already been employed in multicomponent systems with the well-studied poly(3-hexylthiophene-2,5-diyl), P3HT, *e.g.*, for organic device fabrication (thin-film transistors, organic photovoltaic devices).[13,24–30] Thereby, specific processing conditions needed to be followed to lead to functioning devices. We, thus, also elucidated the crystallization during thin-film fabrication by studying the blend microstructure development upon solution coating *in-situ* using grazing-incidence wide-angle X-ray scattering (GIWAXS).

Experimental

Materials

High-density polyethylene, HDPE, (M_w = 125 kg/mol, density = 0.95 g/mL at 25 °C), poly(methyl methacrylate), PMMA, ($M_w \approx$ 120 kg/mol), octadecyltrichlorosilane (OTS) and all the solvents were purchased from Sigma Aldrich and used as received. P(NDI2OD-T2), also known as N2200 (M_n = 35.3 kg/mol; Đ ≈ 1.8 (GPC)) was purchased from Flexterra Corporation, DPP-TT-T (number-average molecular weight: M_n = 24 kg/mol; dispersity Đ ≈ 3.7), synthesized using previously reported procedures.[31] P3HT (weight-average molecular weight: $M_w \approx$ 115 kg/mol; Đ ≈ 1.5; regioregularity, RR = 99%) was synthesized using previously reported procedures.[32]

Samples and Device Fabrication

Materials were first weighed with a balance (Mettler Toledo XS205), then transferred in a vial and, after adding the appropriate solvent they were stirred on a hot plate till complete dissolution. DPP-TT-T (10 mg/mL in chlorobenzene) and N2200 (10 mg/mL 1,2-dichlorobenzene) solutions were mixed with HDPE solutions prepared with the same solvent and at the same concentration as the neat materials. Blend solutions were stirred at 120 ˚C to assure full dissolution of polyethylene, prior to deposition with a wire-bar coater. The latter was kept at a temperature of 100 ˚C (both the coating bed and the wire bar), while the coating speed was selected to be in the range between 20 to 30 mm/s. Bottom-gate/bottom-contact testbeds from Fraunhofer institute were used in order to fabricate *p*-type OTFTs. A thermally grown silicon oxide (90 - 230 nm thick) served as dielectric, while a heavily doped silicon substrate was used as the bottom gate electrode. Interdigitated source-drain electrodes were made in gold with a channel width of 1 cm and a range of channel lengths of 2.5, 5, 10, and 20 µm. Substrates were cleaned by sonication in acetone and isopropanol followed by a 20 minutes UV-ozone treatment. Subsequently, testbeds were soaked in a solution of 20 µl octadecyltrichlorosilane (OTS) in 5 mL toluene followed by sequential rinsing in pure toluene, hexane, and isopropanol. Films coated in air were immediately transferred to a glovebox or vacuum chamber for storage and testing. Top-gate/bottom-contact OTFTs were fabricated employing low alkali 1737F Corning glasses as substrates. After cleaning them in an ultrasonic bath of

acetone and isopropyl alcohol, they were exposed to O_2 plasma at 100 W for 5 min. Bottom electrodes were defined by a photolithographic lift-off process and deposited by thermal evaporation of 25 nm-thick Au with a 1.5 nm-thick Cr adhesion layer. The channel width was 2 mm and a range of channel lengths of 2.5, 5, 10, and 20 µm was used. Patterned substrates were cleaned in a ultrasonic bath with isopropyl alcohol before the active layer deposition. Finally, a PMMA layer was spin coated at 1300 rpm for 60 s, leading to a dielectric thickness of 550-600 nm, before thermal evaporation of Al through shadow mask to define the gate electrode. The devices were then transferred into a N_2 filled glovebox and annealed at 100 ˚C for one hour before electrical measurements were performed.

Thin-film characterization

A Perkin Elmer Lambda 25 spectrophotometer was employed for UV-vis absorption spectroscopy measurements. Grazing incidence wide-angle X-ray scattering (GIWAXS) was carried out at the D-line, Cornell High Energy Synchrotron Source (CHESS) at Cornell University. A wide band-pass (1.47%) X-ray beam with a wavelength of 1.155 Å was employed with a sample-to-detector distance of 17.3756 cm; the incidence angles were ranging between 0.15˚ and 0.25˚. A 2-D Pilatus 200k detector with a pixel size of 172 µm and a beam stopper (1.5 mm wide tantalum rod) was used to block the X-ray at small angles. Films analysed *in-situ* were cast with a homemade blade coater mounted within the experimental set-up on a temperature-controlled stage, as explained in Ref. 33. An Ion TOF 5 SIMS was used to measure depth profiles of blend samples. All samples were sputtered using a 1 keV Cs^+ (~75 nA) beam across a 250 × 250 µm square. Analysis was carried out using a Bi_3^+ (~1 pA) beam over the central 50 × 50 µm region of the sputter crater with charge compensation and negative ions were collected. SIMS measurements were carried out directly on OTFT active layers, which had been delaminated from the transistor and re-deposited onto a bare silicon substrate. The delamination was performed by first depositing a viscous solution of PVA:PVP (1:1) (24 wt% in water) onto the active layer. After complete evaporation of the solvent, the resulting bilayer was peeled off from the substrate. The strong adhesion of the active layer with the PVA:PVP film allowed a complete removal of the entire bilayer from the substrate. This self-standing film was then flipped and placed in water with the PVA:PVP layer face down. After complete dissolution of the PVA:PVP, a Si substrate was used to collect the active layer so that the top surface of the produced sample corresponded to the original bottom surface of the active layer that had been in contact with OTS/SiO_2.

[Note: Certain commercial equipment, instruments, or materials are identified in this paper in order to adequately specify the experimental procedure. Such identification is not intended to imply recommendation or endorsement by the National Institute of Standards and Technology, nor is it intended to imply that the materials or equipment identified are necessarily the best available for the purpose.]

Results and discussion

To illustrate the general benefit of blending with HDPE, we chose state-of-the-art semiconducting polymers. We started with a diketopyrrolopyrrole (DPP) low-bandgap donor-acceptor copolymer, that is DPP-TT-T (generally, a hole-transporting material), and poly{[N,N'-bis(2-octyldodecyl)-naphthalene-1,4,5,8-bis(dicarboximide)2,6-diyl]-alt-5,5'-(2,2'-bithiophene)}, P(NDI2OD-T2), also known as N2200 and an electron-transporting polymer. Their chemical structures are shown in Figure 1 (insets). The DPP-based polymers are some of the most prominent high hole-mobility materials reported in literature thanks to their backbone planarity,[34] while N2200 has so far been the reference electron-transporting polymer having resulted in the realization of high-mobility *n*-type OTFTs.[35,36]

In a first set of experiments, thin-film transistors were fabricated with 1:1 (by weight) semiconductor:insulator blends using wire-bar coating for film deposition. A bottom-gate/bottom-contact

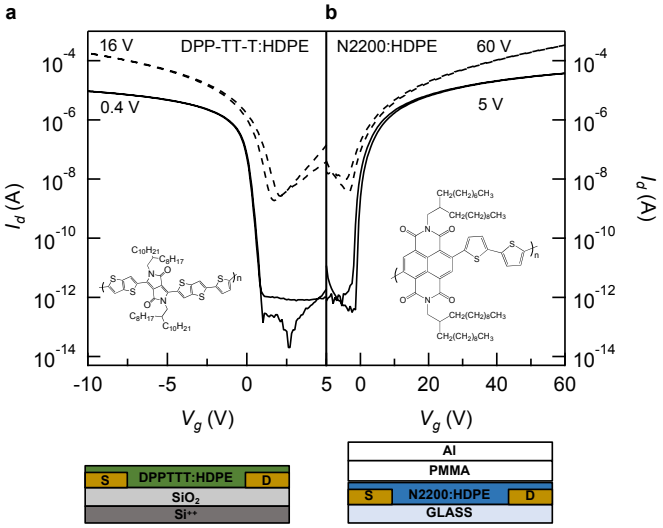

Figure 1: Representative transfer characteristics of a) 1:1 DPP-TT-T:HDPE and b) 1:1 N2200:HDPE OTFTs. The chemical structures of the two polymers are shown in the insets; source-drain voltages used are indicated in the graphs. In addition the device architectures utilized are given: bottom-gate/bottom-contact devices with a SiO_2 dielectric (thickness = 90 nm) were used for DPP-TT-T and its blends with HDPE; top-gate/bottom-contact with a PMMA dielectric (thickness = 600 nm) were employed for N2200 and N2200:HDPE devices.

configuration was selected for the DPP-TT-T:HDPE blends, while a top-gate/bottom-contact geometry was chosen for the N2200:HDPE binaries to optimize device performance. The corresponding transfer characteristics are shown in Figure 1a and b, respectively; the output characteristics are displayed in Figure S1.

Both, the *p*-type and the *n*-type devices display well-behaved transfer characteristics in the linear regime, with steep turn-"ONs", indicative of a low trap density at the critical semiconductor/gate dielectric interface, and high ratios between the "ON"- and "OFF" currents (I_{on}/I_{off}) of 10^7, which we attribute to high device mobilities and excellent charge depletion prior to charge accumulation. At high lateral fields, ambipolar transport is observed in the transfer characteristics for both materials, in agreement with literature.[37,38] Moreover, the output

characteristics (Figure S1) show a clean, linear dependency of drain current (I_d) with gate voltage at low source-drain voltages (V_d). From this, we infer good ohmic charge injection despite the presence of a relatively large amount of insulator in the active layer.

From the above observations it is evident that the addition of HDPE to DPP-TT-T is not negatively affecting the device operation; indeed, blending leads to an improvement of the subthreshold region, reducing V_{th} and I_{off}, while the charge-carrier mobility is essentially unaffected. Similarly, N2200:HDPE blends show enhancements in the device function. The electron mobility in the saturation regime (μ_{sat}) in blends exceeds 2 cm²/Vs in our best device, while OTFTs fabricated with neat N2200 exhibit a μ_{sat} = 0.9 cm²/Vs.

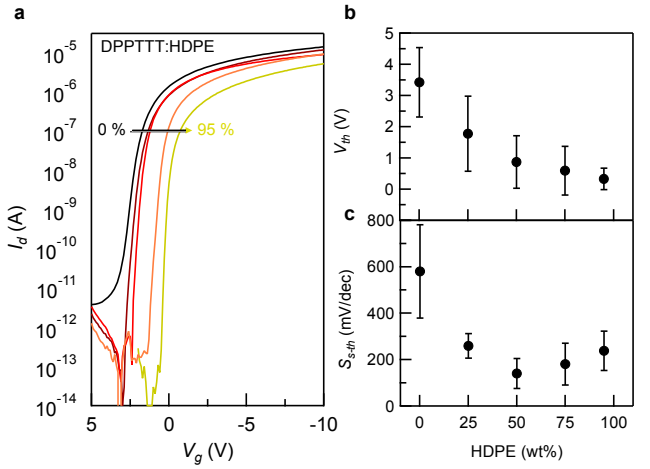

Figure 2: a) Representative transfer characteristics of DPP-TT-T:HDPE blends as a function of HDPE content ranging from 0 wt%, 25 wt%, 50 wt%, 75 wt% to 95 wt%, indicated with a colour gradient and an arrow. Only forward traces at V_d = -0.4 V are shown for clarity. (b) Corresponding threshold voltage (V_{th}) extracted in saturation regime and (c) subthreshold slope, $S_{s\text{-}th}$ as a function of HDPE content. The error bars indicate the standard deviation.

Having established that blending allows fabrication of high-performing transistors with materials such as DPP-TT-T and N2200, we went on to elucidate in more detail how addition of HDPE influences OTFT characteristics. For this, we prepared blends where we systematically increased the HDPE weight fraction to up to 95 wt% focusing on DPP-TT-T-based devices (Figure 2). A few observations can be made. The charge carrier mobility is essentially unaltered upon increasing the HDPE content (Figure S2). Moreover, and beneficially, the threshold voltage shows a monotonic shift towards zero voltage with increasing insulator content, with devices made with blends comprising ≥50 wt% HDPE displaying $V_{th} \approx 0$ V (Figure 2a,b). At low source-drain voltages, the reduction of V_{th} is accompanied by the complete disappearance of the hysteresis between forward and backwards gate-bias sweeps that is observed in neat semiconductor devices; although, it is relatively modest also for these devices (See Figure S3-5). At higher source-drain voltages, a slight hysteresis is present also in OTFTs fabricated with blends, likely as a consequence of an unbalanced ambipolar charge transport that can result from, among other things, limited electron injection and trapping.

Another change in device operation when using blends is observed in the "OFF" state of the device. More specifically, the "OFF" current, defined as the current measured at positive V_g before the onset of any field effect, is considerably reduced in the linear regime (reverse sweep) compared to devices made with neat DPP-TT-T. For instance, an I_{off} below 10^{-12} A is observed for blend devices produced with active layers of a thickness of ≈50 nm, while the neat DPP-TT-T shows $I_{off} = 2 \times 10^{-10}$.

The shift of V_{th} towards 0 V and the decrease of I_{off} contributes to the subthreshold slope, $S_{s\text{-}th}$, to become notably steeper, from ≈600 mV/dec for the neat semiconductor, to ≈200 mV/dec for blend layers comprising 95 wt% HDPE. This means that the 'blend' devices turn-"ON" faster (Figure 2c). As alluded to already above, this suggests that blending leads to a narrowing of the density of states and decreases the trap density (N_T) at the active layer/gate dielectric interface.[39] The latter can be estimated utilizing the following equation:

$$N_T \approx \left(\frac{S_{s-th} q \log(e)}{K_b T} - 1\right)\frac{C}{q} \qquad (1)$$

where q is the electron elementary charge, K_B is the Boltzmann constant, C is the dielectric capacitance, T is the absolute temperature. N_T shows a dramatic reduction in blend devices as summarized in Table 1.

Table 1: Estimated charge trap densities (N_T) in DPP-TT-T:HDPE blends as a function of HDPE content.

	HDPE content (wt%)				
	0	**25**	**50**	**75**	**95**
N_T ($eV^{-1} \cdot cm^{-2} \cdot 10^{12}$)	2.1	0.8	0.3	0.5	0.7

The achieved decrease in N_T is technological relevant since it leads to a reduction of the required transistor operation voltage. For instance, using a source-to-drain voltage of -50 mV to drive devices prepared with 1:1 DPP-TT-T:HDPE blends, a V_g sweep of 2 V is sufficient to modulate the current from 10^{-12} A in the "OFF" state to 10^{-6} A in the "ON" state, while the devices fabricated with the neat semiconductor can only be modulated from 10^{-10} A in the "OFF" state to 10^{-6} in the "ON" state with a V_g sweep of 3 V (Figure S6). We assign this beneficial effect to the "dilution" of the semiconductor upon addition of the insulator; that is, the insulator is taking up volume within the active layer, reducing parasitic bulk-current effects. Such a "dilution" leads to a decreased trap density and, hence, to the observed, improved device characteristics. [Note: some unintentional doping of the bulk of the semiconductor by oxygen molecules may contribute to the bulk current as well].

We like to highlight that comparable observations were made with devices fabricated with N2200:HDPE blends: the I_{off} decreases from 10^{-11} for the neat semiconductor to below 10^{-12} in 1:1 blend devices. However, in contrast to the *p*-type devices, only a minor effect of blending is observed on threshold voltage and subthreshold slope for these systems, probably owing to the already steep turn-"ON" of neat N2200 devices. It is also possible that some changes in device characteristics are hidden

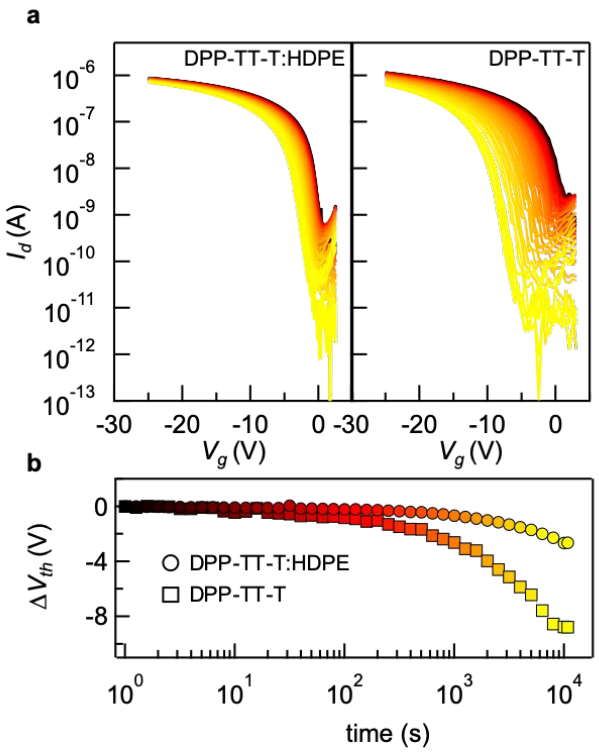

Figure 3: a) Transfer curves of OTFTs made of neat DPP-TT-T and 1:1 DPP-TT-T:HDPE blends measured at a constant bias stress of -20 V, in glovebox. b) Corresponding threshold voltage shift (ΔV_{th}). Squares: data for neat DPP-TT-T; circles: data for the 1:1 blend. The source-drain voltage was -1 V, the dielectric thickness 230 nm. The colour gradient from black, to red and yellow indicates the evolution of stress over time, which is performed for a total of 10000 s.

beneath other device non-idealities. For example, high-performing N2200 devices typically show a non-negligible V_g dependence of the device mobility, as reported in literature.[40,41] This renders extraction of fit parameters (*e.g.*, V_{th}) more challenging than for, *e.g.*, the DPP-TT-T-based devices (Figure S7).

Blending has an additional, positive effect on N2200 devices: it leads to a notable enhancement in charge-carrier mobilities, which we assign to an increase in charge-transport anisotropy. Indeed, we find that the device mobilities, measured in the saturated regime with channels positioned parallel and perpendicular to the wire-bar coating direction ($\mu_{sat,para}$ and $\mu_{sat,perp}$, respectively), result in a $\mu_{sat,para}/\mu_{sat,perp}$ ratio of 23 and an average mobility of $\mu_{sat,para}$ = 1.2 ± 0.5 cm^2/Vs, compared to $\mu_{sat,para}/\mu_{sat,perp} \approx 12$ and an average mobility of 0.5 ± 0.35 cm^2/Vs for neat N2200 devices. Evidently, addition of the high-molecular weight HDPE assists to achieve molecular orientation during wire-bar coating. This is in agreement with the fact that we observe an increased optical dichroic ratio (DR) for blends of 1.7, measured by polarized UV–vis absorption spectroscopy, while neat N2200 displays a DR = 1.2 (Figure S8). The spectral shape of N2200 appears to be unaffected by the introduction of HDPE. [NB. We define the DR as the ratio between the maximum absorption centred around 700 nm measured with the polarization parallel and perpendicular to the coating direction.]

The fact that addition of HDPE leads to some structural and, thus, electronic anisotropy may not be surprising. It has, for instance, been reported that neat N2200 forms fibrils during film formation, which can be oriented along the wire-coating direction. This structural anisotropy affects charge transport, resulting in an increase of electron mobility along the oriented fibrils as shown in Refs. 38,42 — an effect that seems to be enhanced by the addition of the HDPE.

Encouraged by our results and, especially, the steep subthreshold slopes and the close-to-zero-volt threshold voltages observed both in our *p*- and *n*-type blend devices, we proceeded to assess the bias-stress stability of DPP-TT-T:HDPE binaries. The bias-stress stability is related to the variation of transistor characteristics over time, under application of a constant gate voltage.[43] For this we compared the evolution of the transfer curves of DPP-TT-T devices fabricated with and without addition of HDPE, over time (Figure 3; gate dielectric thickness: 230 nm). We applied a constant gate bias of -20 V and measured devices in the glove-box in the dark. The devices were measured as prepared, without performing any further treatment. During stress, the bias was released only to measure the transfer curve, when a V_d = -1 V was applied. Intriguingly, while devices based on neat DPP-TT-T display a substantial threshold voltage shift in the direction of the applied bias, devices prepared with blends degrade significantly slower (Figure 3). More precisely, a threshold voltage shift of 2.5 V is recorded after 3 hours for 1:1 DPP-TT-T:HDPE blends. In strong contrast, neat devices exhibit a shift of close to 9 V at identical conditions/time periods. The field effect mobility, thereby, is essentially unaffected by the bias stress, with a slight decrease being observed at higher stressing times.

Note also that the degradation induced by the bias-stressing was completely reversible, with V_{th} returning to its initial value for all systems – blend or neat. This is in agreement with other studies that show that the threshold voltage in *p*-type devices can recover after the stress is removed.[44]

Different hypothesis have previously been advanced to explain the origin of threshold-voltage shifts induced by a constant bias at the gate electrode. It is generally accepted that immobile charges resulting from charge trapping at the semiconductor/gate dielectric interface are one reason for this specific device degradation.[44] The immobilization of charges was reported to result from a redox reaction, in which water plays a major role. As a result of this reaction, protons (H^+) are produced at the semiconductor/dielectric interface due to adsorbed water. These protons can migrate into the dielectric, forming immobilized charges.

Our results agree with such a picture. In devices made of neat DPP-TT-T, we observe a fast increase of the threshold voltage in the first stages of the bias stress where proton diffusion has been reported to be dominant (Figure 3b),[44] suggesting that in neat DPP-TT-T devices there is a relatively high concentration of H^+ protons at the interface with the gate dielectric (here: SiO_2). On the contrary, blend devices show a drastically slower development. We attribute this behaviour to the highly hydrophobic nature of HDPE, leading to a low permeation of water molecules. As a consequence, semiconducting:insulating

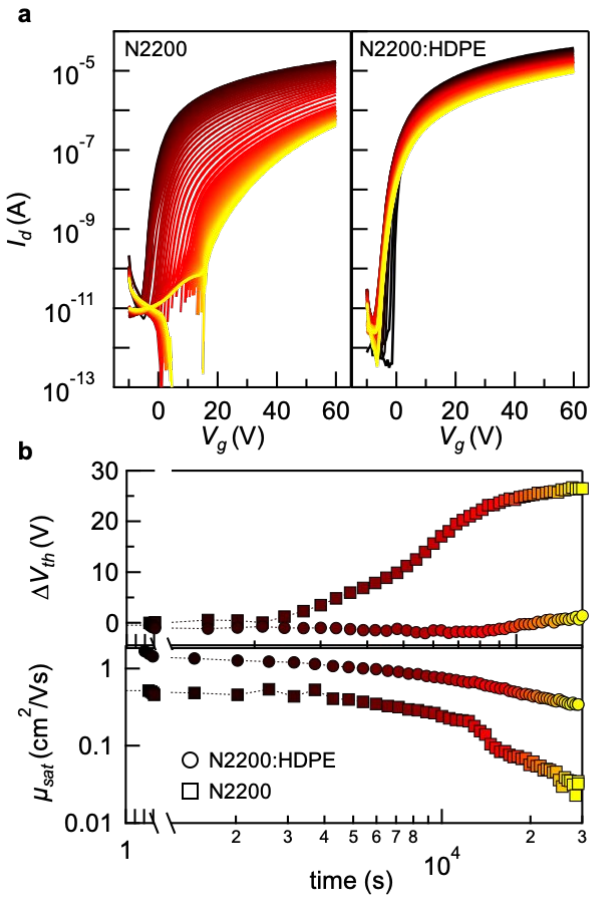

Figure 4: a) Transfer curves of OTFTs made with neat N2200 and 1:1 N2200:HDPE blends measured in air every 5 minutes for 8 hours. The linear characteristic is shown (V_d = 5 V). b) Corresponding threshold voltage shift (ΔV_{th}) and charge carrier mobility evolution. Squares: data for N2200; circles: data for the blend. The colour gradient from black, to red and yellow indicates the time evolution.

polymer blends with high content of polyethylene will have a decreased moisture permeability, leading to an 'encapsulation' effect that reduces the water content in the active layer. Proton diffusion and drift, which is thought to be responsible for the threshold voltage shift,[44] may, thus, be kinetically hindered, even though dynamically unaltered.

Having established that noticeable improvements in terms of bias stress can be achieved in *p*-type devices through a possible, water/humidity-repellent protection, we assessed the capability of HDPE to enhance the stability of N2200 blends. Since moisture and oxygen are known to be detrimental for *n*-type devices, often leading not only to a threshold voltage shift but also a significant reduction in device mobility,[36] we focused on the effect of blending on the shelf life of N2200 devices in air. For this, we measured devices every five minutes for 8 hours (Figure 4). OTFTs were prepared in ambient conditions and subsequently annealed in a glovebox at 100 ˚C in order to minimize the amount of water molecules absorbed within the different layers.

N2200 top-gate/bottom contact devices with a 600 nm PMMA gate dielectric show a rapid degradation of all principle device parameters (Figure 4a). A progressive deviation of the I_d-*vs.*-V_g characteristics from an ideal behaviour was observed as well. Distinctively, after around 60 minutes air exposure/device measurements, the V_{th} begins to notably shift towards positive values following a stretched exponential function; within 8 hours, V_{th} is shifted by +27 V (Figure 4b/top panel). The electron mobility also starts to considerably decrease after 60 minutes (Figure 4b/bottom panel), initially dropping logarithmically from 0.5 cm^2/Vs to 0.2 cm^2/Vs within roughly 3 hours, followed by an even steeper decrease that can be fitted with a double exponential and that leads to a reduction of mobility to a value of only 0.03 cm^2/Vs in 8 hours. In stark contrast, devices fabricated with 1:1 N2200:HDPE blends show a rather remarkable stability: the threshold voltage of the transistor only slightly changes over time. Moreover, only a moderate shift of the turn-on voltage (V_{on}), defined as the onset of the field-effect current in the transfer characteristic,[45] towards negative values is recorded.

Blending with HDPE does, however, not provide a full protection. Over time the sub-threshold slope $S_{s\text{-}th}$ becomes less steep. In addition, the electron mobility decreases logarithmically from the initial value of ≈1.5 cm^2/Vs to ≈0.35 cm^2/Vs in 8 hours, leading to a reduction of I_{on} over time. We like to emphasize that these effects are small compared to those observed for neat N2200 as the comparison of the development ofΔV_{th} and μ_{sat} shown in Figure 4b illustrates. Moreover, upon annealing the devices in glovebox at 100 ˚C for 1 hour, the blend devices almost entirely recovered their initial performance, while the initial device performance observed for transistors produced with neat N2200 was not fully recoverable (Figure S9).

This difference between neat and blend devices may be related to the mechanisms that lead to N2200 OTFT degradation, including electrochemical processes involving oxygen and water molecules. For instance, Di Pietro *et al.* reported how device instabilities occur as a consequence of the formation of oxygen-induced shallow traps in the bulk of the active film through an electrochemical reversible process.[46] Moreover, the same authors showed how water plays a role as well, with a mechanism associated to two different processes: an electron transfer process that has only a limited and reversible impact on the device, and a chemical degradation of the polymer film that is irreversible. Furthermore, while comparing the effect of oxygen and water individually, the latter was found to induce a faster degradation of the transistor, especially on the charge carrier mobility.

Considering that our devices were first annealed in order to reduce as much as possible the amount of water and oxygen molecules that may have penetrated into the active layer, we speculate that the enhanced stability displayed by blend devices is associated with a decreased permeation of water molecules in the bulk of the active layer, owing to the particularly low permeability (*P*) of H_2O in HDPE, P_{H_2O} = 1.2 – 2.5 $cm^2 \cdot mm \cdot 10^8/cm^2 \cdot s \cdot cm\,Hg$ (exact values depend on the density and crystallinity of the film).[23] Such a process may also explain why we observed some reversible reduction in electron mobility in N2200:HDPE devices — after all, HDPE is not the best oxygen barrier (P_{O_2} = 11 $cm^2 \cdot mm \cdot 10^{10}/cm^2 \cdot s \cdot cmHg$) compared to semicrystalline commodity polymers such as

poly(ethylene glycol terephthalate) (PET, P_{O_2} = 0.3 $cm^2 \cdot mm \cdot 10^{10}/cm^2 \cdot s \cdot cmHg$). Thus, a certain O_2 permeation across the dielectric and within the active layer occurs for both neat and blend devices. Nevertheless, the almost complete recovery of the transfer characteristics to its initial state indicates that H_2O diffusion within the blend film is almost completely hindered (in the timescale of our experiment), probably due to the slower kinetics of diffusion of this molecule, drastically increasing the shelf life of blend devices.

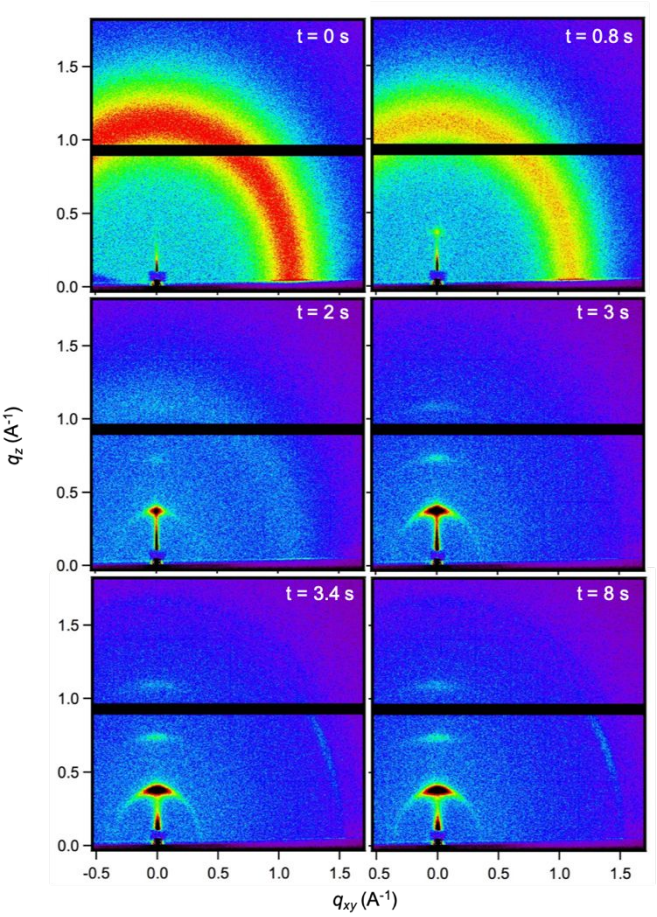

Figure 5: 2D-GIWAXS patterns of 1:1 P3HT:HDPE blends measured in-situ during film formation at 100 ˚C. Time evolution is shown in the top right corner; *t* = 0 s refers to the first acquisition after casting. P3HT reflections are developing during solvent evaporation (*t* = 0.8 s) with intensities increasing with time. Only when most of the solvent was evaporated did HDPE start to crystallize (*t* = 3.4 s). Solutions were prepared in decahydronaphthalene (*i.e.*, decalin) and the total polymer concentration was 10 mg/mL.

Like for other semiconductor:semicrystalline insulator blends, [26] to achieve such excellent devices performances with enhanced bias-stress- or shelf-life stability, selection of processing conditions is critical. The deposition temperature has to be chosen such that the semiconductor is forced to crystallize while the insulator is still in the liquid phase, solution or melt.[26,28,29] If these conditions are fulfilled, the semiconductor can crystallize relatively freely, *i.e.* in a scenario where diffusive transport is high. This is followed by crystallization of the insulator which assists producing percolation pathways of the semiconductors, as described by Goffri and co-workers on the example of the well-studied P3HT, blended with HDPE.[26] They concluded this from a phase diagram produced via superimposing plots of crystallization temperature of the two materials as a function of solvent concentration, which allows identifying the crystallization sequence during solvent evaporation for different scenarios.[26] For example, P3HT was revealed to crystallize prior to HDPE at elevated deposition temperatures above 80 ˚C, leading to excellent transistor performances, while below that temperature HDPE crystallizes first. This results in devices that

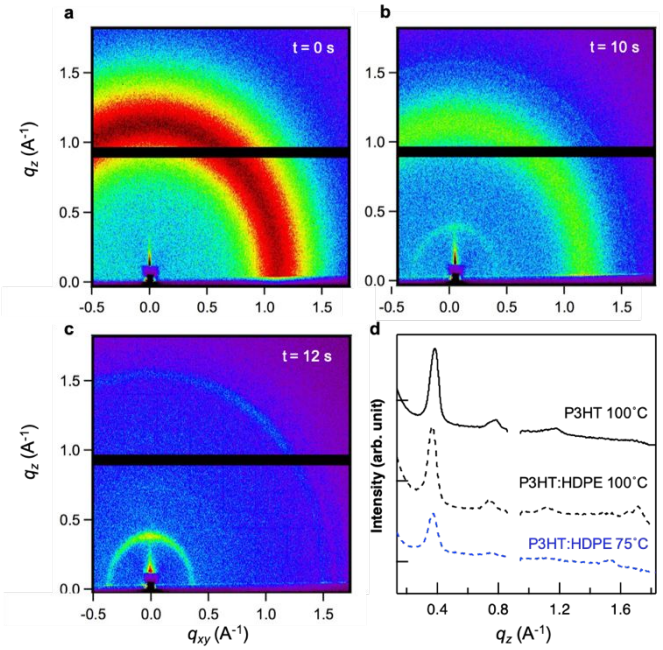

Figure 6: (a-c) Representative two-dimensional GIWAXS patterns of 1:1 P3HT:HDPE blends measured in-situ during film formation at 75 ˚C. Time evolution is shown in the top right corner; *t* = 0 s refers to the first acquisition after casting. P3HT and HDPE reflections are developing simultaneously during solvent evaporation (*t* = 10 s). The overall crystallization of P3HT is extremely restricted. (d) Out-of-plane scattering integration of P3HT (black solid line) cast at 105 ˚C; P3HT:HDPE cast at 105 ˚C (black dashed line); and P3HT:HDPE cast at 75 ˚C (blue dashed line). Solutions were prepared in decahydronaphthalene (decalin) and the total polymer concentration was 10 mg/mL.

are not functioning.[26]

Despite the extended literature on P3HT:HDPE blends, there are no studies providing experimental evidence of the crystallization process during thin-film formation beside thermal analysis data. We, thus, selected this well-studied binary as testbed to learn what insights can be gained on the microstructure development of thin films upon solution coating via *in-situ* grazing-incidence wide-angle X-ray scattering (GIWAXS) using synchrotron radiation.[33] To this end, 10 mg/mL solutions of P3HT:HDPE in decahydronaphthalene (also called decalin) were blade coated onto temperature-controlled substrates, while the crystallization was assessed with 2D-GIWAXS (Figure 5).

In a first set of experiments, the deposition temperature was set at 100 ˚C. The acquisition of GIWAXS data started as soon as the blade was moved onto the substrate, spreading the solution to form a liquid layer. Initially, a broad feature centred at $q \approx 1.1$ A^{-1} is visible in all the scattering directions. This amorphous halo

is produced by the two polymers, which are both fully dissolved at this stage. The solvent then begins to rapidly evaporate due to the relatively high deposition temperature selected. Crystallization of P3HT sets in within less than a second. We deduce this from the development of the characteristic [100] diffraction of P3HT, which we find predominately in the out-of-plane direction. In the following seconds the corresponding higher order diffractions —*i.e.*, the [200] and [300] diffractions— appear. This observation suggests that, at this stage, P3HT is fully crystallized, surrounded by polyethylene that is still in the liquid state. As the evaporation process advances, another diffraction at $q \approx 1.5$ A^{-1} appears and the evaporation of the solvent is complete. We associate this feature with the [110] diffraction of the polyethylene orthorhombic crystal phase.

Based on our GIWAXS data, we conclude that, unambiguously, in P3HT:HDPE blends cast from decalin at ≈ 100 ˚C, the semiconducting polymer crystallizes prior to the insulator as expected from the phase diagram. Since the insulator solidifies after the semiconductor, the latter's crystallization is essentially unhindered and both the orientation and crystallinity of P3HT are only minimally affected when compared with a sample of neat semiconductor cast at the same conditions.

In a second set of experiments, a deposition temperature of 75 ˚C was selected to test this crystallization scenario (Figure 6). A few initial observations can be made: at ≈ 75 ˚C, solvent evaporation is slower than in the first scenario using a casting temperature of 100 ˚C. This can be inferred from the fact that the amorphous halo observed during the initial stage of casting is dominating the X-ray pattern for a longer period of time. The crystallization of the two components is occurring essentially simultaneously with the [100] diffractions of P3HT and the [110] ones of HDPE developing after approximately 10 s. Most strikingly, the extent of crystallization of P3HT is considerably affected by the polyethylene crystallizing at the same time: only one order of the P3HT [h00] diffractions is observed and its intensity is notably reduced. From these findings, we deduce that at even lower deposition temperatures, HDPE would crystallize prior to the semiconducting component, hindering nearly entirely the crystallization of P3HT, as predicted by the phase diagram by Goffri *et al*. [Note: Use of deposition temperatures <75 ˚C led to rapid precipitation of polyethylene, which rendered *in-situ* experiments challenging.]

Since *in-situ*-GIWAXS can clearly identify crystallization sequences in semiconducting:semicrystalline insulator blends, we advanced to investigate the film formation of DPP-TT-T:HDPE blend films. We focused also on 1:1 systems, as for P3HT:HDPE, but cast the blends from 10 mg/mL solutions in chlorobenzene (CB) at a substrate temperature of 100 ˚C. The evaporation of the solution is more rapid compared to the P3HT:HDPE:decalin system, due to the lower boiling point of CB. Diffractions at $q \approx 0.36$ A^{-1}, characteristic for ordering of the semiconductor, appear within 1 second. The crystallization is completed within 1.8 seconds and occurs while HDPE is still dissolved/molten. Only after a few more seconds, signs of polyethylene crystallization are observed: the [110] diffractions of the orthorhombic crystal phase of HDPE develop, revealing *i*) that both components at least partly crystallize, and *ii*) that the

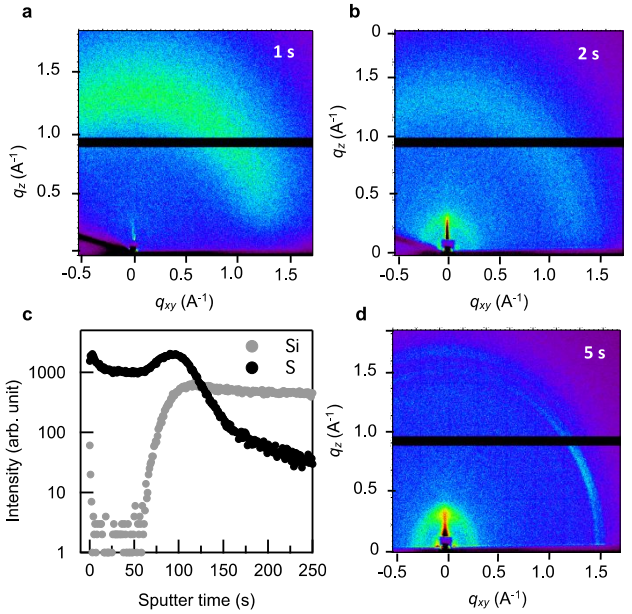

Figure 7: a, b, d) Integrated radial scattering as a function of time (indicated in the top right corner) extracted from 2D-GIWAXS of a 1:1 DPP-TT-T:HDPE blend collected in-situ during film formation. Deposition temperature ≈100 ˚C. Initially (1 s), scattering due to the solution only is visible (a). After 2 s, DPPTTT crystallizes and a certain amount of solution containing mainly HDPE is present (b). Finally, after 5 s HDPE crystallizes and the solvent is evaporated (d). c) D-SIMS profiles of sulphur (S; blue line) and Si (grey line) of 1:1 DPP-TT-T:HDPE blends (a). An accumulation of the semiconducting polymer is present at both interphases.

insulator crystallizes after the semiconductor as found for P3HT:HDPE blends at comparable conditions.

A similar behaviour is recorded for blends comprising an HDPE content ranging from 0 to 99 wt%. Thereby, the semiconductor diffractions intensities decrease with insulator content and those related to HDPE become more intense, as expected. Intriguing is that even at high contents of polyethylene, such as 99 wt% HDPE, the DPP-TT-T diffractions are still clearly visible, implying that even high HDPE fractions do not hinder the semiconductor's ordering because of the favourable crystallization sequence we selected (Figure S10).

It is important to emphasize that the crystallization of the HDPE leads to a *partial* vertical composition gradient in the blends films, albeit in much less notable fashion compared to systems using amorphous insulators.[19,21,47–49] We conclude this from time-of flight secondary ion mass spectroscopy (ToF-SIMS) measurements focusing on 1:1 DPP-TT-T (Figure 7c), carried out directly on OTFT active layers, delaminated from the transistor substrate and re-deposited onto bare silicon to limit artefacts introduced by the employment of a different substrate. We find that the film is enriched with the semiconductor both at the bottom interface with the SiO_2/OTS dielectric and at the top interface with air. Critically, a strong signal related to sulphur (S) is also found throughout the entire film, suggesting that an interpenetrating DPP-TT-T network within HDPE is formed throughout the film. This is important as this type of *partial* vertical phase separation can be used for a broad range of active layers in a wide variety of devices, including other transistor geometries such as top-gate bottom-contact devices, solar cells and light emitting diodes.

From our structural analysis, the beneficial effect of HDPE, including enhanced transistor performances and a notably increased device stability, can be attributed to the facts that (*i*) HDPE is taking up volume that is occupied by semiconducting material in neat films, indeed, slightly depleting the bulk of the active layer of the semiconductor, reducing undesirable bulk charge transport; (*ii*) the relatively minor, but notable vertical phase separation of the semiconductor to both interfaces, assists in creating charge-transport pathways at critical interfaces; and (*iii*) the beneficial effect that the pronounced hydrophobicity of HDPE has on stabilizing the transistor performance of blends compared to the neat materials.

Conclusions

In this work, we illustrated the versatility of blending organic semiconductors with insulating, semicrystalline polymers. This requires that the blends are solidified such that the semiconductor crystallize prior to the insulating matrix. In this scenario, addition of HDPE, even in large quantities, does not negatively affect OTFT device performance. On the contrary, blend devices display enhanced electrical properties, with drastically reduced bulk currents, leading to low I_{off} and, hence, high "ON"/"OFF" ratios. The threshold voltage is stabilized at ≈0 V, in DPP-TT-T based devices, and the turn-"ON" becomes significantly faster; *i.e.*, the sub-threshold slope $S_{s\text{-}th}$ becomes notably steeper. We attribute this observation to a smaller number of trap states at the semiconductor/dielectric interface and a narrowed density of states. Moreover, blending is found to improve electron mobilities in N2200 devices. The reason is that HDPE seems to enable an increased molecular orientation when wire-bar coating the active layer, leading to a higher transport anisotropy compared to the one found in neat N2200 films.

The stability of our OTFTs is also improved, both in presence of bias stress and in ambient conditions. We speculate that this enhancement is associated to an encapsulation action of HDPE, owing to the good barrier properties of this material to water. Indeed, the reduced threshold-voltage shift observed in bias-stressed DPP-TT-T:HDPE devices, together with the increased environmental stability and reversibility of the degradation in N2200:HDPE transistors supports the view that the concentration of water molecules in the active layer is minimized. Clearly, blending provides a versatile and widely applicable tool to organic transistor fabrication, delivering a possible solution towards the realization of high-efficiency and stable devices.

Conflicts of interest

There are no conflicts to declare

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