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Reconfigurable artificial synapses with an organic antiambipolar transistor for brain-inspired computing†

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Neuromorphic computing, a nonvon Neumann architecture, holds promise for low-power, high-efficiency data processing. Herein, we demonstrated reconfigurable artificial synapses using a floating-gate-type organic antiambipolar transistor (FG-OAAT) to mimic biological synapses. The FG-OAAT exhibited a Λ-shaped transfer curve with negative differential transconductance. A two-dimensional continuous Au film was used as the floating gate to induce a large peak voltage shift in the Λ-shaped transfer curve by controlling hole- and electron-trapping processes in the floating gate. This feature enabled reconfigurable synaptic operations. Long-term potentiation/depression, excitatory/inhibitory, and paired-pulse facilitation/depression functions were electrically reconfigured by tuning the charge conditions in the floating gate. These versatile synaptic operations were induced by a consistent pre-synaptic signal, with fixed polarity, applied voltage, and pulse width. These behaviors closely resembled those of biological synapses, highlighting the potential for a brain-like computing architecture that surpasses current von Neumann systems.

1. Introduction

The development of high-performance artificial intelligence (AI) is crucial for the upcoming Internet of Everything society owing to the rapid increase in data volumes from versatile information and communication systems including automobile systems, healthcare sensors, and industrial robots.[1–6] However, current AI systems based on the von Neumann architecture exhibit high power consumption.[7,8] For instance, the power consumption of supercomputer "K" reaches 10 MW.[9] This issue arises from the increased access frequency between logic and memory units, known as the von Neumann bottleneck. Therefore, the evolution of energy-efficient AI systems is an essential challenge in the big data era.

Neuromorphic computing systems, a type of non von Neumann architecture, offer a solution for energy-efficient AI.[10–12] These systems mimic the brain, which operates with ultralow power consumption (20 W) through parallel data processing.[13] Neuromorphic devices integrate logic and memory units, with nonvolatile memories such as magnetic random-access memory and ferroelectric memory widely used.[14–17] This device configuration enables extremely low-power consumption and high-speed parallel data processing. In addition, the adoption of pulse-based analog operations, such as spiking neural networks, is expected to drive the evolution of highly energy-efficient AI systems.[18–20]

Organic transistors with nonvolatile memories are widely employed in neuromorphic applications because of their attractive features, including light weight, flexibility, and biocompatibility.[21–24] The recognition of complex images and voice patterns has already been demonstrated.[25,26] However, conventional organic transistors usually support only synaptic operations for an input signal because they exhibit unipolar carrier transport.[21–24] Meanwhile, biological synapses exhibit diverse responses to identical input signals, with synaptic operations reconfigured by neuromodulatory commands.[27–30] Accordingly, the development of reconfigurable artificial synapses is a key challenge in the construction of brain-inspired AI systems. To address this, we demonstrate reconfigurable neuromorphic operations based on a floating-gate-type organic antiambipolar transistor (FG-OAAT).

An OAAT is a heterojunction transistor with at least one p–n junction in the transistor channel, which induces negative differential transconductance and produces a Λ-shaped transfer curve.[31–37] The drain current increases and then decreases

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with increasing gate voltage. This unique carrier transport in OAATs has enabled the creation of logic circuits, including ternary and quaternary inverters, ternary logic-in-memory, and reconfigurable two-input logic circuits.[38–43]

Herein, we applied OAATs to a reconfigurable artificial synapse, using 2,7-dioctyl[1]benzothieno[3,2-*b*][1]benzothiophene (C8-BTBT) and PhC_2H_4-benzo[*de*]isoquinolino[1,8-*gh*]quinolone diimide (PhC_2-BQQDI) films as the p-type and n-type transistor channels, respectively. Notably, a Au film was introduced as the floating gate (FG) to induce a large peak voltage shift in the Λ-shaped transfer curve by controlling the hole- and electron-trapping processes in the FG. This feature enabled unique synaptic operations, with long-term potentiation (LTP)/depression (LTD), excitatory/inhibitory, and paired-pulse facilitation (PPF)/depression (PPD) electrically reconfigured by adjusting the charge conditions of the Au FG. These findings suggest the potential to realize a new computing architecture beyond the current von Neumann computing.

2. Experimental methods

2.1. Formation of FG-OAATs

FG-OAATs with C8-BTBT and PhC_2-BQQDI were fabricated on a highly doped p-type Si(100) substrate (< 0.01 Ω cm) with a 200 nm-thick SiO_2 layer. First, a Au (30 nm)/Cr (5 nm) electrode was deposited as a back gate (BG) on the SiO_2/Si substrate *via* thermal vacuum deposition. Subsequently, a HfO_2 film (35 nm) was prepared as the gate insulating layer using atomic layer deposition (ALD) (SUGA Co. Ltd., SAL 1000), with the substrate temperature set at 175 °C. Here, tetrakis(dimethylamino)hafnium and water were used as the hafnium and oxygen sources, respectively. Afterward, an Au (10 nm)/Cr (5 nm) film was thermally grown on the HfO_2 layer as the FG, with a deposition rate of 5 Å s^{-1} to ensure a smooth surface morphology of the Au thin film. Then, a 10 nm-thick HfO_2 tunneling layer was formed *via* ALD, following the same process as the gate insulating layer. To passivate carrier trap sites on the HfO_2 surface, a 10 nm-thick polystyrene (PS) (Sigma-Aldrich, 182427, average molecular weight: 280 000) layer was spin-coated on the HfO_2 surface. Subsequently, C8-BTBT (13 ± 3 nm) and PhC_2-BQQDI (8 ± 2 nm) films were grown as p- and n-type organic channels, respectively, *via* thermal vacuum deposition at a background pressure of 10^{-7} Pa. Finally, 30 nm-thick Au films were deposited for the source (S) and drain (D) electrodes *via* thermal vacuum deposition, with typical width and length dimensions of 400 and 200 μm, respectively.

2.2 Transistor measurement

Transistor measurements of the FG-OAATs and neuromorphic operations were performed using a source measure unit (Keysight Technology, B2912B) under atmospheric conditions. All the measurements were conducted with a four-probe system at room temperature.

3. Results and discussion

Fig. 1a and b show the device structure and optical microscope image of the FG-OAAT. The transistor features a BG-type structure, with 14 nm-thick C8-BTBT and 8 nm-thick PhC_2-BQQDI films as the p- and n-type transistor channels, respectively. The detailed optimization processes of FG-OAATs are described in ESI† (Fig. S1–S5). Fig. 1c and d exhibit a typical drain current (I_D)–BG voltage (V_{BG}) curve and the differential transconductance (dI_D/dV_{BG}) curve for the n-type operation of the FG-OAAT, with the D voltage (V_D) fixed at 3.0 V. The transistor exhibited a Λ-shaped transfer curve (Fig. 1c), with no hysteresis appearing in the forward and reverse V_{BG} sweeps (black and red solid lines, respectively, in Fig. 1c), indicating no carrier trapping in the Au FG within the applied voltage range. I_D started to increase at V_{BG} (V_{on}) = 0.2 V, reaching 126 nA at V_{BG} (V_{peak}) = 1.8 V. Thereafter, I_D was completely suppressed at V_{BG} (V_{off}) = 2.6 V in the forward V_{BG} sweep from 0 to 3.0 V (black solid line in Fig. 1c). A distinct negative differential transconductance was observed between 1.9 and 2.6 V in the forward V_{BG} sweep of up to 3.0 V (Fig. 1d). Additionally, it is noteworthy that the low voltage operation of below 3.0 V was another essential achievement, which is induced by the employment of HfO_2 layer as the gate insulating layer. Usually, operation voltages of more than 5.0 V are required for OAATs.[31–38]

In our previous study, the Λ-shaped transfer curves in OAATs were interpreted analogously to the shoot-through current in complementary metal-oxide-semiconductor inverters. Namely, I_D of FG-OAATs is the overlapped current of the constituent n-type and p-type transistors described using the following equations:[44–47]

$$I_{D,n} = \frac{W}{2L_n}\mu_n C_i \left(V_{BG} - V_{th,n}\right)^2 \quad \left(V_{BG} \le V_{peak}\right) \tag{1}$$

$$I_{D,p} = \frac{W}{2L_p}\mu_p C_i \left(V_D - V_{BG} + V_{th,p}\right)^2 \quad \left(V_{BG} > V_{peak}\right) \tag{2}$$

where L_n and L_p are the channel lengths of the PhC_2-BQQDI and C8-BTBT channels, respectively, W is the common channel width, and C_i is the capacitance of the gate insulator per unit area. Additionally, μ_n and $V_{th,n}$ are the electron mobility and threshold voltage of the PhC_2-BQQDI transistor, respectively. Similarly, μ_p and $V_{th,p}$ represent the hole mobility and the threshold voltage of the C8-BTBT transistor, respectively. Accordingly, V_{on} and V_{off} in Fig. 1c correspond to the threshold voltages of the PhC_2-BQQDI and C8-BTBT transistors, respectively, while V_{peak} is the value of V_{BG} at the intersection of the transfer curves of both transistors.

Based on the above argument, the carrier transport process in FG-OAATs can be explained using the illustrations shown in Fig. 1e and f. In $V_{BG} < V_{on}$ region (Fig. 1e), no electron current flows because V_{BG} is below the $V_{th,n}$ of the PhC_2-BQQDI channel. However, holes accumulate in the C8-BTBT channel owing to the applied effective gate voltage (V_D–V_{BG}). However, the hole current is suppressed by the potential barrier at the p–n junction, resulting in no I_D in the V_{BG} range. In $V_{BG} > V_{on}$

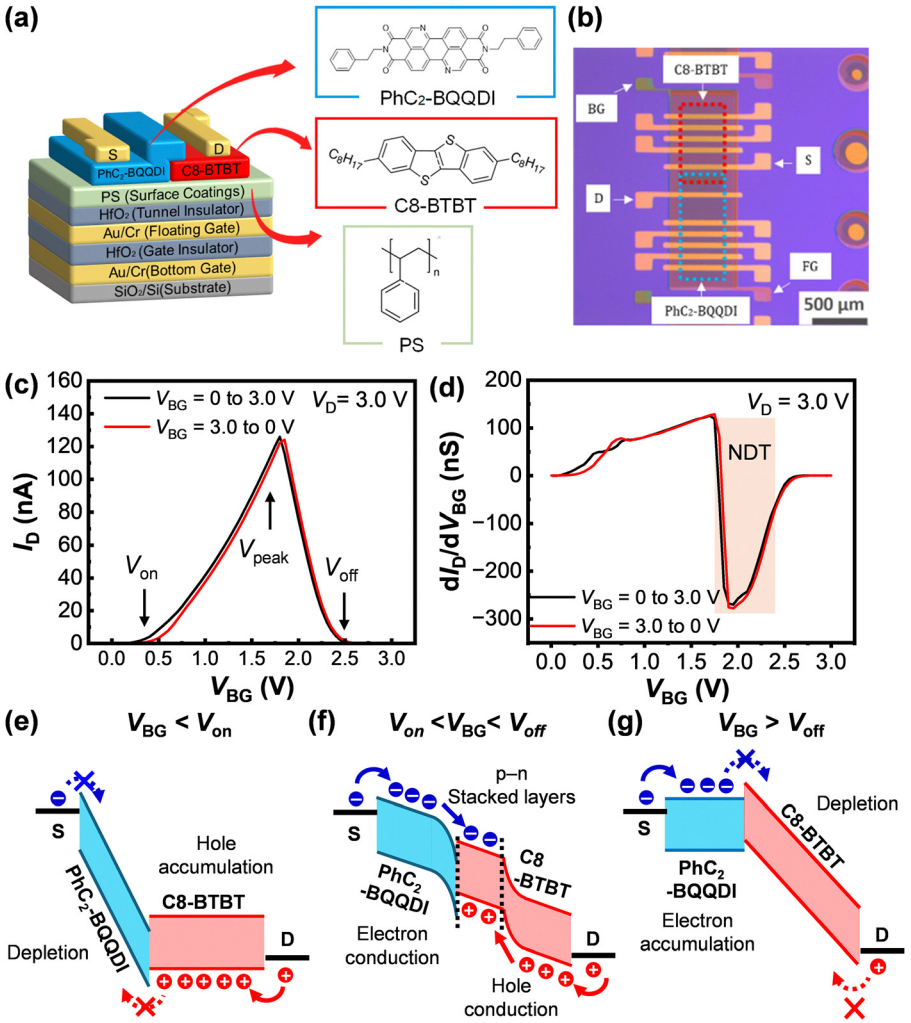

Fig. 1 (a) Device structure and (b) optical microscope image of the FG-OAAT, utilizing PhC_2-BQQDI and C8-BTBT films as transistor channels, with an Au film serving as the floating gate. (c) I_D–V_{BG} and (d) differential transconductance curve of the FG-OAAT measured at V_D = 3.0 V. (e) Illustrations of carrier transport in the FG-OAAT across V_{BG} ranges: (a) $V_{BG} < V_{on}$, (b) $V_{on} < V_{BG} < V_{off}$, and (c) $V_{off} < V_{BG}$.

(Fig. 1f), electrons are introduced from the S electrode and flow toward the D electrode. Simultaneously, the accumulated holes in the C8-BTBT channel begin to flow toward the S electrode, generating I_D in FG-OAATs. A further increase in V_{BG} ($V_{BG} > V_{off}$ Fig. 1g) hinders I_D because the C8-BTBT channel enters the off state.

Next, the Λ-shaped transfer curve in the FG-OAAT can be controlled using the Au FG. Fig. 2a–c illustrate the processes of erasing, electron trapping, and hole trapping. The corresponding I_D–V_{BG} curves are depicted in Fig. 2d, where the solid and dotted lines at each state represent the forward and reverse V_{BG} sweeps, respectively. First, the Au FG was grounded to erase the carriers (electrons or holes) in the Au FG, which is defined as the erasing process (Fig. 2a). The resulting I_D–V_{BG} curve is exhibited by the black solid and dotted lines in Fig. 2d. V_{peak} was estimated at 2.1 V. Then, V_{BG} = 5.0 V was applied for 10 s to trap electrons in the Au FG (Fig. 2b), where the S and D electrodes were grounded. This operation shifted the I_D–V_{BG} curve higher V_G, as shown by the blue solid and dotted lines in Fig. 2d. V_{peak} shifted from 2.1 to 3.1 V. Importantly, no hysteresis was observed in the shifted I_D–V_{BG} curve, revealing that the trapped electrons in the Au FG were retained during the V_{BG} sweeps. After the erasing process (Fig. 2a), the opposite BG voltage, V_{BG} = −5.0 V, was applied for 10 s to trap holes in the Au FG (Fig. 2c). As a result, V_{peak} shifted to 1.0 V (red solid and dotted line in Fig. 2d). No hysteresis appeared in the I_D–V_{BG} curve, similar to the electron-trapped sate. Consequently, the total variation in V_{peak} reached 2.1 V by controlling the charge conditions (holes or electrons) in the Au FG. This value is much larger than that observed in our previous study with a zinc-phthalocyanine-core star-shaped polymer ($ZnPc\text{-}PS_4$) as the FG.[43,48] This improvement in V_{peak} shift in this study benefits from using the Au FG.

Fig. 2e shows the retention property of electron- and hole-trapped states, where the potential of the Au FG was monitored. The trapped electrons and holes were retained for at least 1800 s. The switching behavior between the erased and electron-trapped states of the FG-OAATs is depicted

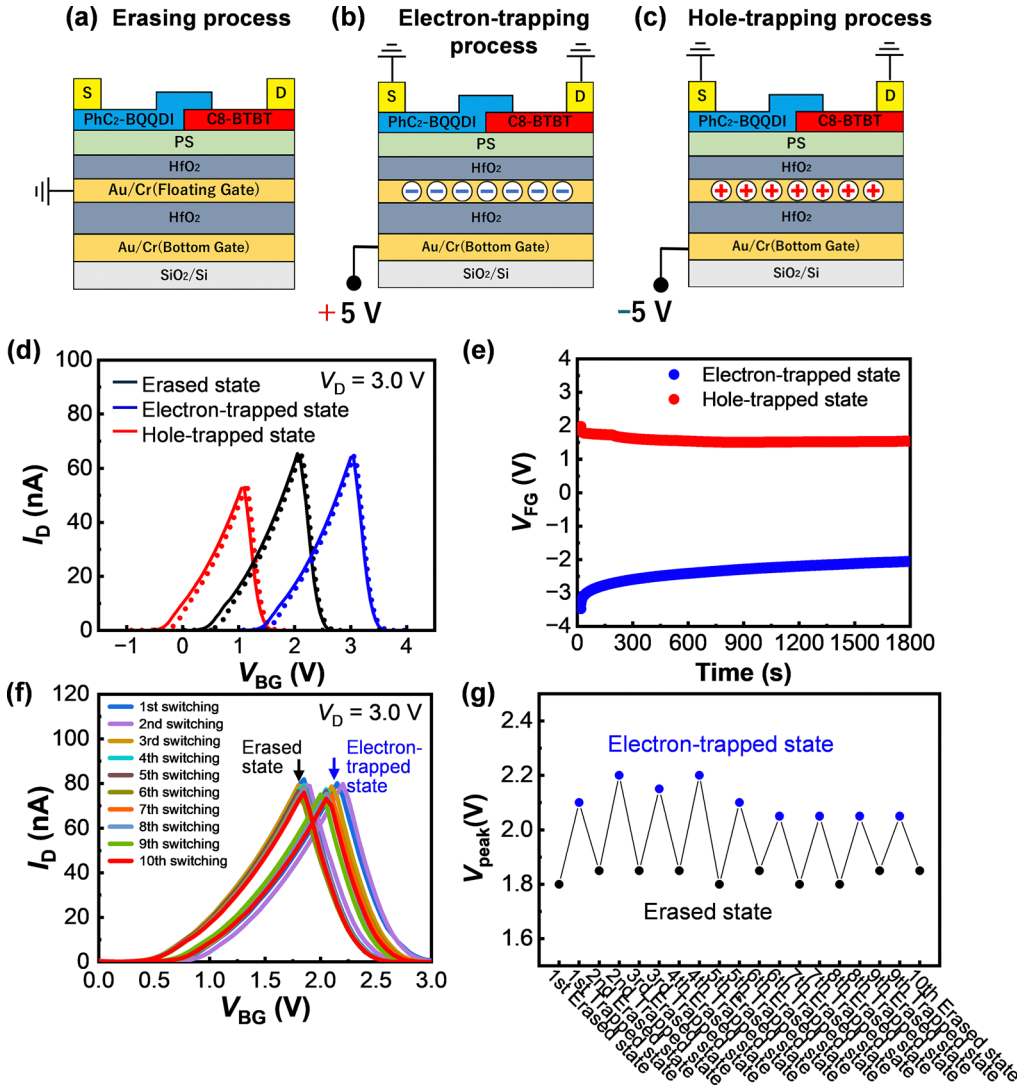

Fig. 2 (a) Erasing, (b) electron-trapping, and (c) hole-trapping processes of the FG-OAATs. (d) I_D–V_{BG} curves for the erased (black line), electron-trapped (blue line), and hole-trapped (red line) states, with solid and dotted lines representing forward and reverse V_{BG} sweeps, respectively. (e) Retention property of the FG-OAAT. (f) Switching behavior of the FG-OAAT. (g) Variation in V_{peak} values in electron-trapped and erased states as a function of switching cycles.

in Fig. 2f and g. After 10 switching cycles, the V_{peak} positions after the electron-trapping and releasing processes were almost identical.

Based on these nonvolatile memory properties, we applied the FG-OAAT to a neuromorphic device. For synaptic operations with the FG-OAAT, the BG and D electrodes function as the presynaptic input and postsynaptic output terminals, respectively. I_D was monitored as the postsynaptic current (PSC). Fig. 3a shows I_D–V_{BG} for the erased (black solid line), electron-trapped (blue solid line), and hole-trapped (red solid line) states. As shown in Fig. 3b–d, a variety of synaptic operations were reconfigured by adjusting the initial charge condition in the Au FG. First, Fig. 3b illustrates the transition from LTP to LTD with the FG-OAAT. Prior to this measurement, the initial I_D–V_{BG} curve was set to the electron-trapped state (blue solid line in Fig. 3a) by applying a V_{BG} of 5.0 V for 10 s. PSC ($I_{D,read}$) was monitored at a V_G ($V_{G,read}$) of 1.8 V and V_D ($V_{D,read}$) of 3.0 V. When negative V_{BG} pulses (V_{BG} = −5.0 V, pluse width (P_{width}) = 100 ms) were applied, $I_{D,read}$ started increasing and was maintained even after the V_{BG} pulses were turned off, indicating the LTP operation. Thereafter, $I_{D,read}$ decreased with identical positive V_{BG} pulses (V_{BG} = 5.0 V, P_{width} = 100 ms), corresponding to the LTD operation. Next, the opposite transition from LTD to LTP was observed as shown in Fig. 3c even with identical sequence of presynaptic pulses (V_{BG} = −5.0 V, P_{width} = 100 ms and V_{BG} = 5.0 V, P_{width} = 100 ms) applied to the transistor. The difference of Fig. 3b and c is the initial charge conditions in the Au FG.

In Fig. 3c, the initial I_D–V_{BG} curve was set to the erased state (black solid line in Fig. 3a). As a result, the transition from LTD to LTP was induced by applying the same sequence of V_{BG} pulses with the negative-to-positive polarity change. Finally,

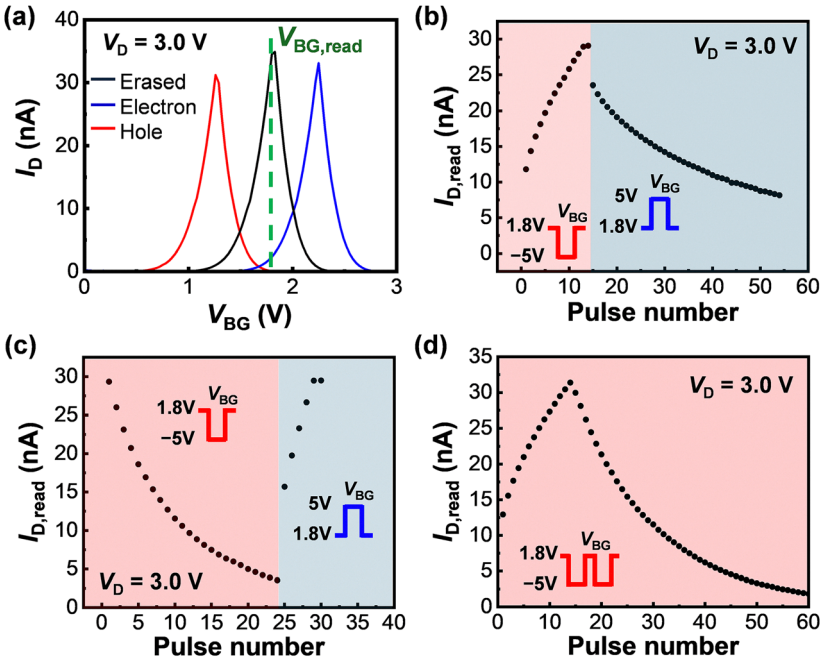

Fig. 3 (a) I_D–V_{BG} curves at the erased (black line), electron-trapped (blue line), and hole-trapped (red line) states. (b) LTP and LTD operations as a function of presynaptic pulse numbers, with the electron-trapped state defined as the initial state. (c) LTD and LTP as a function of presynaptic pulse numbers, following an erasing operation. *I.e.*, no carriers were trapped in the Au FG. (c) Transition from LTP to LTD induced by continuous presynaptic pulses.

Fig. 3d shows that the transition from LTP to LTD can be induced by applying only negative V_{BG} pulses (V_{BG} = −5.0, P_{width} = 100 ms) continuously. (V_{BG} = −5 V, P_{width} = 100 ms) (Fig. 3d). Here, the initial I_D–V_{BG} curve was set to the electron-trapped state (blue solid line in Fig. 3a).

The abovementioned results clearly reveal that reconfigurable synaptic operations, transitioning from LTP to LTD and *vice versa*, can be achieved by controlling the initial charge conditions of the Au FG. Such synaptic plasticity has typically not been demonstrated in conventional transistors, which exhibit unipolar carrier transport.[21–26] By contrast, biological synapses are known to display different responses to synaptic plasticity under neuromodulatory control, even when the same polarity, applied voltage, and pulse width are applied.[27–30] This suggests that our proposed transistor has the potential to truly mimic biological synapses. Notably, the continuous V_{BG} pulse applications in Fig. 3d enabled a smooth transition from LTP to LTD, while a sharp drop in $I_{D,read}$ was observed in Fig. 3b when the V_{BG} pulse polarity was reversed. The nonlinearity coefficients and asymmetric factors of LTP/LTD behaviors were also improved by the continuous V_{BG} pulse applications (Fig. S6 in ESI†). This improvement offers an additional advantage of using our proposed transistor.

In a similar manner to the LTP/LTD behaviors, excitatory/inhibitory and PPF/PPD operations were electrically reconfigured, as shown in Fig. 4. Fig. 4a shows the I_D–V_{BG} curves before (black dotted line) and after (black solid line) the application of a negative V_{BG} pulse (V_{BG} = −5 V for 100 ms), where no carriers were accumulated in the Au FG in the initial state (black dotted line). The corresponding variation in $I_{D,read}$ is depicted in Fig. 4b, where $I_{D,read}$ was monitored at $V_{G,read}$ = 1.2 V and $V_{D,read}$ = 3.0 V. A sharp increase in $I_{D,read}$ from 25 to 40 nA was observed by the application of a negative V_{BG} pulse (V_{BG} = −5 V for 100 ms). Importantly, $I_{D,read}$ was maintained at 30 nA after the V_{BG} pulse was turned off, due to the threshold voltage shift induced by the hole-trapping process in the Au FG. This variation in $I_{D,read}$ corresponds to the excitatory synaptic operation. The synaptic plasticity was changed by the presynaptic input pulse. Moreover, the PPF behavior distinctly appeared with the application of double-negative V_{BG} pulses (V_{BG} = −5 V for 100 ms) (Fig. 4c). The FFP ratio ($I_{D,read,change}$) was calculated using the following equation:

$$I_{D,read,change} = \frac{(I_{2,read} - I_{1,read})}{I_{1,read}} \times 100(\%) \quad (3)$$

where $I_{1,read}$ and $I_{2,read}$ represent the $I_{D,read}$ values after the first and second V_{BG} pulses, respectively. The change in $I_{D,read}$ was enhanced by shortening the pulse intervals ($P_{interval}$). The FFP ratio increased from 8.0% at $P_{interval}$ = 3.5 s to 12.0% at $P_{interval}$ = 0.5 s. Moreover, the FFP curve was well fitted by double exponential equations (Fig. S7a in ESI†), exhibiting a similar response of biological synapses.

Strikingly, the opposite synaptic behaviors, namely inhibitory and PPD operations, are shown in Fig. 4d–f, even though the same V_{BG} pulses as in Fig. 4a–c were applied to the transistor. First, the I_D–V_{BG} curve was set to the red dotted line in Fig. 4d, where holes were trapped in the Au FG. Then, the application of a negative V_{BG} pulse (V_{BG} = −5 V for 100 ms) shifted the transfer curve from the red dotted line to the solid line (Fig. 4d), leading to a reduction in $I_{D,read}$, as shown in Fig. 4e. Similarly, PPD was obtained by applying the same double-negative V_{BG} pulses as in Fig. 4c. The PPD ratio was

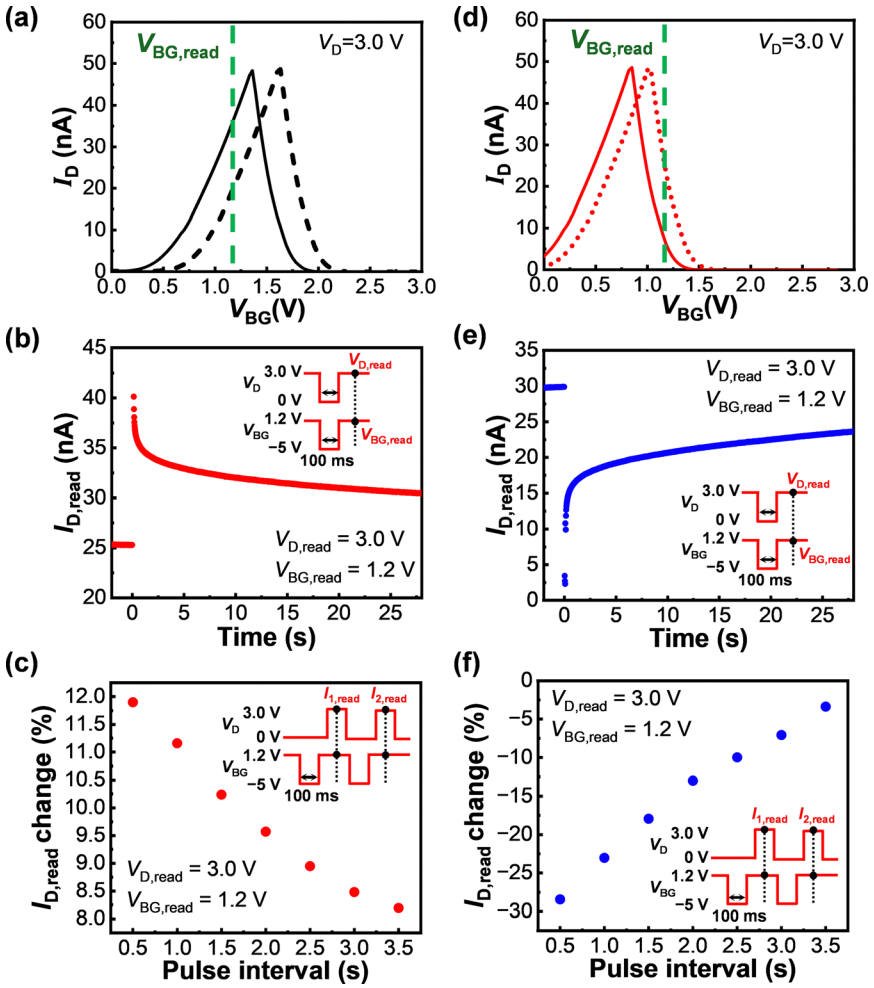

Fig. 4 (a) I_D–V_{BG} curves before (black dotted line) and after (black solid line) a presynaptic pulse application (V_{BG} = −5 V, P_{width} = 100 ms), with no carriers trapping in the Au FG at the initial state. (b) Excitatory and (c) PPF operations of the FG-OAAT, with $V_{D,read}$ and $V_{G,read}$ set to 3.0 and 1.2 V, respectively; no carriers were accumulated in the Au FG at the initial state in both cases. (d) I_D–V_{BG} curves before (red dotted line) and after (red solid line) a presynaptic pulse application (V_{BG} = −5 V, P_{width} = 100 ms), with holes trapped in the Au FG at the initial state. (e) Inhibitory and (f) PPD operations of the FG-OAAT, where holes were accumulated in the Au FG at the initial state.

varied from −2.5% at $P_{interval}$ = 3.5 s to −28.0% at $P_{interval}$ = 0.5 s with a reduction in pulse intervals.

As shown, we realized reconfigurable synaptic operations. Namely, LTP/LTD, inhibitory/excitatory, and PPF/PPD operations were electrically reconfigured by adjusting the charging conditions of the Au FG. Such reconfigurable synaptic operations have not been attained in other neuromorphic devices. Conversely, our transistor enables versatile operations without changing the presynaptic signals, similar to biological synapses. Thus, our proposed transistors have the potential to enable brain-like computing architectures, surpassing the limitations of the current von Neumann model.

4. Conclusions

We achieved reconfigurable artificial synapses with FG-OAAT, using the Au film as the FG. The transistor exhibited a typical Λ-shaped transfer curve. Notably, the Au FG induced a large V_{peak} shift in the transfer curve by controlling hole- and electron-trapping processes. This feature was applied to reconfigurable synaptic operations, where excitatory/inhibitory, LTP/LTD, and PPF/PPD behaviors were electrically reconfigured by adjusting the charge conditions of the Au FG. Importantly, these versatile synaptic operations were induced by identical presynaptic input signals, similar to those of the human brains. These findings are expected to pave the way for highly brain-like AI systems, advancing the evolution of computing systems.

Author contributions

This manuscript was written through the contributions of all authors.

Conflicts of interest

The authors declare no competing financial interest.

Data availability

The data that support the findings of this study are available from the corresponding authors upon reasonable request.

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